FAIRCHILD
SEMICONDUCTOR™

March 1999

NM25C041
4K-Bit Serial Interface CMOS EEPROM (Serial Peripheral Interface (SPI™) Synchronous Bus)

General Description

The NM25C041 is a 4096-bit MODE 1 SPI (Serial Peripheral Interface) CMOS EEPROM which is designed for high-reliability non-volatile data storage applications. The SPI interface features a byte-wide format (all data is transferred in 8-bit words) to interface with the Motorola 68HC11 microprocessor, or equivalent, at a 2.1MHz clock transfer rate. (This interface is considered the fastest serial communication method.) This 4-wire SPI interface allows the end user full EEPROM functionality while keeping pin count and space requirements low for maximum PC board space utilization.

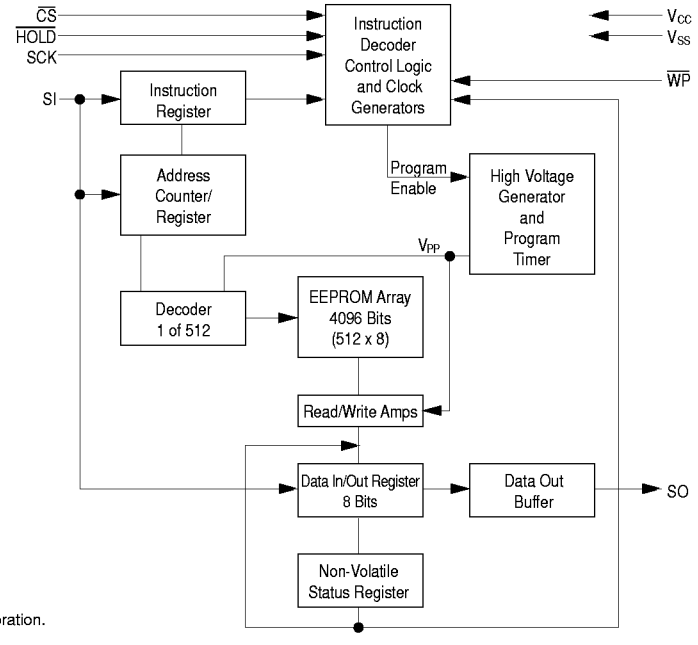
The SPI interface requires four I/O pins on each EEPROM device: Chip Select ($\overline{CS}$), Clock (SCK), Serial Data In (SI), and Serial Data Out (SO), as well as 2 other control pins: Write Protect ($\overline{WP}$) and HOLD ($\overline{HOLD}$). The Write Protect pin can be used to disable the Write operation and the $\overline{HOLD}$ pin is used to interrupt the SI datastream and place the device in a Hold state during microprocessor instruction generation. Please refer to the following diagrams and description for more details.

All programming cycles are completely self-timed and do not require an ERASE, or similar setup, before programming any cells. Programming can be performed in 3 modes, address (byte) write, page (4 addresses/bytes) write or **partial** page write. Furthermore, the EEPROM is provided with 4 levels of write protection wherein the data, once programmed, cannot be altered. This is controlled by the Status Register and is described in greater detail within this datasheet. In order to prevent spurious programming, the EEPROM has both a Write Enable command, which is immediately disabled after each programming operation, and a Write Protect ($\overline{WP}$) pin, which must be pulled HIGH to program.

Features

- 2.1 MHz clock rate @ 2.7V to 5.5V
- 4096 bits organized as 512 x 8
- Multiple chips on the same 3 wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor RDY/BUSY
- Both the Write Protect ($\overline{WP}$) pin and 'auto-write disable after programming' provides hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP and 8-pin SO

Block Diagram

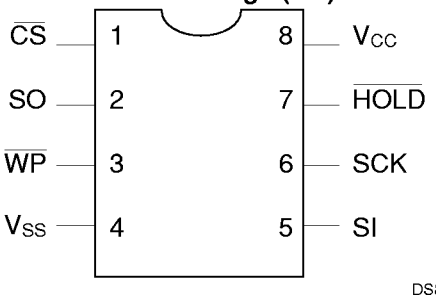


SPI™ is a trademark of Motorola Corporation.

DS800002-1

Connection Diagram

Dual-In-Line Package (N) and SO Package (M8)



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Top View

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

NM 25 C XX LZ E XX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 4.5V
	LZ	2.7V to 4.5V and <1µA Standby Current
Density/Mode	041	4K, mode 1
	C	CMOS
Interface	25	SPI
	NM	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C041	0°C to +70°C
NM25C041E	-40°C to +85°C
NM25C041V	-40°C to +125°C
Power Supply (V_{CC})	
NM25C041	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \le V_{CC} \le 5.5V$

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS} = V_{IL}$		3	mA
I_{CCSB}	Standby Current	$\overline{CS} = V_{CC}$		50	µA
I_{IL}	Input Leakage	V_{IN} = 0 to V_{CC}	-1	1	µA
I_{OL}	Output Leakage	V_{OUT} = GND to V_{CC}	-1	1	µA
V_{IL}	Input Low Voltage		-0.3	V_{CC} * 0.3	V
V_{IH}	Input High Voltage		0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA	V_{CC} - 0.8		V
f_{OP}	SCK Frequency			2.1	MHz
t_{RI}	Input Rise Time			2.0	µs
t_{FI}	Input Fall Time			2.0	µs
t_{CLH}	Clock High Time	(Note 2)	190		ns
t_{CLL}	Clock Low Time	(Note 2)	190		ns
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time		240		ns
t_{DIS}	Data Setup Time		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		240		ns
t_{DIN}	Data Hold Time		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay	C_L = 200 pF		240	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			100	ns
t_{DF}	Output Disable Time	C_L = 200 pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			100	ns
t_{WP}	Write Cycle Time	1–4 Bytes		10	ms

Capacitance (Note 4) $T_A = 25°C$, f = 2.1/1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} - 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, $t_{CLH} + t_{CLL}$ must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 3: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V_{CC} ≤ 4.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C041L/LZ	0°C to +70°C
NM25C041LE/LZE	-40°C to +85°C
NM25C041LV	-40°C to +125°C
Power Supply (V_{CC})	2.7V - 4.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 4.5V

Symbol	Parameter	Conditions	25C041L/LE 25C041LZ/LZE		25C041LV		Units
			Min.	Max.	Min	Max	
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}		3		3	mA
I_{CCSB}	Standby Current L LZ	$\overline{CS}$ = V_{CC}		 10 1	µA	 10 N/A	
I_{IL}	Input Leakage	V_{IN} = 0 to V_{CC}	-1	1	-1	1	µA
I_{OL}	Output Leakage	V_{OUT} = GND to V_{CC}	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.3	V_{CC} * 0.3	-0.3	V_{CC} * 0.3	V
V_{IH}	Input High Voltage		0.7 * V_{CC}	V_{CC} + 0.3	0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 0.8 mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.8 mA	V_{CC} - 0.8		V_{CC} - 0.8		V
f_{OP}	SCK Frequency			1.0		1.0	MHz
t_{RI}	Input Rise Time			2.0		2.0	µs
t_{FI}	Input Fall Time			2.0		2.0	µs
t_{CLH}	Clock High Time	(Note 6)	410		410		ns
t_{CLL}	Clock Low Time	(Note 6)	410		410		ns
t_{CSH}	Min. $\overline{CS}$ High Time	(Note 7)	500		500		ns
t_{CSS}	$\overline{CS}$ Setup Time		500		500		ns
t_{DIS}	Data Setup Time		100		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		240		240		ns
t_{CSN}	$\overline{CS}$ Hold Time		500		500		ns
t_{DIN}	Data Hold Time		100		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		240		240		ns
t_{PD}	Output Delay			500		500	ns
t_{DH}	Output Hold Time		0		0		ns
t_{LZ}	$\overline{HOLD}$ Output Low Z			240		240	ns
t_{DF}	Output Disable Time			500		500	ns
t_{HZ}	$\overline{HOLD}$ to Output Hi Z			240		240	ns
t_{WP}	Write Cycle Time	1-4 Bytes		15		15	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} - 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

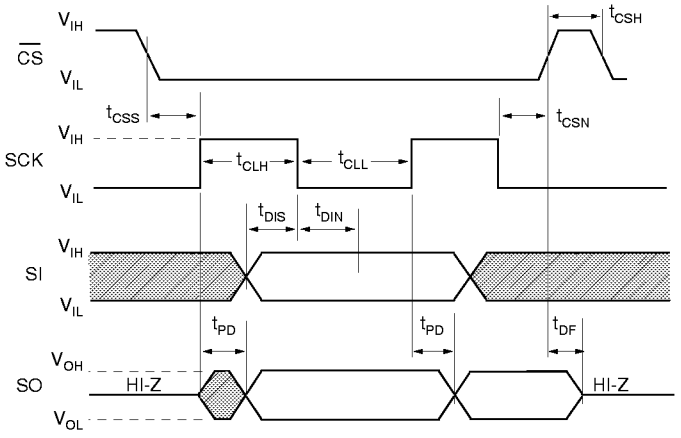
Note 6 : The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 7: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

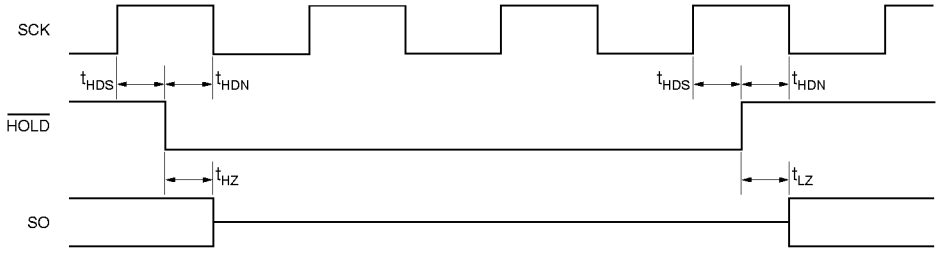
AC Test Conditions (Continued)

FIGURE 1. Synchronous Data Timing



DS800002-4

FIGURE 2. HOLD Timing



DS800002-6

Functional Description

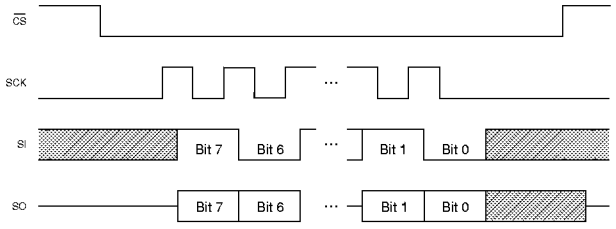
TABLE 1. Op Codes Table

Instruction Name	Instruction Opcode	Operation
WREN	0000 0110	Set Write Enable Latch
WRDI	0000 0100	Reset Write Enable Latch
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 A011	Read Data from Memory Array
WRITE	0000 A010	Write Data to Memory Array

Note: As the NM25C040 requires 9 address bits (4,096 ÷ 8 = 512 bytes = 2^9), the 9th bit (for R/$\overline{W}$ instructions) is inputted in the Instruction Set Byte in bit I_3. **This convention only applies to 4K SPI protocol.**

The NM25C041 SPI device uses a $\overline{CS}$ functionality, so the device is selected when $\overline{CS}$ is LOW ($\overline{CS}$ is to be held HIGH during 'standby' periods and between instruction sets). As stated above, the SPI protocol defines this as a MODE 1 part, with a CLOCK PHASE 1 and CLOCK POLARITY 0. This means that the part is active with $\overline{CS}$ = 0 (V_{IL}), all INPUT data is latched into the device on the RISING edge of SCK and all OUTPUT data is clocked out on the FALLING edge of SCK.

FIGURE 3. SPI Protocol

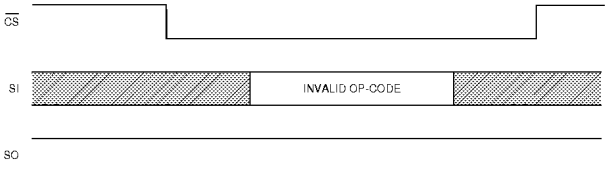


DS800002-5

The HOLD pin operation is used when the device is selected ($\overline{CS}$ LOW) and the application requires that the SI datastream be stopped and then restarted. The HOLD pin allows a fully 'static' operation, wherin the device may be put on HOLD by bringing the HOLD pin LOW (V_{IL}). During the HOLD state, SCK must be HIGH and $\overline{CS}$ must remain LOW (device selected). In order to resume EEPROM serial communication, HOLD must be again brought HIGH and the SCK/SI signals resumed. During the HOLD state, SO is tri-stated (high impedance).

As an additional protection against data corruption, the device is designed so that, if an invalid opcode is received, the device will not shift any further data into the SI latches and SO will remain tri-stated. In this case, $\overline{CS}$ must again be brought HIGH to re-initialize the device and a new opcode re-entered. See Figure 4.

FIGURE 4. Invalid Op-Code

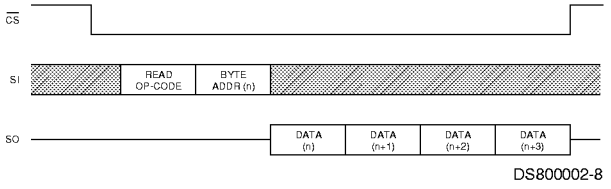


DS800002-7

READ STATUS REGISTER (RDSR): The Read Status Register (RDSR) instruction provides access to the status register which is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

READ SEQUENCE: Reading the memory via the SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) to be read. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached (1FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 5.

FIGURE 5. Read Sequence



DS800002-8

Functional Description (Continued)

TABLE 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	RDY

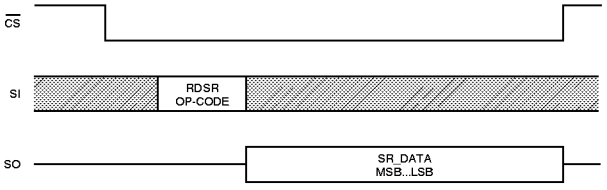
X = Don't Care

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. **Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s.** See Figure 6.

TABLE 3. Block Write Protection Levels

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	180–1FF
2	1	0	100–1FF
3	1	1	000–1FF

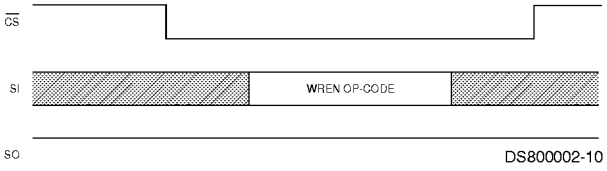
FIGURE 6. Read Status



DS800002-9

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all modes must be preceded by a WRITE ENABLE (WREN) instruction. Additionally the $\overline{WP}$ pin must be held high during a WRITE ENABLE instruction. At the completion of a WRITE or WRSR cycle the device is automatically turned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction or forcing the $\overline{WP}$ pin low will also return the device to the write disable state. See Figure 7.

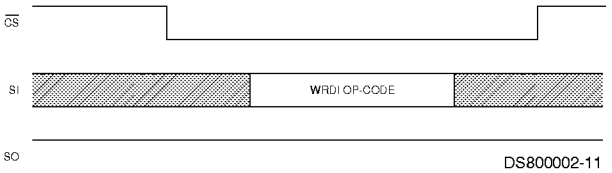
FIGURE 7. Write Enable



DS800002-10

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. The WRITE DISABLE instruction is independent of the status of the $\overline{WP}$ pin. See Figure 8.

FIGURE 8. Write Disable

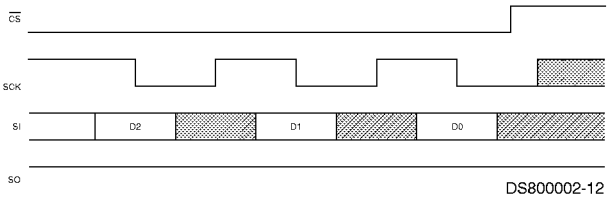


DS800002-11

WRITE SEQUENCE: To program the device the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) and the corresponding pro-data (D7–D0) to be programmed. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

FIGURE 9. Start WRITE Condition

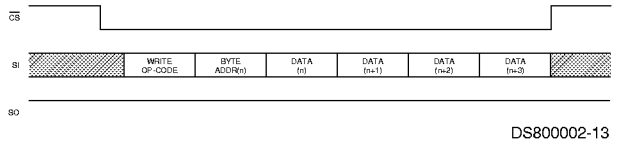


DS800002-12

Functional Description (Continued)

The NM25C041 is capable of a four byte PAGE WRITE operation. After receipt of each byte of data the two low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than four bytes of data, the address counter will "roll over", and the previously loaded data will be reloaded. See Figure 10.

FIGURE 10. 4 Page Byte Write



DS800002-13

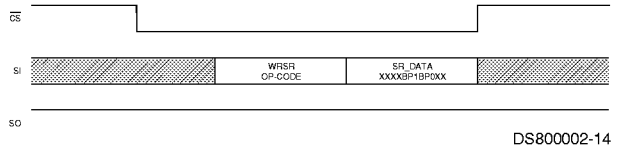
At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the WP pin is forced low or the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when CS is forced high. A new CS falling edge is required to re-initialize the serial communication.

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). As in the WRITE mode the WRITE PROTECT (WP) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

The WRSR command requires the following sequence. The CS line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed (see Figure 11).

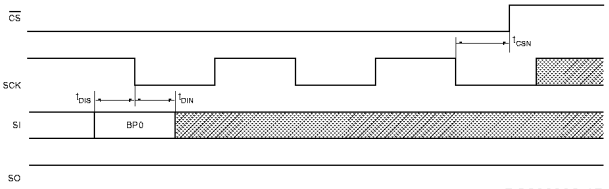
FIGURE 11. Write Status Register



DS800002-14

Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the CS pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the CS pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 12.

FIGURE 12. Start WRSR Condition

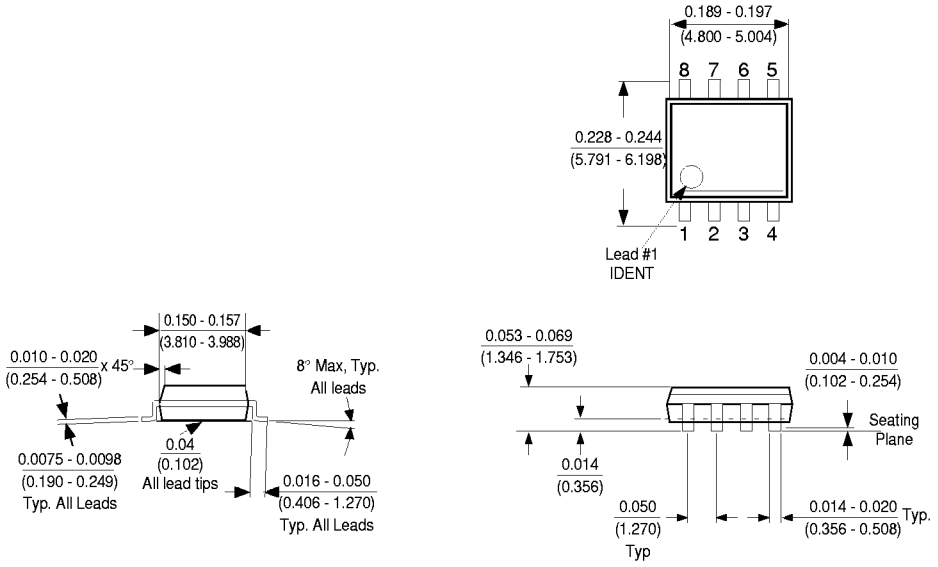


DS800002-15

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

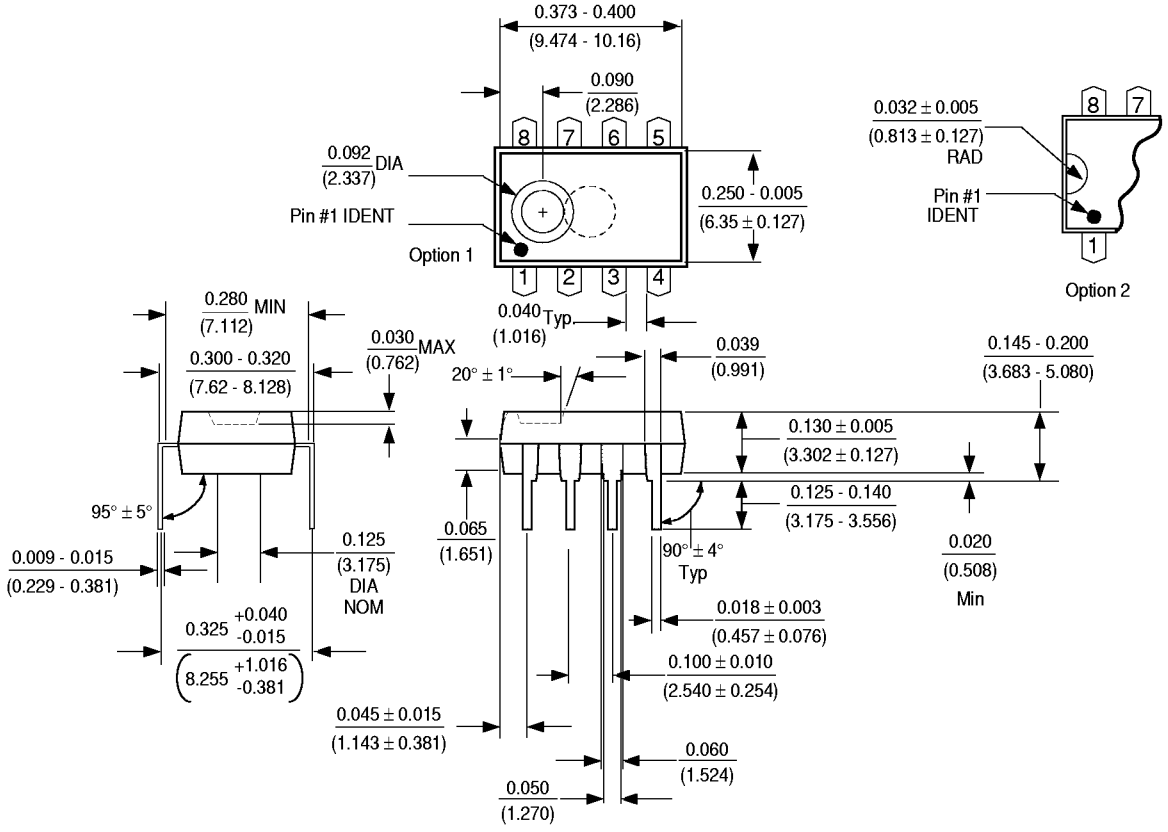
At the completion of a WRSR cycle the device is automatically returned to the write disable state.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Order Number NM25C041M8
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number NM25C041N
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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