

Features

- Split Gate Trench MOSFET Technology
- Excellent Package for Heat Dissipation
- High Density Cell Design for Low $R_{DS(ON)}$
- Halogen Free Available Upon Request By Adding Suffix "-HF"
- Epoxy Meets UL 94 V-0 Flammability Rating
- Lead Free Finish/RoHS Compliant ("P" Suffix Designates RoHS Compliant. See Ordering Information)
- Moisture Sensitivity Level 1

Maximum Ratings

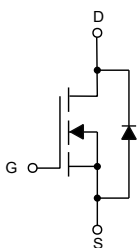
- Operating Junction Temperature Range : -55°C to +150°C
- Storage Temperature Range: -55°C to +150°C
- Thermal Resistance: 15°C/W Junction to Ambient($t \leq 10S$)⁽¹⁾
- Thermal Resistance: 60°C/W Junction to Ambient(Steady-State)⁽¹⁾
- Thermal Resistance: 0.48°C/W Junction to Case

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	120	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	90	A
Pulsed Drain Current ⁽²⁾	I_{DM}	360	A
Total Power Dissipation ⁽³⁾	P_D	260	W
Single Pulsed Avalanche Energy ⁽⁴⁾	E_{AS}	306	mJ

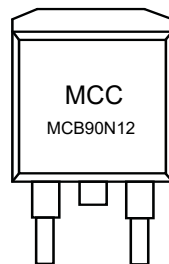
Note:

1. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ C$. The Power dissipation PDSM is based on $R_{\theta JA}$ $t \leq 10s$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
2. Repetitive rating; pulse width limited by max. junction temperature.
3. P_D is based on max. junction temperature, using junction-case thermal resistance.
4. $V_{DD}=50V$, $R_G=25\Omega$, $L=0.5mH$, $T_J=25^\circ C$.

Internal Structure and Marking Code

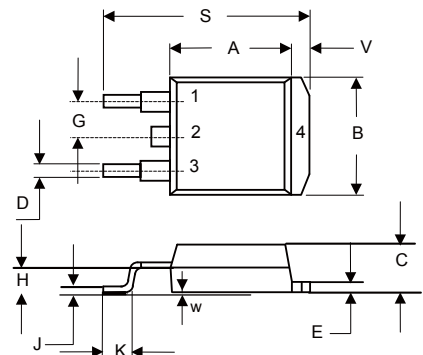


1. Gate
- 2,4. Drain
3. Source



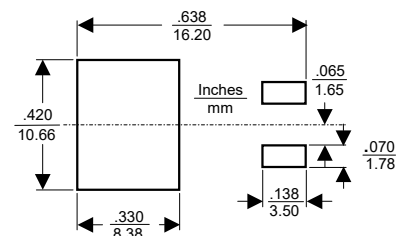
**N-CHANNEL
MOSFET**

D²-PAK



DIM	DIMENSIONS				NOTE
	INCHES		MM		
	MIN	MAX	MIN	MAX	
A	0.331	0.370	8.40	9.40	
B	0.378	0.417	9.60	10.60	
C	0.165	0.189	4.20	4.80	
D	0.027	0.037	0.68	0.94	
E	0.045	0.055	1.14	1.40	
G	0.010		2.54		TYP.
H	0.096	0.134	2.43	3.40	
J	0.011	0.025	0.28	0.64	
K	0.071	0.131	1.80	3.32	
S	0.575	0.625	14.60	15.87	
V	0.042	0.058	1.07	1.47	
W	0.000	0.010	0.00	0.25	

Suggested Solder Pad Layout



Electrical Characteristics @ 25°C (Unless Otherwise Specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	120			V
Gate-Source Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=120V, V_{GS}=0V$			1	μA
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3.2	4	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		6.2	7.2	m Ω
Gate Resistance	R_G	f=1MHz, Open drain		0.9		Ω
Diode Characteristics						
Continuous Body Diode Current	I_S				90	A
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=20A$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F=20A, di_F/dt=100A/\mu s$		84		ns
Reverse Recovery Charge	Q_{rr}			191		nC
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V, f=1MHz$		4514		pF
Output Capacitance	C_{oss}			1110		
Reverse Transfer Capacitance	C_{rss}			34		
Total Gate Charge	Q_g	$V_{DS}=50V, V_{GS}=10V, I_D=20A$		65		nC
Gate-Source Charge	Q_{gs}			25.9		
Gate-Drain Charge	Q_{gd}			8.9		
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=50V, V_{GEN}=10V, R_G=2.2\Omega, I_{DS}=20A$		21.6		ns
Turn-On Rise Time	t_r			39.9		
Turn-Off Delay Time	$t_{d(off)}$			35		
Turn-Off Fall Time	t_f			40.9		

Curve Characteristics

Fig. 1 - Typical Output Characteristics

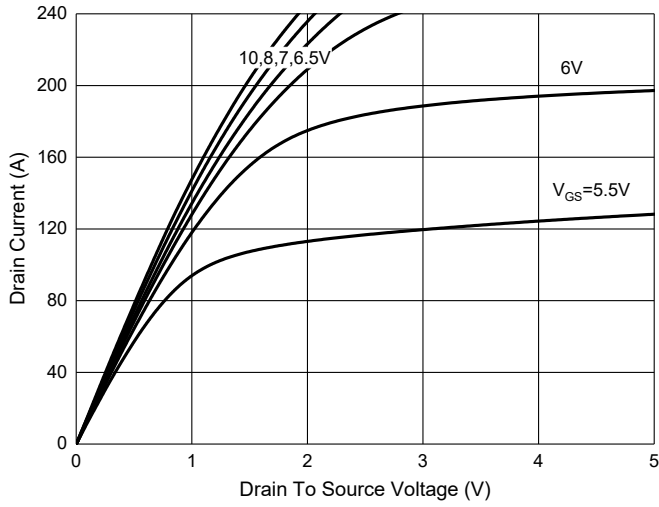


Fig. 2 - Transfer Characteristics

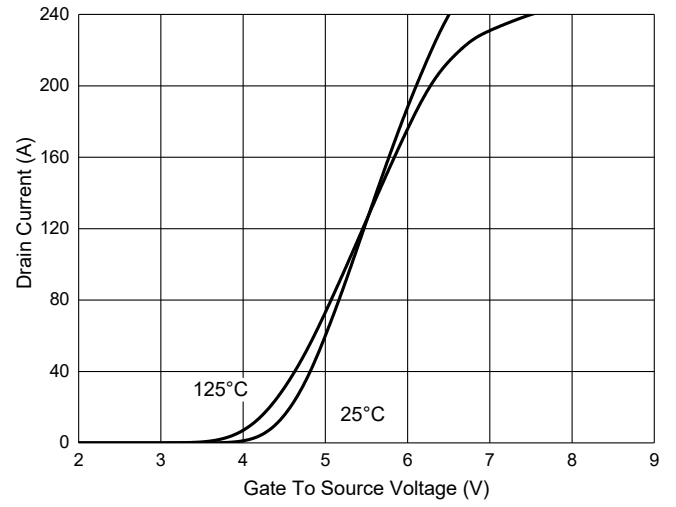


Fig. 3 - $R_{DS(ON)} - V_{GS}$

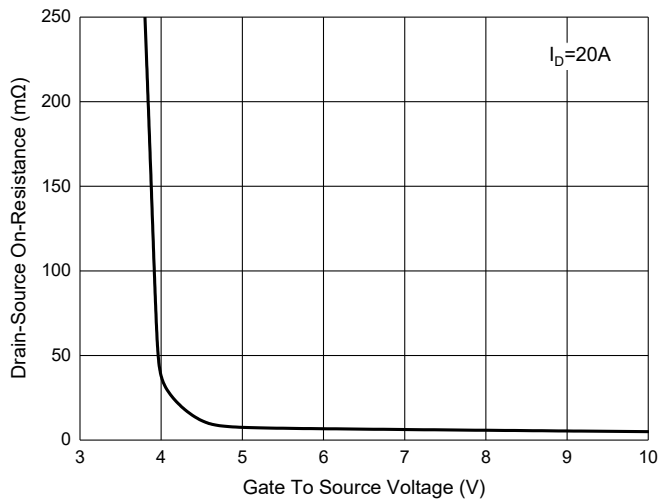


Fig. 4 - Normalized On Resistance Characteristics

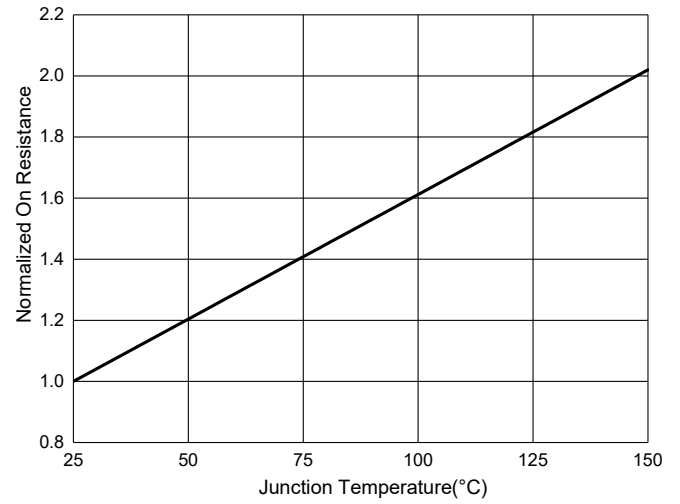


Fig. 5 - Capacitance Characteristics

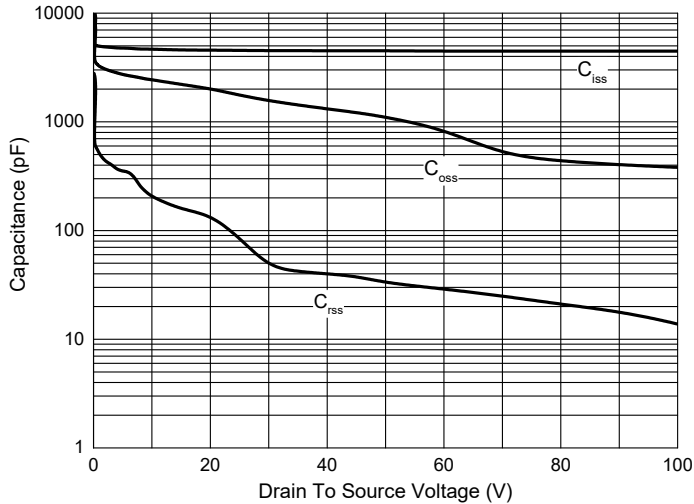
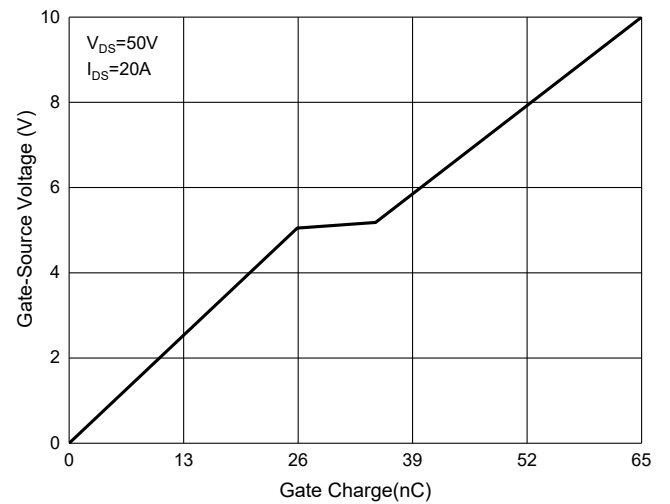
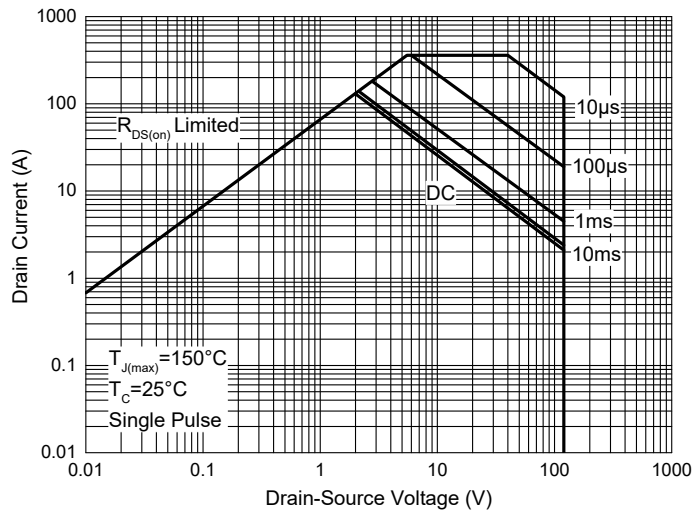


Fig. 6 - Gate Charge



Curve Characteristics

Fig. 7 - Safe Operation Area



Ordering Information

Device	Packing
Part Number-TP	Tape&Reel: 800pcs/Reel

Note : Adding "-HF" Suffix for Halogen Free, eg. Part Number-TP-HF

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