4.0 ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	−65 °C to +150 °C
Case Temperature Under Bias(2)	−40 °C to +125 °C
Supply Voltage wrt. V_{SS}	−0.5V to +6.5V
Voltage on Other pins wrt V_{SS}	−0.5V to V_{CC} +0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2. Operating Conditions

Operating Conditions (80960CF-33, -25, -16)

Symbol	Parameter		Min	Max	Units	Notes
V_{CC}	Supply Voltage	80960CF-30	4.75	5.25	V	
		80960CF-25	4.50	5.50		
		80960CF-16	4.50	5.50		
f_{CLK2x}	Input Clock Frequency (2-x Mode)	80960CF-30	0	60.6	MHz	
		80960CF-25	0	50	MHz	
		80960CF-16	0	32	MHz	
f_{CLK1x}	Input Clock Frequency (1-x Mode)	80960CF-30	8	30.3	MHz	(1)
		80960CF-25	8	25	MHz	
		80960CF-16	8	16	MHz	
T_C	Case Temperature Under Bias 80960CF-30, -25, -16	PGA Package	−40	+110	°C	

NOTES:
(1) When in the 1-x input clock mode, CLKIN is an input to an internal phase-locked loop and must maintain a minimum frequency of 8 MHz for proper processor operation. However, in the 1-x Mode, CLKIN may still be stopped when the processor either is in a reset condition or is reset. If CLKIN is stopped, the specified $\overline{\text{RESET}}$ low time must be provided once CLKIN restarts and has stabilized.
(2) Case temperatures are "Instant On".

4.3 Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} (GND) pins. Every 80960CF-based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "N.C." **must not** be connected in the system.

Liberal decoupling capacitance should be placed near the 80960CF. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA packages will offer the lowest possible inductance.

For reliable operation, always connect unused inputs to an appropriate signal level. In particular, any unused interrupt ($\overline{\text{XINT}}$, $\overline{\text{NMI}}$) or DMA ($\overline{\text{DREQ}}$) input should be connected to V_{CC} through a pull-up resistor, as should $\overline{\text{BTERM}}$ if not used. Pull-up resistors should be in the range of 20 KΩ for each pin tied high. If $\overline{\text{READY}}$ or HOLD are not used, the unused input should be connected to ground. **N.C. pins must always remain unconnected.** Refer to the *i960 CA Microprocessor Reference Manual* for more information.

4.4. DC Specifications

DC Characteristics
(80960CF-30, -25, -16 under the conditions described in **Section 4.2, Operating Conditions.**)

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage for all pins except $\overline{RESET}$	−0.3	0.8	V	
V_{IH}	Input High Voltage for all pins except $\overline{RESET}$	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5 mA
V_{OH}	Output High Voltage I_{OH} = −1mA I_{OH} = −200μA	2.4 V_{CC} − 0.5		V V	
V_{ILR}	Input Low Voltage for $\overline{RESET}$	− 0.3	1.5	V	
V_{IHR}	Input High Voltage for $\overline{RESET}$	3.5	V_{CC} + 0.3	V	
I_{LI1}	Input Leakage Current for each pin *except*: $\overline{BTERM}$, $\overline{ONCE}$, $\overline{DREQ3:0}$, STEST, $\overline{EOP3:0}$/$\overline{TC3:0}$, $\overline{NMI}$, $\overline{XINT7:0}$, $\overline{READY}$, HOLD, $\overline{BOFF}$, CLKMODE		±15	μA	0V≤V_{IN}≤V_{CC} (1)
I_{LI2}	Input Leakage Current for: $\overline{BTERM}$, $\overline{ONCE}$, $\overline{DREQ3:0}$, STEST, $\overline{EOP3:0}$/$\overline{TC3:0}$, $\overline{NMI}$, $\overline{XINT7:0}$, $\overline{BOFF}$	0	−325	μA	V_{IN} = 0.45V (2)
I_{LI3}	Input Leakage Current for: $\overline{READY}$, HOLD, CLKMODE	0	500	μA	V_{IN} = 2.4V (3)
I_{LO}	Output Leakage Current		±15	μA	0.45V≤V_{OUT}≤V_{CC}
I_{CC}	Supply Current (80960CF-30) I_{CC} Max I_{CC} Typ		 1150 960	 mA	 (4) (5)
I_{CC}	Supply Current (80960CF-25) I_{CC} Max I_{CC} Typ		 950 775	 mA	 (4) (5)
I_{CC}	Supply Current (80960CF-16) I_{CC} Max I_{CC} Typ		 750 575	 mA	 (4) (5)
I_{ONCE}	ONCE-mode Supply Current		150	mA	
C_{IN}	Input Capacitance for: CLKIN, $\overline{RESET}$, $\overline{ONCE}$, $\overline{READY}$, HOLD, $\overline{DREQ3:0}$, $\overline{BOFF}$ $\overline{XINT7:0}$, $\overline{NMI}$, $\overline{BTERM}$, CLKMODE	0	12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance of each output pin		12	pF	F_C = 1 MHz, (6)
$C_{I/O}$	I/O Pin Capacitance		12	pF	F_C = 1 MHz

NOTES:
(1) No Pull-up or pull-down.
(2) These pins have internal pullup resistors.
(3) These pins have internal pulldown resistors.
(4) Measured at worst case frequency, V_{CC} and temperature, with device operating and outputs loaded to the test conditions described in **Section 4.5.1, AC Test Conditions.**
(5) I_{CC} Typical is not tested.
(6) Output Capacitance is the capacitive load of a floating output.
(7) CLKMODE pin has a pulldown resistor only when $\overline{ONCE}$ pin is deasserted.

4.5 AC Specifications

AC Characteristics — 80960CF-30

(80960CF-30 only, under the conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions.**) See notes which follow this table.

Symbol	Parameter		Min	Max	Units	Notes
INPUT CLOCK(10)						
T_F	CLKIN Frequency		0	60.6	MHz	(1)
T_C	CLKIN Period	In 1-x Mode (f_{CLK1x})	33	125	ns	(1,12)
		In 2-x Mode (f_{CLK2x})	16.5	∞	ns	(1)
T_{CS}	CLKIN Period Stability	In 1-x Mode (f_{CLK1x})		±0.1%	Δ	(1,13)
T_{CH}	CLKIN High Time	In 1-x Mode (f_{CLK1x})	6	62.5	ns	(1,12)
		In 2-x Mode (f_{CLK2x})	6	∞	ns	(1)
T_{CL}	CLKIN Low Time	In 1-x Mode (f_{CLK1x})	6	62.5	ns	(1,12)
		In 2-x Mode (f_{CLK2x})	6	∞	ns	(1)
T_{CR}	CLKIN Rise Time		0	6	ns	(1)
T_{CF}	CLKIN Fall Time		0	6	ns	(1)
OUTPUT CLOCKS(9)						
T_{CP}	CLKIN to PCLK2:1 Delay	In 1-x Mode (f_{CLK1x})	−2	2	ns	(1,3,13,14)
		In 2-x Mode (f_{CLK2x})	2	25	ns	(1,3)
T	PCLK2:1 Period	In 1-x Mode (f_{CLK1x})	T_C		ns	(1,13)
		In 2-x Mode (f_{CLK2x})	$2T_C$		ns	(1,3)
T_{PH}	PCLK2:1 High Time		(T/2) − 2	T/2	ns	(1,13)
T_{PL}	PCLK2:1 Low Time		(T/2) − 2	T/2	ns	(1,13)
T_{PR}	PCLK2:1 Rise Time		1	4	ns	(1,3)
T_{PF}	PCLK2:1 Fall Time		1	4	ns	(1,3)
SYNCHRONOUS OUTPUTS(10)						
T_{OV} T_{OH}	Output Valid Delay, Output Hold					(6, 11)
	T_{OV1}, T_{OH1}	A31:2	3	14	ns	
	T_{OV2}, T_{OH2}	$\overline{BE3:0}$	3	16	ns	
	T_{OV3}, T_{OH3}	$\overline{ADS}$	6	18	ns	
	T_{OV4}, T_{OH4}	W/$\overline{R}$	3	18	ns	
	T_{OV5}, T_{OH5}	D/$\overline{C}$, $\overline{SUP}$, $\overline{DMA}$	4	16	ns	
	T_{OV6}, T_{OH6}	$\overline{BLAST}$, $\overline{WAIT}$	5	16	ns	
	T_{OV7}, T_{OH7}	$\overline{DEN}$	3	16	ns	
	T_{OV8}, T_{OH8}	HOLDA, BREQ	4	16	ns	
	T_{OV9}, T_{OH9}	$\overline{LOCK}$	4	16	ns	
	T_{OV10}, T_{OH10}	$\overline{DACK3:0}$	4	18	ns	
	T_{OV11}, T_{OH11}	D31:0	3	16	ns	
	T_{OV12}, T_{OH12}	DT/$\overline{R}$	T/2 + 3	T/2 + 14	ns	
	T_{OV13}, T_{OH13}	$\overline{FAIL}$	2	14	ns	(6, 11)
	T_{OV14}, T_{OH14}	$\overline{EOP}$/$\overline{TC3:0}$	3	18	ns	
T_{OF}	Output Float for all outputs		3	22	ns	(6)
SYNCHRONOUS INPUTS(10)						
T_{IS}	Input Setup					
	T_{IS1}	D31:0	3		ns	(1,11)
	T_{IS2}	$\overline{BOFF}$	17		ns	(1,11)
	T_{IS3}	$\overline{BTERM}$/READY	7		ns	(1,11)
	T_{IS4}	HOLD	7		ns	(1,11)
T_{IH}	Input Hold					
	T_{IH1}	D31:0	5		ns	(1,11)
	T_{IH2}	$\overline{BOFF}$	5		ns	(1,11)
	T_{IH3}	$\overline{BTERM}$/READY	2		ns	(1,11)
	T_{IH4}	HOLD	3		ns	(1,11)

AC Characteristics — 80960CF-30

(80960CF-30 only, under the conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions.**) See notes which follow this table. (Continued)

Symbol	Parameter	Min	Max	Units	Notes
RELATIVE OUTPUT TIMINGS(9,7)					
T_{AVSH1}	A31:2 Valid to $\overline{ADS}$ Rising	T − 4	T + 4	ns	
T_{AVSH2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, D/$\overline{C}$, $\overline{DMA}$, $\overline{DACK3:0}$ Valid to $\overline{ADS}$ Rising	T − 6	T + 6	ns	
T_{AVEL1}	A31:2 Valid to $\overline{DEN}$ Falling	T − 4	T + 4	ns	
T_{AVEL2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, $\overline{INST}$, $\overline{DMA}$, $\overline{DACK3:0}$ Valid to $\overline{DEN}$ Falling	T − 6	T + 6	ns	
T_{NLQV}	$\overline{WAIT}$ Falling to Output Data Valid	±6		ns	
T_{DVNH}	Output Data Valid to $\overline{WAIT}$ Rising	N*T − 6	N*T + 6	ns	(4)
T_{NLNH}	$\overline{WAIT}$ Falling to $\overline{WAIT}$ Rising	N*T ± 4		ns	(4)
T_{NHQX}	Output Data Hold after $\overline{WAIT}$ Rising	(N + 1) * T − 6	(N + 1) * T + 6	ns	(5)
T_{EHTV}	DT/$\overline{R}$ Hold after $\overline{DEN}$ High	T/2 − 6	∞	ns	(6)
T_{TVEL}	DT/$\overline{R}$ Valid to $\overline{DEN}$ Falling	T/2 − 4	T/2 + 4	ns	(7)
RELATIVE INPUT TIMINGS(7)					
T_{IS5}	$\overline{RESET}$ Input Setup (2x Clock Mode)	6		ns	(14)
T_{IH5}	$\overline{RESET}$ Input Hold (2x Clock Mode)	5		ns	(14)
T_{IS6}	$\overline{DREQ3:0}$ Input Setup	12		ns	(8)
T_{IH6}	$\overline{DREQ3:0}$ Input Hold	7		ns	(8)
T_{IS7}	$\overline{XINT7:0}$, $\overline{NMI}$ Input Setup	7		ns	(8)
T_{IH7}	$\overline{XINT7:0}$, $\overline{NMI}$ Input Hold	3		ns	(8)
T_{IS8}	$\overline{RESET}$ Input Setup (1x Clock Mode)	3		ns	(15)
T_{IH8}	$\overline{RESET}$ Input Hold (1x Clock Mode)	T/4 + 1		ns	(15)

NOTES:

1. See **Section 4.5.2, AC Timing Waveforms** for waveforms and definitions.
2. See Figure 22 for capacitive derating information for output delays and hold times.
3. See Figure 23 for capacitive derating information for rise and fall times.
4. Where N is the number of N_{RAD}, N_{RDD}, N_{WAD}, or N_{WDD} wait states that are programmed in the Bus Controller Region Table. When there are no wait states in an access, $\overline{WAIT}$ never goes active.
5. N = Number of wait states inserted with $\overline{READY}$.
6. Output Data and/or DT/$\overline{R}$ may be driven indefinitely following a cycle if there is no subsequent bus activity.
7. See Notes 1, 2 and 3.
8. Since asynchronous inputs are synchronized internally by the 80960CF they have no required setup or hold times in order to be recognized and for proper operation. However, to guarantee recognition of the input at a particular edge of PCLK2:1 the setup times shown must be met. Asynchronous inputs must be active for at least two consecutive PCLK2:1 rising edges to be seen by the processor.
9. These specifications are guaranteed by the processor.
10. These specifications must be met by the system for proper operation of the processor.
11. This timing is dependent upon the loading of PCLK2:1. Use the derating curves of **Section 4.5.3** to adjust the timing for PCLK2:1 loading.
12. In the 1-x input clock mode, the maximum input clock period is limited to 125 ns while the processor is operating. When the processor is in reset, the input clock may stop even in 1-x mode.
13. When in the 1-x input clock mode, these specifications assume a stable input clock with a period variation of less than ±0.1% between adjacent cycles.
14. In 2x clock mode, $\overline{RESET}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{RESET}$ pin must meet setup and hold times to the falling edge of the CLKIN. (See Figure 28a.)
15. In 1x clock mode, $\overline{RESET}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{RESET}$ pin must be deasserted while CLKIN is high and meet setup and hold times to the rising edge of the CLKIN. (See Figure 28b.)

AC Characteristics — 80960CF-25

(80960CF-25 only, under the conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions**.)

Symbol	Parameter		Min	Max	Units	Notes
	INPUT CLOCK(10)					
T_F	CLKIN Frequency		0	50	MHz	(1)
T_C	CLKIN Period	In 1-x Mode (f_{CLK1x})	40	125	ns	(1,12)
		In 2-x Mode (f_{CLK2x})	20	∞	ns	(1)
T_{CS}	CLKIN Period Stability	In 1-x Mode (f_{CLK1x})		±0.1%	Δ	(1,13)
T_{CH}	CLKIN High Time	In 1-x Mode (f_{CLK1x})	8	62.5	ns	(1,12)
		In 2-x Mode (f_{CLK2x})	8	∞	ns	(1)
T_{CL}	CLKIN Low Time	In 1-x Mode (f_{CLK1x})	8	62.5	ns	(1,12)
		In 2-x Mode (f_{CLK2x})	8	∞	ns	(1)
T_{CR}	CLKIN Rise Time		0	6	ns	(1)
T_{CF}	CLKIN Fall Time		0	6	ns	(1)
	OUTPUT CLOCKS(9)					
T_{CP}	CLKIN to PCLK2:1 Delay	In 1-x Mode (f_{CLK1x})	−2	2	ns	(1,3,13,14)
		In 2-x Mode (f_{CLK2x})	2	25	ns	(1,3)
T	PCLK2:1 Period	In 1-x Mode (f_{CLK1x})	T_C		ns	(1,13)
		In 2-x Mode (f_{CLK2x})	$2T_C$		ns	(1,3)
T_{PH}	PCLK2:1 High Time		(T/2) − 3	T/2	ns	(1,13)
T_{PL}	PCLK2:1 Low Time		(T/2) − 3	T/2	ns	(1,13)
T_{PR}	PCLK2:1 Rise Time		1	4	ns	(1,3)
T_{PF}	PCLK2:1 Fall Time		1	4	ns	(1,3)
	SYNCHRONOUS OUTPUTS(10)					
T_{OV} T_{OH}	Output Valid Delay, Output Hold					(6, 11)
	T_{OV1}, T_{OH1}	A31:2	3	16	ns	
	T_{OV2}, T_{OH2}	$\overline{BE3:0}$	3	18	ns	
	T_{OV3}, T_{OH3}	$\overline{ADS}$	6	20	ns	
	T_{OV4}, T_{OH4}	W/$\overline{R}$	3	20	ns	
	T_{OV5}, T_{OH5}	D/$\overline{C}$,$\overline{SUP}$,$\overline{DMA}$	4	18	ns	
	T_{OV6}, T_{OH6}	$\overline{BLAST}$, $\overline{WAIT}$	5	18	ns	
	T_{OV7}, T_{OH7}	$\overline{DEN}$	3	18	ns	
	T_{OV8}, T_{OH8}	HOLDA, BREQ	4	18	ns	
	T_{OV9}, T_{OH9}	$\overline{LOCK}$	4	18	ns	
	T_{OV10}, T_{OH10}	$\overline{DACK3:0}$	4	20	ns	
	T_{OV11}, T_{OH11}	D31:0	3	18	ns	
	T_{OV12}, T_{OH12}	DT/$\overline{R}$	T/2 + 3	T/2 + 16	ns	
	T_{OV13}, T_{OH13}	$\overline{FAIL}$	2	16	ns	
	T_{OV14}, T_{OH14}	$\overline{EOP3:0}$/$\overline{TC3:0}$	3	20	ns	(6, 11)
T_{OF}	Output Float for all outputs		3	22	ns	(6)
	SYNCHRONOUS INPUTS(10)					
T_{IS}	Input Setup					
	T_{IS1}	D31:0	5		ns	(1,11)
	T_{IS2}	$\overline{BOFF}$	19		ns	(1,11)
	T_{IS3}	$\overline{BTERM}$/$\overline{READY}$	9		ns	(1,11)
	T_{IS4}	HOLD	9		ns	(1,11)
T_{IH}	Input Hold					
	T_{IH1}	D31:0	5		ns	(1,11)
	T_{IH2}	$\overline{BOFF}$	7		ns	(1,11)
	T_{IH3}	$\overline{BTERM}$/$\overline{READY}$	2		ns	(1,11)
	T_{IH4}	HOLD	5		ns	(1,11)

AC Characteristics — 80960CF-25

(80960CF-25 only, under the conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions.**) (Continued)

Symbol	Parameter	Min	Max	Units	Notes
	RELATIVE OUTPUT TIMINGS(9,7)				
T_{AVSH1}	A31:2 Valid to $\overline{ADS}$ Rising	T − 4	T + 4	ns	
T_{AVSH2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, D/$\overline{C}$, $\overline{DMA}$, $\overline{DACK3:0}$ Valid to $\overline{ADS}$ Rising	T − 6	T + 6	ns	
T_{AVEL1}	A31:2 Valid to $\overline{DEN}$ Falling	T − 4	T + 4	ns	
T_{AVEL2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, $\overline{INST}$, $\overline{DMA}$, $\overline{DACK3:0}$ Valid to $\overline{DEN}$ Falling	T − 6	T + 6	ns	
T_{NLQV}	$\overline{WAIT}$ Falling to Output Data Valid	±6		ns	
T_{DVNH}	Output Data Valid to $\overline{WAIT}$ Rising	N*T − 6	N*T + 6	ns	(4)
T_{NLNH}	$\overline{WAIT}$ Falling to $\overline{WAIT}$ Rising	N*T ± 4		ns	(4)
T_{NHQX}	Output Data Hold after $\overline{WAIT}$ Rising	(N + 1) * T − 6	(N + 1) * T + 6	ns	(5)
T_{EHTV}	DT/$\overline{R}$ Hold after $\overline{DEN}$ High	T/2 − 6	∞	ns	(6)
T_{TVEL}	DT/$\overline{R}$ Valid to $\overline{DEN}$ Falling	T/2 − 4	T/2 + 4	ns	(7)
	RELATIVE INPUT TIMINGS(7)				
T_{IS5}	$\overline{RESET}$ Input Setup (2x Clock Mode	8		ns	(14)
T_{IH5}	$\overline{RESET}$ Input Hold (2x Clock Mode)	7		ns	(14)
T_{IS6}	$\overline{DREQ3:0}$ Input Setup	14		ns	(8)
T_{IH6}	$\overline{DREQ3:0}$ Input Hold	9		ns	(8)
T_{IS7}	$\overline{XINT7:0}$, $\overline{NMI}$ Input Setup	9		ns	(8)
T_{IH7}	$\overline{XINT7:0}$, $\overline{NMI}$ Input Hold	5		ns	(8)
T_{IS8}	$\overline{RESET}$ Input Setup (1x Clock Mode)	3		ns	(15)
T_{IH8}	$\overline{RESET}$ Input Hold (1x Clock Mode)	T/4 + 1		ns	(15)

NOTES:
(1) See **Section 4.5.2, AC Timing Waveforms** for waveforms and definitions.
(2) See Figure 22 for capacitive derating information for output delays and hold times.
(3) See Figure 23 for capacitive derating information for rise and fall times.
(4) Where N is the number of N_{RAD}, N_{RDD}, N_{WAD}, or N_{WDD} wait states that are programmed in the Bus Controller Region Table. When there are no wait states in an access, $\overline{WAIT}$ never goes active.
(5) N = Number of wait states inserted with $\overline{READY}$.
(6) Output Data and/or DT/$\overline{R}$ may be driven indefinitely following a cycle if there is no subsequent bus activity.
(7) See Notes 1, 2 and 3.
(8) Since asynchronous inputs are synchronized internally by the 80960CF they have no required setup or hold times in order to be recognized and for proper operation. However, to guarantee recognition of the input at a particular edge of PCLK2:1 the setup times shown must be met. Asynchronous inputs must be active for at least two consecutive PCLK2:1 rising edges to be seen by the processor.
(9) These specifications are guaranteed by the processor.
(10) These specifications must be met by the system for proper operation of the processor.
(11) This timing is dependent upon the loading of PCLK2:1. Use the derating curves of **Section 4.5.3** to adjust the timing for PCLK2:1 loading.
(12) In the 1-x input clock mode, the maximum input clock period is limited to 125 ns while the processor is operating. When the processor is in reset, the input clock may stop even in 1-x mode.
(13) When in the 1-x input clock mode, these specifications assume a stable input clock with a period variation of less than ±0.1% between adjacent cycles.
(14) In 2x clock mode, $\overline{RESET}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{RESET}$ pin must meet setup and hold times to the falling edge of the CLKIN. (See Figure 28a.)
(15) In 1x clock mode, $\overline{RESET}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{RESET}$ pin must be deasserted while CLKIN is high and meet setup and hold times to the rising edge of the CLKIN. (See Figure 28b.)

AC Characteristics — 80960CF-16

(80960CF-16 only, under the conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions**.) (Continued)

Symbol	Parameter		Min	Max	Units	Notes
	INPUT CLOCK(10)					
T_F	CLKIN Frequency		0	32	MHz	(1)
T_C	CLKIN Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	62.5 31.25	125 ∞	ns ns	(1,12) (1)
T_{CS}	CLKIN Period Stability	In 1-x Mode (f_{CLK1x})		±0.1%	Δ	(1,13)
T_{CH}	CLKIN High Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	10 10	62.5 ∞	ns ns	(1,12) (1)
T_{CL}	CLKIN Low Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	10 10	62.5 ∞	ns ns	(1,12) (1)
T_{CR}	CLKIN Rise Time		0	6	ns	(1)
T_{CF}	CLKIN Fall Time		0	6	ns	(1)
	OUTPUT CLOCKS(9)					
T_{CP}	CLKIN to PCLK2:1 Delay	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	−2 2	2 25	ns ns	(1,3,13,14) (1,3)
T	PCLK2:1 Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	T_C $2T_C$		ns ns	(1,13) (1,3)
T_{PH}	PCLK2:1 High Time		(T/2) − 4	T/2	ns	(1,13)
T_{PL}	PCLK2:1 Low Time		(T/2) − 4	T/2	ns	(1,13)
T_{PR}	PCLK2:1 Rise Time		1	4	ns	(1,3)
T_{PF}	PCLK2:1 Fall Time		1	4	ns	(1,3)
	SYNCHRONOUS OUTPUTS(10)					
T_{OV} T_{OH}	Output Valid Delay, Output Hold					(6, 11)
	T_{OV1}, T_{OH1}	A31:2	3	18	ns	
	T_{OV2}, T_{OH2}	$\overline{BE3:0}$	3	20	ns	
	T_{OV3}, T_{OH3}	$\overline{ADS}$	6	22	ns	
	T_{OV4}, T_{OH4}	W/$\overline{R}$	3	22	ns	
	T_{OV5}, T_{OH5}	D/$\overline{C}$, $\overline{SUP}$, $\overline{DMA}$	4	20	ns	
	T_{OV6}, T_{OH6}	$\overline{BLAST}$, $\overline{WAIT}$	5	20	ns	
	T_{OV7}, T_{OH7}	$\overline{DEN}$	3	20	ns	
	T_{OV8}, T_{OH8}	HOLDA, BREQ	4	20	ns	
	T_{OV9}, T_{OH9}	$\overline{LOCK}$	4	20	ns	
	T_{OV10}, T_{OH10}	$\overline{DACK3:0}$	4	22	ns	
	T_{OV11}, T_{OH11}	D31:0	3	20	ns	
	T_{OV12}, T_{OH12}	DT/$\overline{R}$	T/2 + 3	T/2 + 18	ns	
	T_{OV13}, T_{OH13}	$\overline{FAIL}$	2	18	ns	
	T_{OV14}, T_{OH14}	$\overline{EOP3:0}$/$\overline{TC3:0}$	3	22	ns	(6, 11)
T_{OF}	Output Float for all outputs		3	22	ns	(6)
	SYNCHRONOUS INPUTS(10)					
T_{IS}	Input Setup					
	T_{IS1}	D31:0	5		ns	(1,11)
	T_{IS2}	$\overline{BOFF}$	21		ns	(1,11)
	T_{IS3}	$\overline{BTERM}$/$\overline{READY}$	9		ns	(1,11)
	T_{IS4}	HOLD	9		ns	(1,11)
T_{IH}	Input Hold					
	T_{IH1}	D31:0	5		ns	(1,11)
	T_{IH2}	$\overline{BOFF}$	7		ns	(1,11)
	T_{IH3}	$\overline{BTERM}$/$\overline{READY}$	2		ns	(1,11)
	T_{IH4}	HOLD	5		ns	(1,11)

AC Characteristics — 80960CF-16

(80960CF-16 only, under the conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions.**) (Continued)

Symbol	Parameter	Min	Max	Units	Notes
	RELATIVE OUTPUT TIMINGS(9,7)				
T_{AVSH1}	A31:2 Valid to $\overline{ADS}$ Rising	T − 4	T + 4	ns	
T_{AVSH2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, D/$\overline{C}$, $\overline{DMA}$, $\overline{DACK3:0}$ Valid to $\overline{ADS}$ Rising	T − 6	T + 6	ns	
T_{AVEL1}	A31:2 Valid to $\overline{DEN}$ Falling	T − 6	T + 6	ns	
T_{AVEL2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, $\overline{INST}$, $\overline{DMA}$, $\overline{DACK3:0}$ Valid to $\overline{DEN}$ Falling	T − 6	T + 6	ns	
T_{NLQV}	$\overline{WAIT}$ Falling to Output Data Valid	±6		ns	
T_{DVNH}	Output Data Valid to $\overline{WAIT}$ Rising	N*T − 6	N*T + 6	ns	(4)
T_{NLNH}	$\overline{WAIT}$ Falling to $\overline{WAIT}$ Rising	N*T ± 4		ns	(4)
T_{NHQX}	Output Data Hold after $\overline{WAIT}$ Rising	(N + 1) * T − 6	(N + 1) * T + 6	ns	(5)
T_{EHTV}	DT/$\overline{R}$ Hold after $\overline{DEN}$ High	T/2 − 6	∞	ns	(6)
T_{TVEL}	DT/$\overline{R}$ Valid to $\overline{DEN}$ Falling	T/2 − 4	T/2 + 4	ns	(7)
	RELATIVE INPUT TIMINGS(7)				
T_{IS5}	$\overline{RESET}$ Input Setup (2x Clock Mode)	10		ns	(14)
T_{IH5}	$\overline{RESET}$ Input Hold (2x Clock Mode)	9		ns	(14)
T_{IS6}	$\overline{DREQ3:0}$ Input Setup	16		ns	(8)
T_{IH6}	$\overline{DREQ3:0}$ Input Hold	11		ns	(8)
T_{IS7}	$\overline{XINT7:0}$, $\overline{NMI}$ Input Setup	9		ns	(8)
T_{IH7}	$\overline{XINT7:0}$, $\overline{NMI}$ Input Hold	5		ns	(8)
T_{IS8}	$\overline{RESET}$ Input Setup (1x Clock Mode)	3		ns	(15)
T_{IH8}	$\overline{RESET}$ Input Hold (1x Clock Mode)	T/4 + 1		ns	(15)

NOTES:
(1) See **Section 4.5.2, AC Timing Waveforms** for waveforms and definitions.
(2) See Figure 22 for capacitive derating information for output delays and hold times.
(3) See Figure 23 for capacitive derating information for rise and fall times.
(4) Where N is the number of N_{RAD}, N_{RDD}, N_{WAD}, or N_{WDD} wait states that are programmed in the Bus Controller Region Table. When there are no wait states in an access, $\overline{WAIT}$ never goes active.
(5) N = Number of wait state inserted with $\overline{READY}$.
(6) Output Data and/or DT/$\overline{R}$ may be driven indefinitely following a cycle if there is no subsequent bus activity.
(7) See Notes 1, 2 and 3.
(8) Since asynchronous inputs are synchronized internally by the 80960CF they have no required setup or hold times in order to be recognized and for proper operation. However, to guarantee recognition of the input at a particular edge of PCLK2:1 the setup times shown must be met. Asynchronous inputs must be active for at least two consecutive PCLK2:1 rising edges to be seen by the processor.
(9) These specifications are guaranteed by the processor.
(10) These specifications must be met by the system for proper operation of the processor.
(11) This timing is dependent upon the loading of PCLK2:1. Use the derating curves of Figure 22 to adjust the timing for PCLK2:1 loading.
(12) In the 1-x input clock mode, the maximum input clock period is limited to 125 ns while the processor is operating. When the processor is in reset, the input clock may stop even in 1-x mode.
(13) When in the 1-x input clock mode, these specifications assume a stable input clock with a period variation of less than ±0.1% between adjacent cycles.
(14) In 2x clock mode, $\overline{RESET}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{RESET}$ pin must meet setup and hold times to the falling edge of the CLKIN. (See Figure 28a.)
(15) In 1x clock mode, $\overline{RESET}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{RESET}$ pin must be deasserted while CLKIN is high and meet setup and hold times to the rising edge of the CLKIN. (See Figure 28b.)

4.5.1. AC TEST CONDITIONS

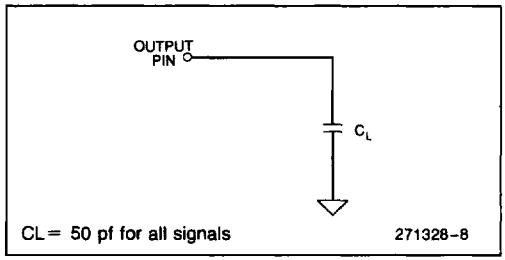

Figure 9. AC Test Load

The AC Specifications in Section 4.5 are tested with the 50 pf load shown in Figure 9. See Figure 16 to see how timings vary with load capacitance.

Specifications are measured at the 1.5V crossing point, unless otherwise indicated. Input waveforms are assumed to have a rise-and-fall time of ≤ 2 ns from 0.8V to 2.0V. See **Section 4.5.2, AC Timing Waveforms** for AC spec definitions, test points and illustrations.

4.5.2. AC TIMING WAVEFORMS

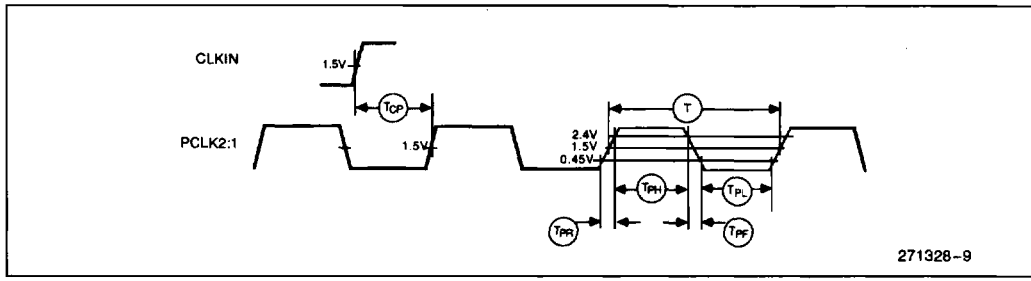

Figure 10a. Input and Output Clocks Waveform

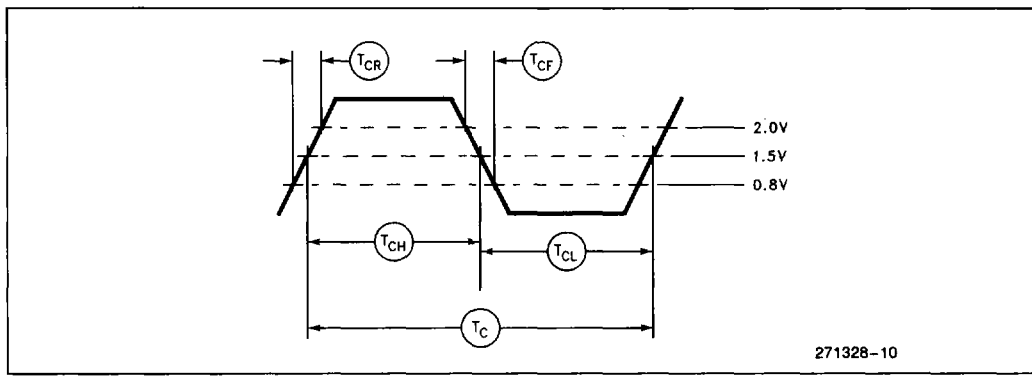

Figure 10b. CLKIN Waveform

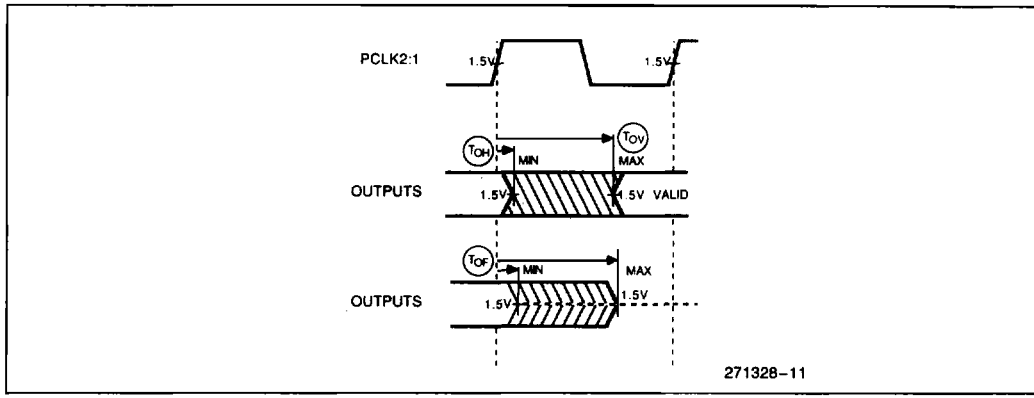

Figure 11. Output Delay and Float Waveform

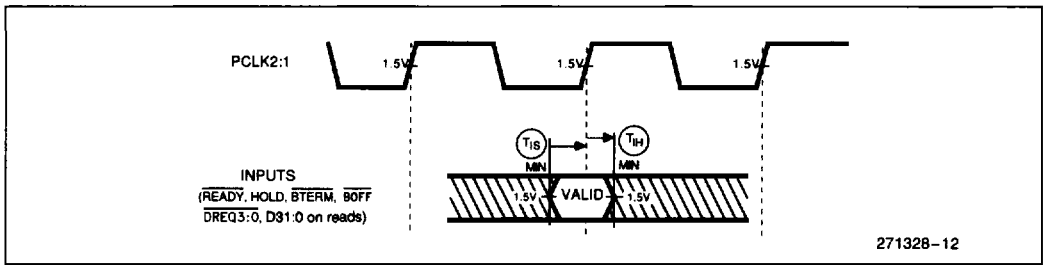

Figure 12a. Input Setup and Hold Waveform

(T_{OV}) (T_{OH}) — OUTPUT DELAY — The maximum output delay is referred to as the Output Valid Delay (T_{OV}). The minimum output delay is referred to as the Output Hold (T_{OH}).

(T_{OF}) — OUTPUT FLOAT DELAY — The output float condition occurs when the maximum output current becomes less than I_{LO} in magnitude.

(T_{IS}) (T_{IH}) — INPUT SETUP AND HOLD — The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

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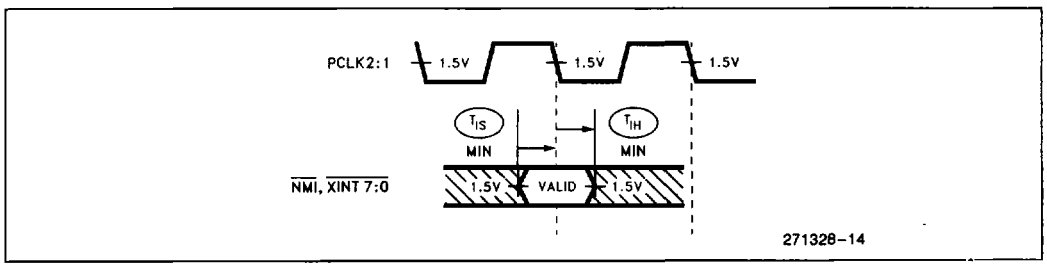
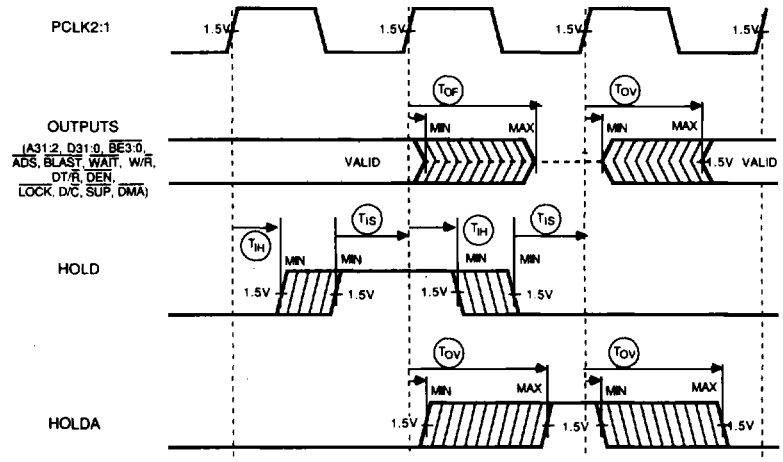


Figure 12b. NMI, XINT7:0 Input Setup and Hold Waveform



T_{OV} T_{OH} — OUTPUT DELAY — The maximum output delay is referred to as the Output Valid Delay (T_{OV}). The minimum output delay is referred to as the Output Hold (T_{OH}).

T_{OF} — OUTPUT FLOAT DELAY — The output float condition occurs when the maximum output current becomes less than I_{LO} in magnitude.

T_{IS} T_{IH} — INPUT SETUP AND HOLD — The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

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Figure 13. Hold Acknowledge Timings

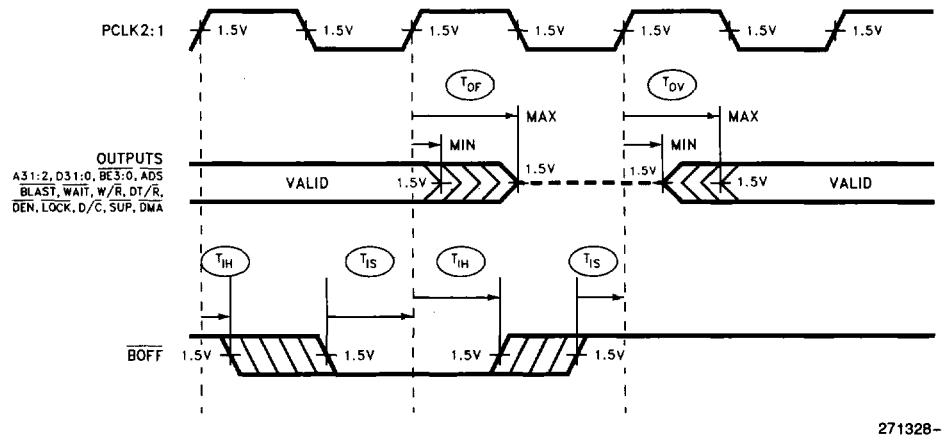

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Figure 14. Bus Back-Off ($\overline{BOFF}$) Timings

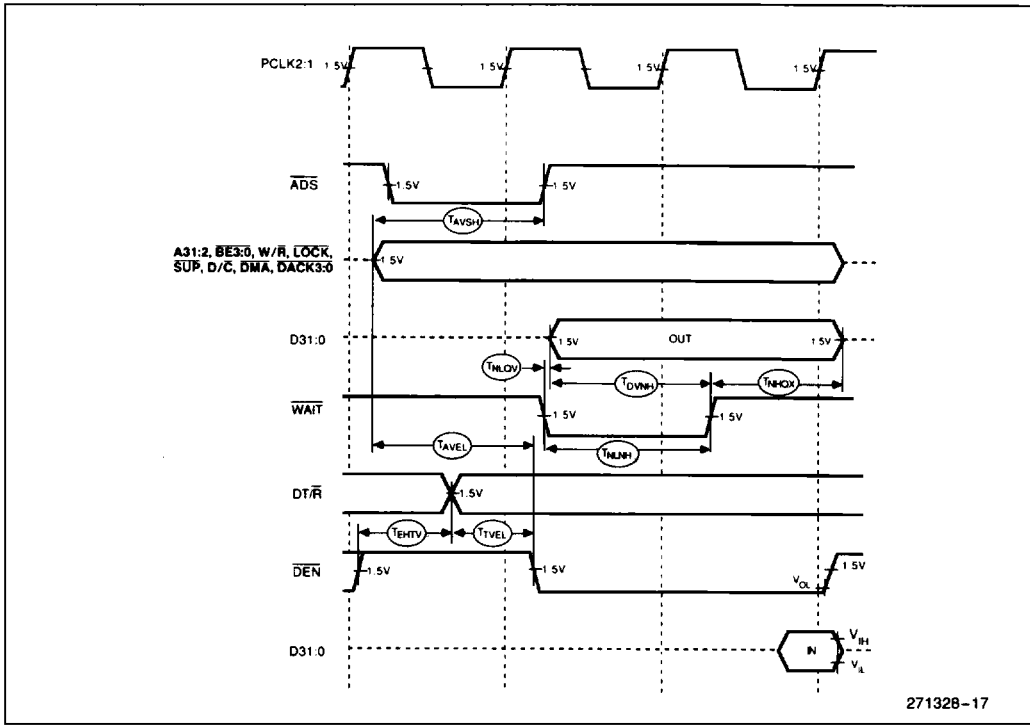
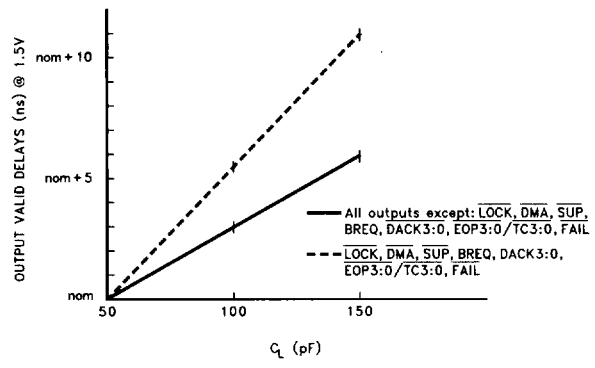


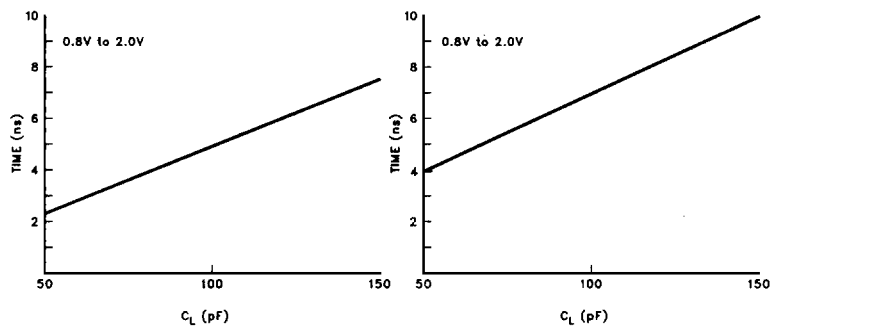
Figure 15. Relative Timings Waveforms

4.5.3 DERATING CURVES



NOTE:
PCLK Load = 50 pF

Figure 16. Output Delay or Hold vs Load Capacitance

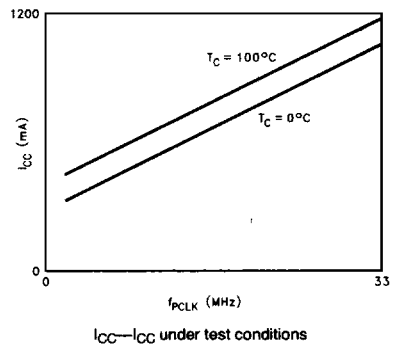


(a) All outputs except: $\overline{LOCK}$, $\overline{DMA}$, $\overline{SUP}$, HOLDA, BREQ, $\overline{DACK3:0}$, $\overline{EOP3:0}$/$\overline{TC3:0}$, $\overline{FAIL}$

(b) $\overline{LOCK}$, $\overline{DMA}$, $\overline{SUP}$, HOLDA, BREQ, $\overline{DACK3:0}$, $\overline{EOP3:0}$/$\overline{TC3:0}$, $\overline{FAIL}$

271328-19

Figure 17. Rise and Fall Time Derating at Highest Operating Temperature and Minimum V_{CC}



271328-20

I_{CC}—I_{CC} under test conditions

Figure 18. I_{CC} vs Frequency and Temperature