CY7C1166V18, CY7C1177V18
CY7C1168V18, CY7C1170V18

18-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)

Features

- 18 Mbit density (2M x 8, 2M x 9, 1M x 18, 512K x 36)
- 300 MHz to 400 MHz clock for high bandwidth
- 2-Word burst for reducing address bus frequency
- Double Data Rate (DDR) interfaces (data transferred at 800 MHz) at 400 MHz
- Read latency of 2.5 clock cycles
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high-speed systems
- Data valid pin (QVLD) to indicate valid data on the output
- Synchronous internally self-timed writes
- Core V_{DD} = 1.8V ± 0.1V; IO V_{DDQ} = 1.4V to V_{DD}[1]
- HSTL inputs and Variable drive HSTL output buffers
- Available in 165-Ball FBGA package (13 x 15 x 1.4 mm)
- Offered in both Pb-free and non Pb-free packages
- JTAG 1149.1-compatible test access port
- Delay Lock Loop (DLL) for accurate data placement

Configurations

With Read Cycle Latency of 2.5 cycles:

CY7C1166V18 – 2M x 8

CY7C1177V18 – 2M x 9

CY7C1168V18 – 1M x 18

CY7C1170V18 – 512K x 36

Functional Description

The CY7C1166V18, CY7C1177V18, CY7C1168V18, and CY7C1170V18 are 1.8V Synchronous Pipelined SRAMs equipped with DDR-II+ architecture. The DDR-II+ consists of an SRAM core with an advanced synchronous peripheral circuitry. Addresses for read and write are latched on alternate rising edges of the input (K) clock. Write data is registered on the rising edges of both K and $\overline{K}$. Read data is driven on the rising edges of K and $\overline{K}$. Each address location is associated with two 8-bit words (CY7C1166V18), or 9-bit words (CY7C1177V18), or 18-bit words (CY7C1168V18), or 36-bit words (CY7C1170V18) that burst sequentially into or out of the device.

Asynchronous inputs include output impedance matching input (ZQ). Synchronous data outputs (Q, sharing the same physical pins as the data inputs D) are tightly matched to the two output echo clocks CQ/$\overline{CQ}$, eliminating the need for separately capturing data from each individual DDR SRAM in the system design.

All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the K or $\overline{K}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

Selection Guide

Description	400 MHz	375 MHz	333 MHz	300 MHz	Unit
Maximum Operating Frequency	400	375	333	300	MHz
Maximum Operating Current	1080	1020	920	850	mA

Note

1. The QDR consortium specification for V_{DDQ} is 1.5V ± 0.1V. The Cypress QDR devices exceed the QDR consortium specification and are capable of supporting V_{DDQ} = 1.4V to V_{DD}.

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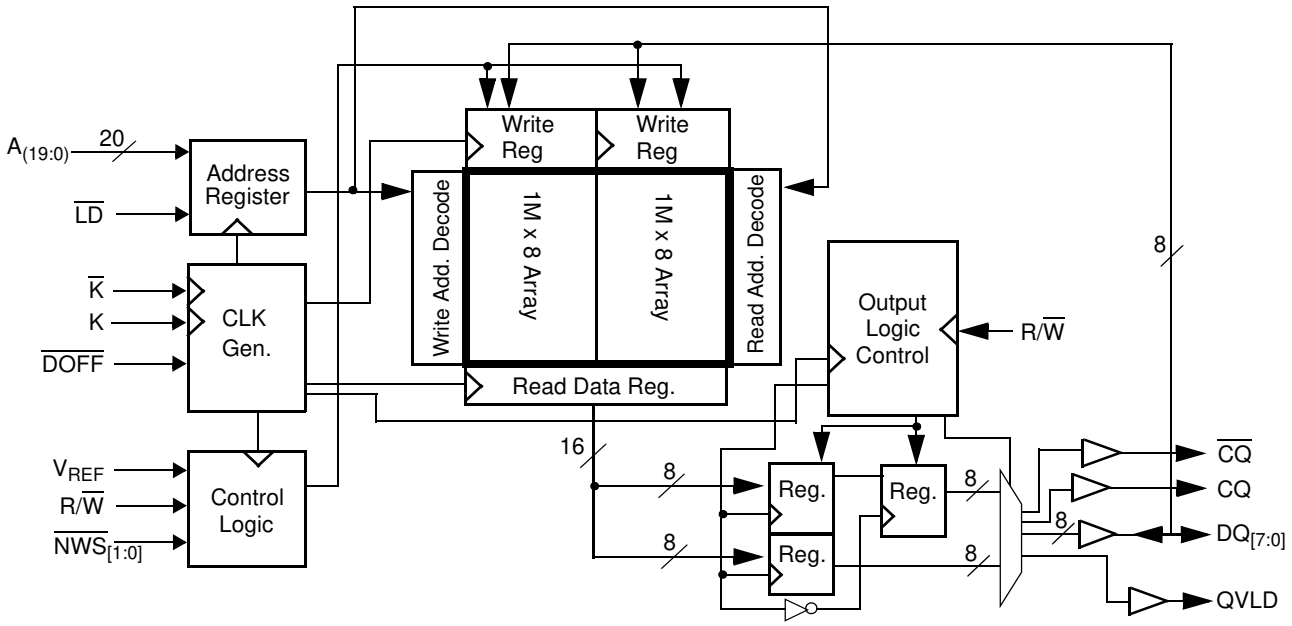
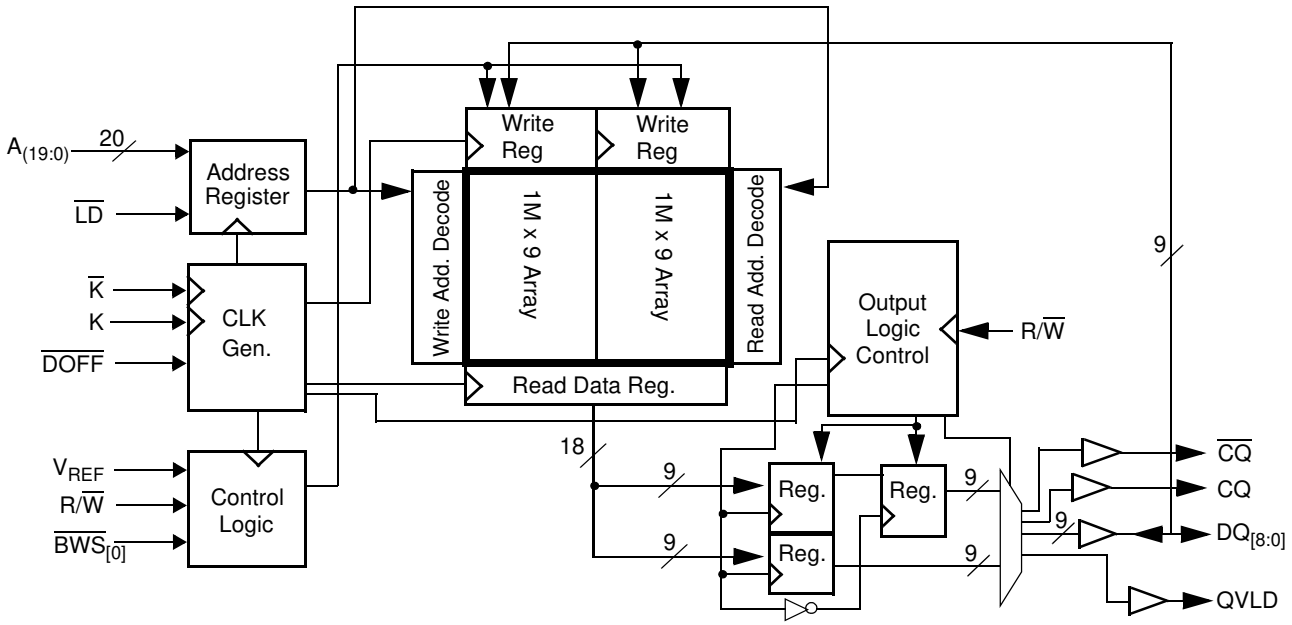
Logic Block Diagram (CY7C1166V18)



Logic Block Diagram (CY7C1177V18)



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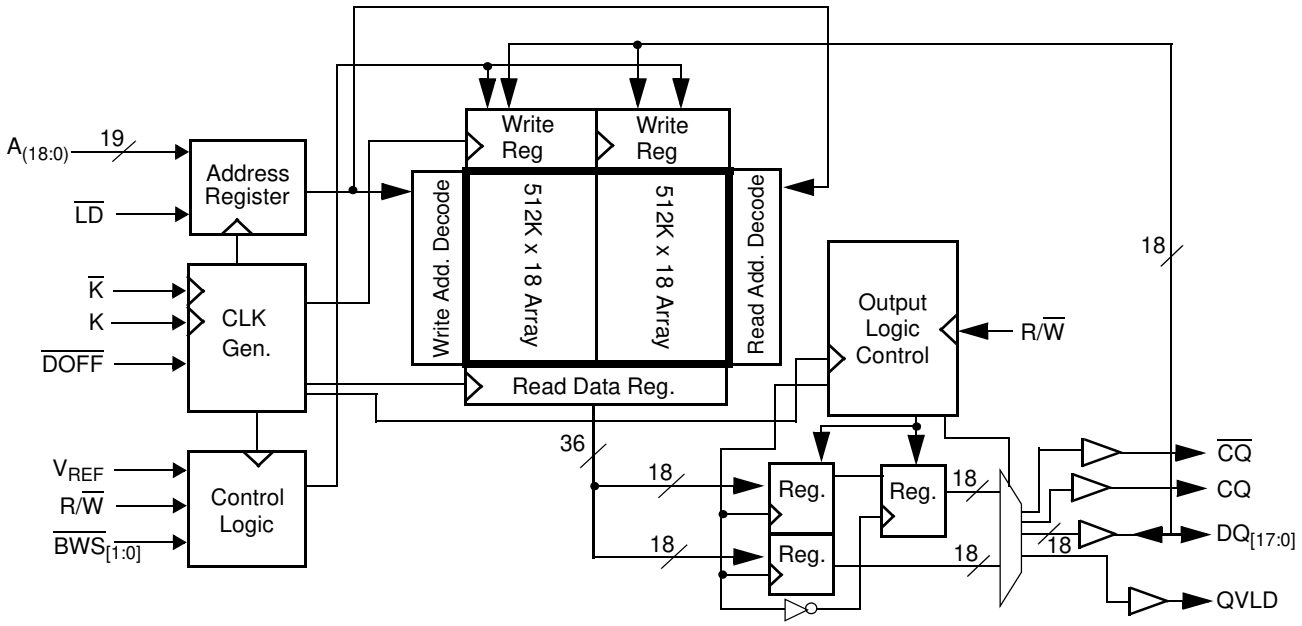
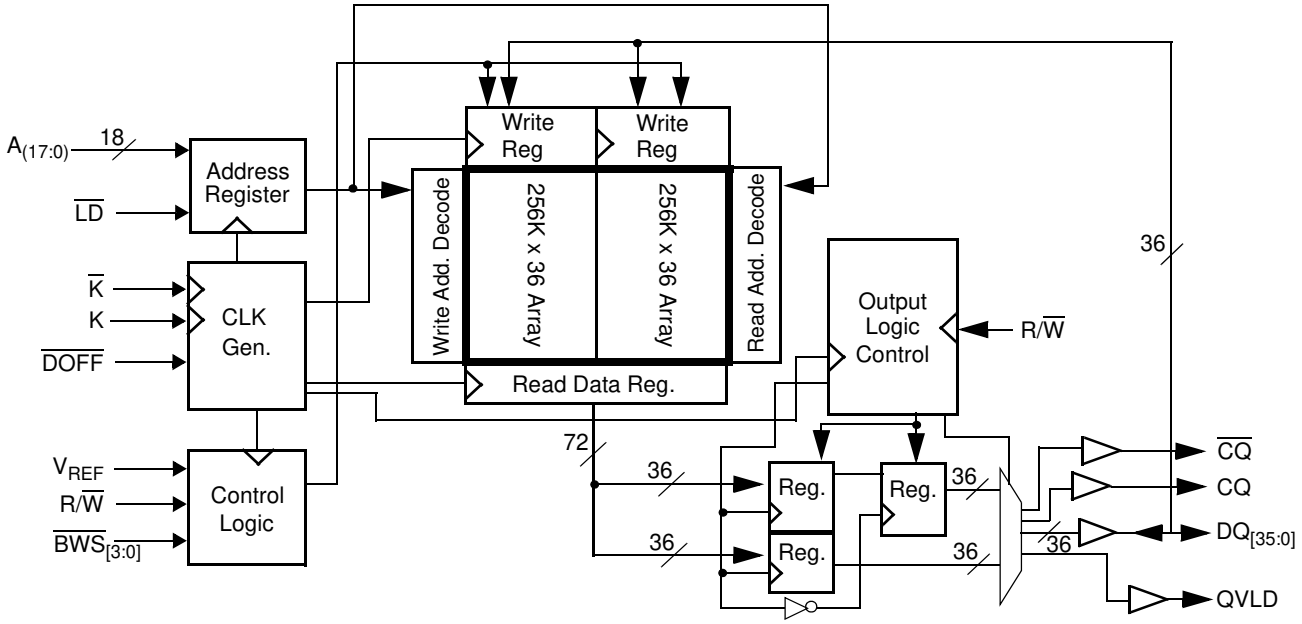
Logic Block Diagram (CY7C1168V18)



Logic Block Diagram (CY7C1170V18)



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Pin Configurations

165-Ball FBGA (13 x 15 x 1.4 mm) Pinout

CY7C1166V18 (2M x 8)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	R/$\overline{W}$	$\overline{NWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	NC/36M	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{NWS_0}$	A	NC	NC	DQ3
C	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ7	A	A	QVLD	A	A	NC	NC	NC
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

CY7C1177V18 (2M x 9)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	R/$\overline{W}$	NC	$\overline{K}$	NC/144M	$\overline{LD}$	A	NC/36M	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ3
C	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ7	A	A	QVLD	A	A	NC	NC	DQ8
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

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Pin Configurations (continued)

165-Ball FBGA (13 x 15 x 1.4 mm) Pinout

CY7C1168V18 (1M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	R/$\overline{W}$	$\overline{BWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	NC/36M	CQ
B	NC	DQ9	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	A	NC	A	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	A	A	QVLD	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

CY7C1170V18 (512K x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	NC/36M	R/$\overline{W}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{LD}$	A	NC/72M	CQ
B	NC	DQ27	DQ18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	A	NC	A	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	A	A	A	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	A	A	QVLD	A	A	NC	DQ9	DQ0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

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Pin Definitions

Pin Name	IO	Pin Description
$DQ_{[x:0]}$	Input Output-Synchronous	**Data Input Output Signals**. Inputs are sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. These pins drive out the requested data when a read operation is active. Valid data is driven out on the rising edge of both the K and K clocks during read operations. When read access is deselected, Q[x:0] are automatically tri-stated. CY7C1166V18 – $DQ_{[7:0]}$ CY7C1177V18 – $DQ_{[8:0]}$ CY7C1168V18 – $DQ_{[17:0]}$ CY7C1170V18 – $DQ_{[35:0]}$
$\overline{LD}$	Input-Synchronous	**Synchronous Load.** This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst of two data. $\overline{LD}$ must meet the setup and hold times around edge of K. $\overline{LD}$ must meet the setup and hold times around edge of K.
$\overline{NWS}_0$, $\overline{NWS}_1$,	Input-Synchronous	**Nibble Write Select 0, 1** – **Active LOW**.(**CY7C1166V18 Only**) Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. It is used to select the nibble that is written into the device $\overline{NWS}_0$ controls $D_{[3:0]}$ and $\overline{NWS}_1$ controls $D_{[7:4]}$. All the Nibble Write Selects are sampled on the same edge as the data. Deselecting a Nibble Write Select ignores the corresponding nibble of data and not written into the device.
$\overline{BWS}_0$, $\overline{BWS}_1$, $\overline{BWS}_2$, $\overline{BWS}_3$	Input-Synchronous	**Byte Write Select 0, 1, 2, and 3** – **Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during Write operations. It is used to select the byte that is written into the device during the current portion of the write operations. Bytes not written remain unaltered. CY7C1177V18 – $\overline{BWS}_0$ controls $D_{[8:0]}$ CY7C1168V18 – $\overline{BWS}_0$ controls $D_{[8:0]}$, and $\overline{BWS}_1$ controls $D_{[17:9]}$ CY7C1170V18 – $\overline{BWS}_0$ controls $D_{[8:0]}$, $\overline{BWS}_1$ controls $D_{[17:9]}$, $\overline{BWS}_2$ controls $D_{[26:18]}$, and $\overline{BWS}_3$ controls $D_{[35:27]}$. All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and not written into the device.
A	Input-Synchronous	**Address Inputs**. Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 2M x 8 (two arrays each of1M x 8) for CY7C1166V18, 2M x 9 (two arrays each of 1M x 9) for CY7C1177V18, 1M x 18 (two arrays each of 512K x 18) for CY7C1168V18, and 512K x 36 (two arrays each of 256K x 18) for CY7C1170V18. All the address inputs are ignored when the appropriate port is deselected.
R/$\overline{W}$	Input-Synchronous	**Synchronous Read/Write Input**. When $\overline{LD}$ is LOW, this input designates the access type (read when R/$\overline{W}$ is HIGH, write when R/$\overline{W}$ is LOW) for loaded address. R/$\overline{W}$ must meet the setup and hold times around edge of K.
QVLD	Valid Output Indicator	**Valid Output Indicator**. The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\overline{CQ}$.
K	Input-Clock	**Positive Input Clock Input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input-Clock	**Negative Input Clock Input**. $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode.
CQ	Clock Output	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock (K) of the DDR-II+. The timings for the echo clocks are shown in the "Switching Characteristics" on page 22.
$\overline{CQ}$	Clock Output	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock ($\overline{K}$) of the DDR-II+. The timings for the echo clocks are shown in the "Switching Characteristics" on page 22.

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Pin Definitions (continued)

Pin Name	IO	Pin Description
ZQ	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	**DLL Turn Off – Active LOW**. Connecting this pin to ground turns off the DLL inside the device. The timings in the DLL turned off operation is different from those listed in this data sheet. For normal operation, this pin can be connected to a pull up through a 10KΩ or less pull up resistor. The device behaves in DDR-I mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with DDR-I timing.
TDO	Output	**TDO for JTAG**.
TCK	Input	**TCK Pin for JTAG**.
TDI	Input	**TDI Pin for JTAG**.
TMS	Input	**TMS Pin for JTAG**.
NC	N/A	**Not Connected to the Die**. Tie to any voltage level.
NC/36M	N/A	**Not Connected to the Die**. Tie to any voltage level.
NC/72M	N/A	**Not Connected to the Die**. Tie to any voltage level.
NC/144M	N/A	**Not Connected to the Die**. Tie to any voltage level.
NC/288M	N/A	**Not Connected to the Die**. Tie to any voltage level.
V_{REF}	Input-Reference	**Reference Voltage Input**. Static input used to set the reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{SS}	Ground	**Ground for the Device**.
V_{DDQ}	Power Supply	**Power Supply Inputs for the Outputs of the Device**.

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Functional Overview

The CY7C1166V18, CY7C1177V18, CY7C1168V18, and CY7C1170V18 are synchronous pipelined Burst SRAMs equipped with a DDR interface.

Accesses are initiated on the rising edge of the positive input clock (K). All synchronous input and output timing are referenced to the rising edge of the Input clocks (K/$\overline{K}$).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the input clocks (K and $\overline{K}$) also.

All synchronous control (R/$\overline{W}$, $\overline{LD}$, $\overline{BWS}_{[0:X]}$) inputs pass through input registers controlled by the rising edge of the input clock (K/$\overline{K}$).

CY7C1168V18 is described in the following sections. The same basic descriptions apply to CY7C1166V18, CY7C1177V18, and CY7C1170V18.

Read Operations

The CY7C1168V18 is organized internally as a single array of 1M x 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting R/$\overline{W}$ HIGH and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the read address register. Following the next two K clock rise, the corresponding 18-bit word of data from this address location is driven onto the $Q_{[17:0]}$ using $\overline{K}$ as the output timing reference. On the subsequent rising edge of K the next 18-bit data word from the address location generated by the burst counter is driven onto the $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the input clock (K/$\overline{K}$). In order to maintain the internal logic, each read access must be allowed to complete. Read accesses can be initiated on every rising edge of the positive input clock (K).

When read access is deselected, the CY7C1168V18 first completes the pending read transactions. Synchronous internal circuitry automatically tri-states the outputs following the next rising edge of the negative Input clock ($\overline{K}$). This enables for a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting R/$\overline{W}$ LOW and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the write address register. On the following K clock rise the data presented to $D_{[17:0]}$ is latched and stored into the 18-bit Write Data register provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the Negative Input Clock ($\overline{K}$) the information presented to $D_{[17:0]}$ is also stored into the Write Data register provided $\overline{BWS}_{[1:0]}$ are both asserted active. The 36 bits of data is then written into the memory array at the specified location. Write accesses can be initiated on every rising edge of the positive input clock (K). This pipelines the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When write access is deselected, the device ignores all inputs after the pending write operations are completed.

Byte Write Operations

Byte Write operations are supported by the CY7C1168V18. A Write operation is initiated as described in the Write Operations section. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$ which are sampled with each set of 18-bit data word. Asserting the appropriate Byte Write Select input during the data portion of a write enables the data being presented to be latched and written into the device. Deasserting the Byte Write Select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature can be used to simplify read/modify/write operations to a Byte Write operation.

Double Data Rate Operation

The CY7C1168V18 enables high-performance operation through high clock frequencies (achieved through pipelining) and double data rate mode of operation. The CY7C1168V18 requires two No Operation (NOP) cycle when transitioning from a read to a write cycle. At higher frequencies, some applications may require a third NOP cycle to avoid contention.

If a read occurs after a write cycle, then the address and data for the write are stored in registers. The write information must be stored because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next write cycle occurs. On the first write cycle after the read(s), the stored data from the earlier write is written into the SRAM array. This is called a Posted Write.

If a read is performed on the same address on which a write is performed in the previous cycle, the SRAM reads out the most current data. The SRAM does this by bypassing the memory array and reading the data from the registers.

Depth Expansion

Depth expansion requires replicating the $\overline{LD}$ control signal for each bank. All other control signals can be common between banks as appropriate.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175Ω and 350Ω, with V_{DDQ} = 1.5V. The output impedance is adjusted every 1024 cycles upon power up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the DDR-II+ to simplify data capture on high-speed systems. Two echo clocks are generated by the DDR-II+. CQ is referenced with respect to K and $\overline{CQ}$ is referenced with respect to $\overline{K}$. These are free-running clocks and are synchronized to the input clock of the DDR-II+. The timings for the echo clocks are shown in the "Switching Characteristics" on page 22.

Valid Data Indicator (QVLD)

QVLD is provided on the DDR-II+ to simplify data capture on high speed systems. The QVLD is generated by the DDR-II+ device along with data output. This signal is also edge-aligned with the

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echo clock and follows the timing of any data pin. This signal is asserted half a cycle before valid data arrives.

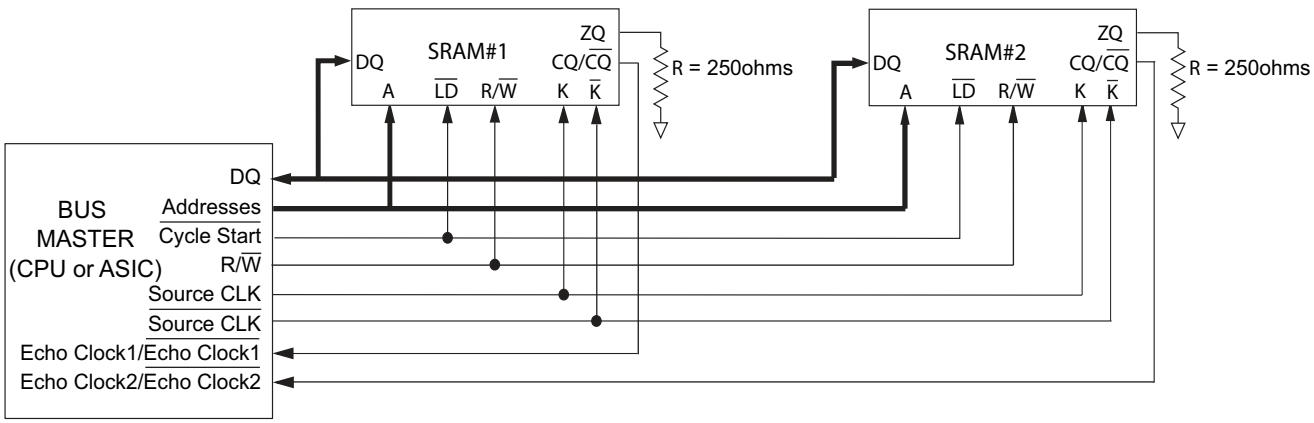
DLL

These chips use a Delay Lock Loop (DLL) that is designed to function between 120 MHz and the specified maximum clock frequency. The DLL may be disabled by applying ground to the $\overline{DOFF}$ pin. When the DLL is turned off, the device behaves in DDR-I mode (with 1.0 cycle latency and a longer access time). For more information, refer to the application note, "DLL Considerations in QDRII/DDRII/QDRII+/DDRII+". The DLL can also be reset by slowing or stopping the input clocks K and $\overline{K}$ for a minimum of 30 ns. However, it is not necessary for the DLL to be reset to lock to the desired frequency. During power up, when the $\overline{DOFF}$ is tied HIGH, the DLL gets locked after 2048 cycles of stable clock.

Application Example

Figure 1 shows two DDR-II+ used in an application.

Figure 1. Application Example



Truth Table

The truth table for the CY7C1166V18, CY7C1177V18, CY7C1168V18, and CY7C1170V18 follows. [2, 3, 4, 5, 6, 7]

Operation	K	$\overline{LD}$	R/$\overline{W}$	DQ	DQ
Write Cycle: Load address; wait one cycle; input write data on consecutive K and $\overline{K}$ rising edges.	L-H	L	L	D(A) at K (t + 1) ↑	D(A + 1) at $\overline{K}$ (t + 1) ↑
Read Cycle: (2.5 Cycle Latency) Load address; wait two and a half cycle; read data on consecutive $\overline{K}$ and K rising edges.	L-H	L	H	Q(A) at $\overline{K}$ (t + 2)↑	Q(A + 1) at K (t + 3) ↑
NOP: No Operation	L-H	H	X	High-Z	High-Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State

Notes

2. X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
3. Device powers up deselected and the outputs in a tri-state condition.
4. "A" represents address location latched by the devices when transaction was initiated and A + 1 represents the addresses sequence in the burst.
5. "t" represents the cycle at which a Read/Write operation is started. t + 1, t + 2, and t + 3 are the first, second, and third clock cycles succeeding the "t" clock cycle.
6. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges.
7. Do K = $\overline{K}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.

[+] Feedback

Write Cycle Descriptions

The write cycle descriptions of CY7C1166V18 and CY7C1168V18 follows. [2, 8]

$\overline{BWS_0}$/ $\overline{NWS_0}$	$\overline{BWS_1}$/ $\overline{NWS_1}$	K	$\overline{K}$	Comments
L	L	L–H	–	During the Data portion of a write sequence: CY7C1166V18 – both nibbles ($D_{[7:0]}$) are written into the device. CY7C1168V18 – both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L-H	During the Data portion of a write sequence: CY7C1166V18 – both nibbles ($D_{[7:0]}$) are written into the device. CY7C1168V18 – both bytes ($D_{[17:0]}$) are written into the device.
L	H	L–H	–	During the Data portion of a write sequence: CY7C1166V18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C1168V18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the Data portion of a write sequence: CY7C1166V18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C1168V18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the Data portion of a write sequence: CY7C1166V18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C1168V18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the Data portion of a write sequence: CY7C1166V18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C1168V18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

The write cycle descriptions of CY7C1177V18 follows. [2, 8]

$\overline{BWS_0}$	K	$\overline{K}$	Comments
L	L-H	–	During the Data portion of a Write sequence, the single byte ($D_{[8:0]}$) is written into the device.
L	–	L-H	During the Data portion of a Write sequence, the single byte ($D_{[8:0]}$) is written into the device.
H	L-H	–	No data is written into the device during this portion of a Write operation.
H	–	L-H	No data is written into the device during this portion of a Write operation.

Note

8. Is based on a write cycle was initiated in accordance with the Write Cycle Description Truth Table. Alter $\overline{NWS_0}$, $\overline{NWS_1}$, $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ on different portions of a write cycle, as long as the setup and hold requirements are achieved.

[+] Feedback

The write cycle descriptions of CY7C1170V18 follows. [2, 8]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L-H	–	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L-H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L-H	–	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L-H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L-H	–	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	–	L-H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L-H	–	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	–	L-H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L-H	–	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L-H	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L-H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L-H	No data is written into the device during this portion of a write operation.

[+] Feedback

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8V IO logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state which does not interfere with the operation of the device.

Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and connect to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For more information about loading the instruction register, see "TAP Controller State Diagram" on page 14. TDI is internally pulled up and unconnected if the TAP is not used in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see "Instruction Codes" on page 17). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSb) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and enable data to be scanned into and out of the SRAM test circuitry. Select only one register at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Load three-bit instructions serially into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in "TAP Controller Block Diagram" on page 15. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture IR state, the two least significant bits are loaded with a binary "01" pattern to allow fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. Use the EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions to capture the contents of the input and output ring.

The "Boundary Scan Order" on page 18 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSb of the register is connected to TDI, and the LSb is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the "Identification Register Definitions" on page 17.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the "Instruction Codes" on page 17. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

[+] Feedback

IDCODE

The IDCODE instruction causes a vendor-specific 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is supplied a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is supplied during the Update IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

EXTEST Output Bus Tri-State

IEEE Standard 1149.1 mandates that the TAP controller is able to put the output bus into a tri-state mode.

The boundary scan register has a special bit located at bit #47. When this scan cell, called the “extest output bus tri-state”, is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High-Z condition.

Set this bit by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

Reserved

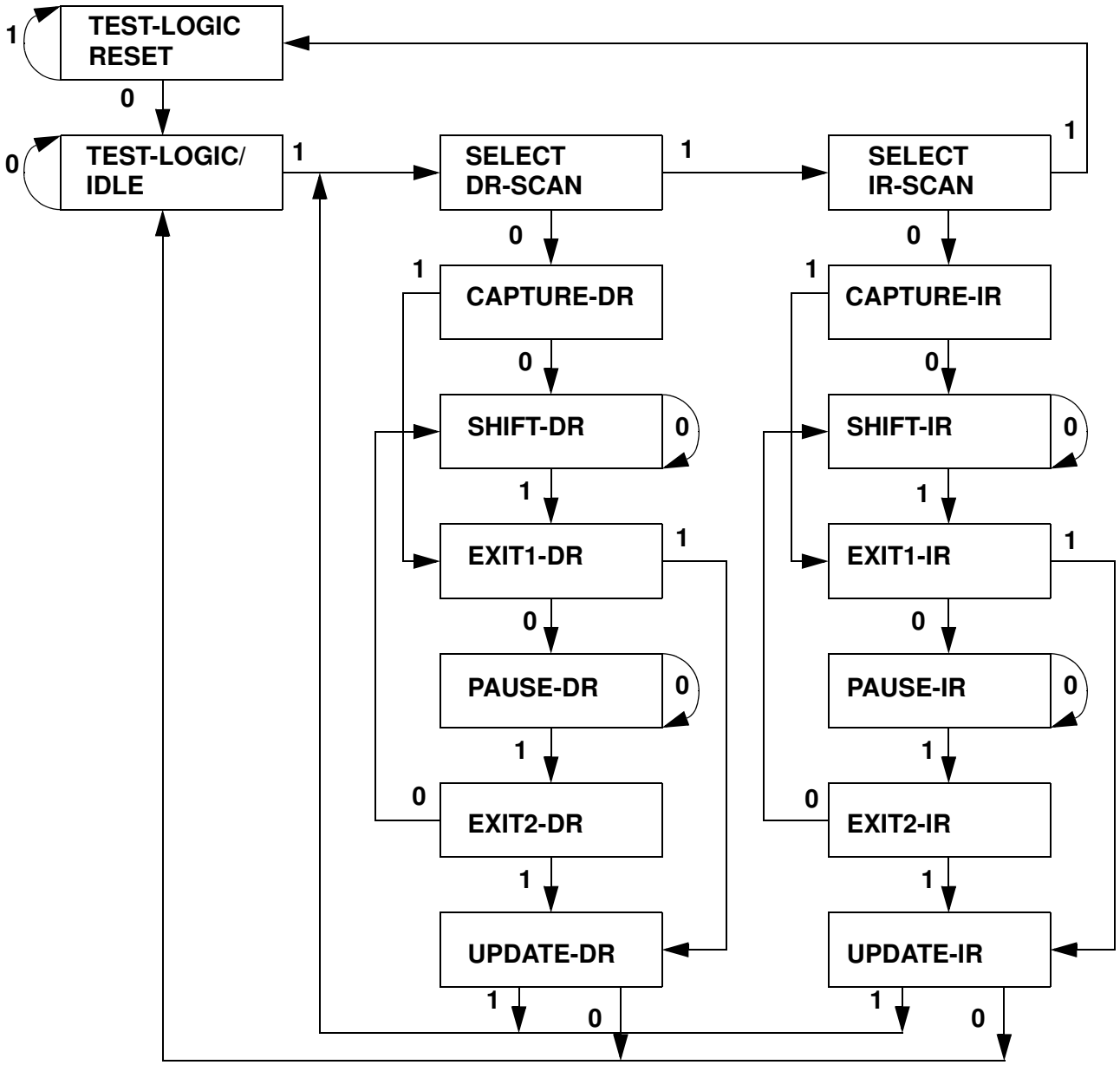
These instructions are not implemented but are reserved for future use. Do not use these instructions.

[+] Feedback

TAP Controller State Diagram

Figure 2 shows the tap controller state diagram. [9]

Figure 2. Tap Controller State Diagram

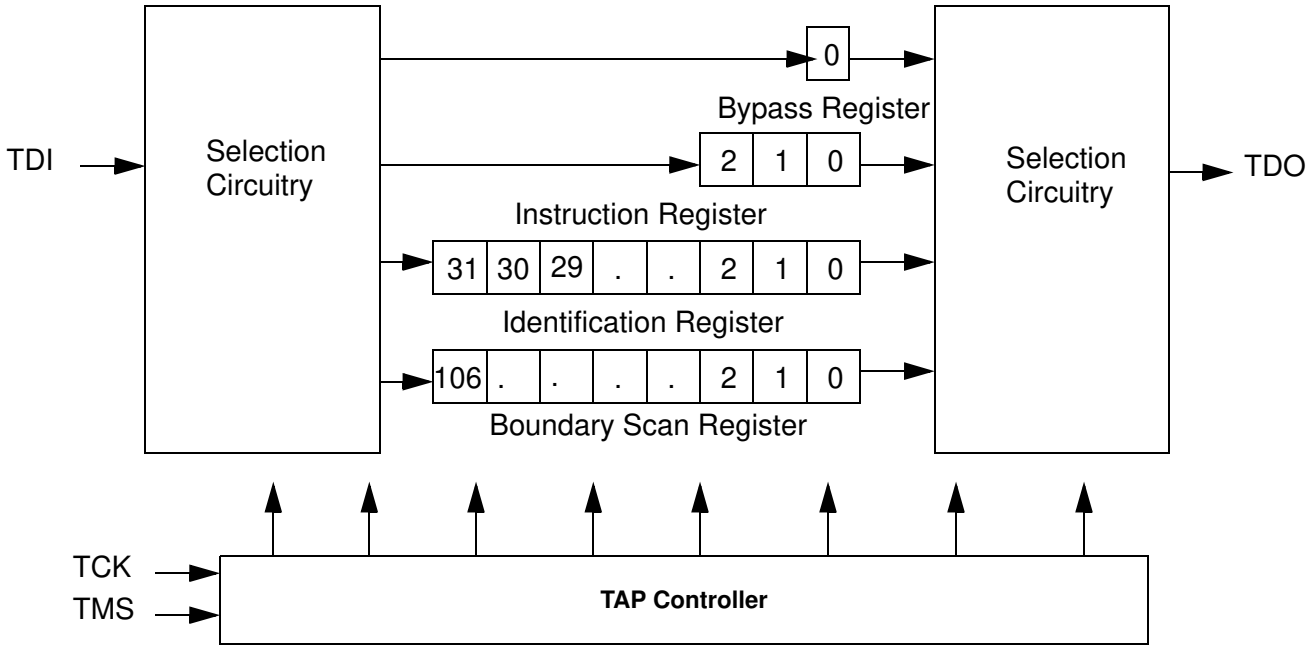


Note
9. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

[+] Feedback

TAP Controller Block Diagram

Figure 3. Tap Controller Block Diagram



TAP Electrical Characteristics

The Tap Electrical Characteristics table over the operating range follows.[10, 11, 12]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –2.0 mA	1.4		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	1.6		V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage		0.65 V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.35 V_{DD}	V
I_X	Input and Output Load Current	GND ≤ V_I ≤ V_{DD}	–5	5	µA

Notes
10. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics Table.
11. Overshoot: $V_{IH}(AC) \leq V_{DDQ} + 0.35V$ (pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) \geq -0.3V$ (pulse width less than $t_{CYC}/2$).
12. All voltage refer to ground.

[+] Feedback

TAP AC Switching Characteristics

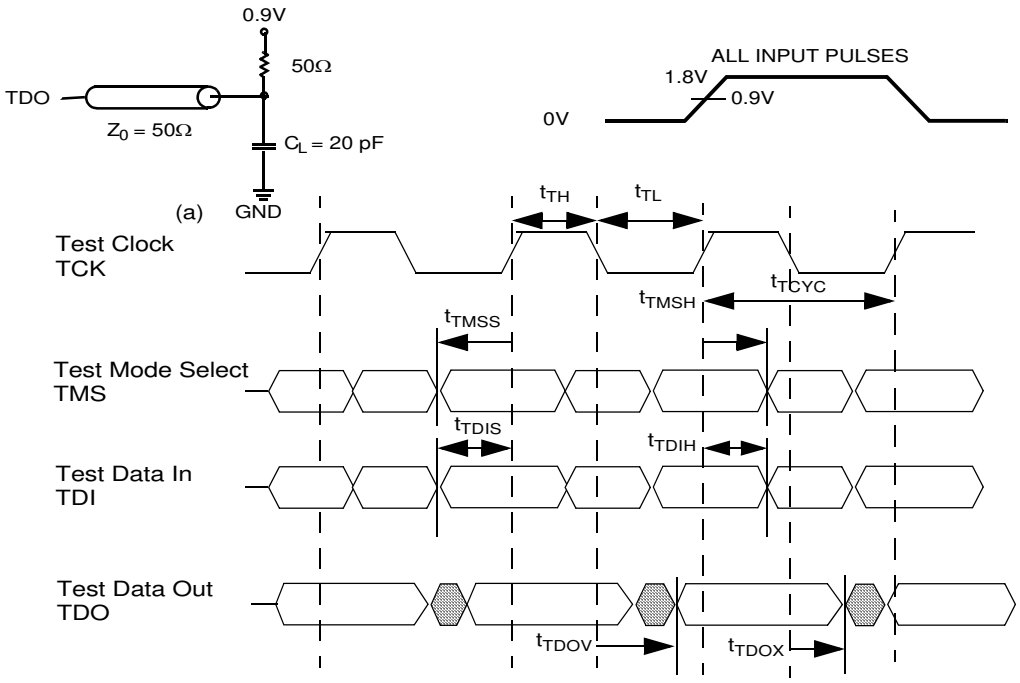
The Tap AC Switching Characteristics over the operating range follows.[13, 14]

Parameter	Description	Min	Max	Unit
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH	20		ns
t_{TL}	TCK Clock LOW	20		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

TAP Timing and Test Condition

The Tap Timing and Test Conditions for the CY7C1166V18, CY7C1177V18, CY7C1168V18, and CY7C1170V18 follows.[14]

Figure 4. TAP Timing and Test Conditions



Notes
13. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
14. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns

[+] Feedback

Identification Register Definitions

Instruction Field	Value				Description
	CY7C1166V18	CY7C1177V18	CY7C1168V18	CY7C1170V18	
Revision Number (31:29)	000	000	000	000	Version number.
Cypress Device ID (28:12)	11010111000000101	11010111000001101	11010111000010101	11010111000100101	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	107

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input Output contents. It places the boundary scan register between TDI and TDO. This forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input output ring contents. It places the boundary scan register between TDI and TDO. This operation does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

[+] Feedback

Boundary Scan Order

Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID
0	6R	27	11H	54	7B	81	3G
1	6P	28	10G	55	6B	82	2G
2	6N	29	9G	56	6A	83	1J
3	7P	30	11F	57	5B	84	2J
4	7N	31	11G	58	5A	85	3K
5	7R	32	9F	59	4A	86	3J
6	8R	33	10F	60	5C	87	2K
7	8P	34	11E	61	4B	88	1K
8	9R	35	10E	62	3A	89	2L
9	11P	36	10D	63	1H	90	3L
10	10P	37	9E	64	1A	91	1M
11	10N	38	10C	65	2B	92	1L
12	9P	39	11D	66	3B	93	3N
13	10M	40	9C	67	1C	94	3M
14	11N	41	9D	68	1B	95	1N
15	9M	42	11B	69	3D	96	2M
16	9N	43	11C	70	3C	97	3P
17	11L	44	9B	71	1D	98	2N
18	11M	45	10B	72	2C	99	2P
19	9L	46	11A	73	3E	100	1P
20	10L	47	Internal	74	2D	101	3R
21	11K	48	9A	75	2E	102	4R
22	10K	49	8B	76	1E	103	4P
23	9J	50	7C	77	2F	104	5P
24	9K	51	6C	78	3F	105	5N
25	10J	52	8A	79	1G	106	5R
26	11J	53	7A	80	1F		

[+] Feedback

Power Up Sequence in DDR-II+ SRAM

DDR-II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations. During power up, when the $\overline{DOFF}$ is tied HIGH, the DLL gets locked after 2048 cycles of stable clock.

Power Up Sequence

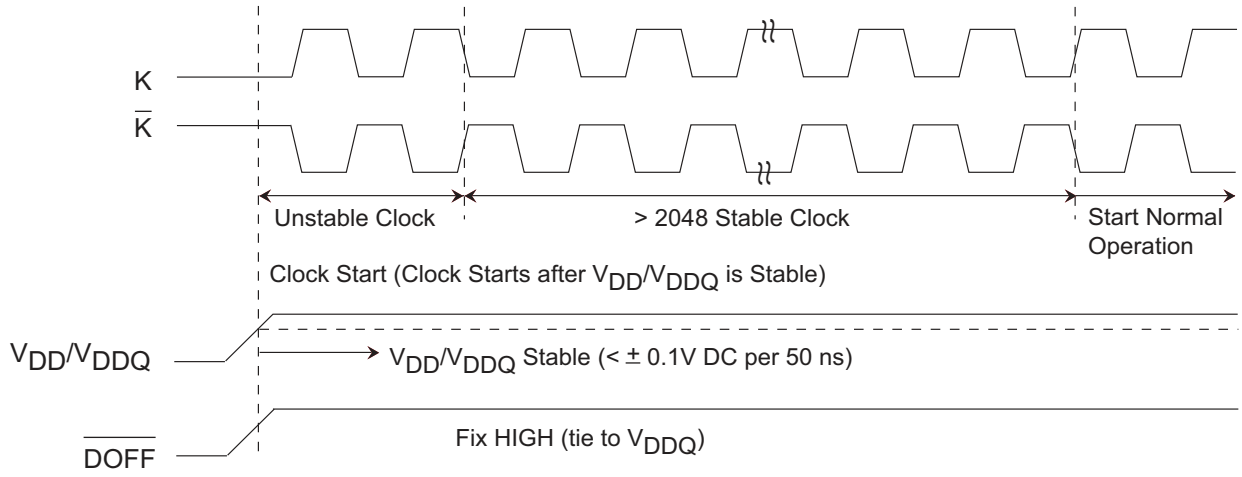
- Apply power with $\overline{DOFF}$ tied HIGH (all other inputs can be HIGH or LOW)
  - Apply V_{DD} before V_{DDQ}
  - Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}
- Provide stable power and clock (K, $\overline{K}$) for 2048 cycles to lock the DLL.

DLL Constraints

- DLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as $t_{KC\ Var}$.
- The DLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the DLL is enabled, then the DLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 2048 cycles stable clock to relock to the desired clock frequency.

Power Up Waveforms

Figure 5. Power Up Waveforms



[+] Feedback

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied. –55°C to + 125°C

Supply Voltage on V_{DD} Relative to GND .....–0.5V to + 2.9V

Supply Voltage on V_{DDQ} Relative to GND..... –0.5V to + V_{DD}

DC Applied to Outputs in High-Z .....–0.5V to V_{DDQ} + 0.3V

DC Input Voltage[11].....–0.5V to V_{DD} + 0.3V

Current into Outputs (LOW).....20 mA

Static Discharge Voltage (MIL-STD-883, M 3015).... >2001V

Latch up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}[15]	V_{DDQ}[15]
Commercial	0°C to +70°C	1.8 ± 0.1V	1.4V to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristic

The DC Electrical Characteristics over the operating range follows.[12]

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage			1.7	1.8	1.9	V
V_{DDQ}	IO Supply Voltage			1.4	1.5	V_{DD}	V
V_{OH}	Output HIGH Voltage	Note 16		$V_{DDQ}/2 – 0.12$		$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output LOW Voltage	Note 17		$V_{DDQ}/2 – 0.12$		$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH Voltage	I_{OH} = –0.1 mA, Nominal Impedance		$V_{DDQ} – 0.2$		V_{DDQ}	V
$V_{OL(LOW)}$	Output LOW Voltage	I_{OL} = 0.1 mA, Nominal Impedance		V_{SS}		0.2	V
V_{IH}	Input HIGH Voltage			$V_{REF} + 0.1$		$V_{DDQ} + 0.15$	V
V_{IL}	Input LOW Voltage			–0.15		$V_{REF} – 0.1$	V
I_X	Input Leakage Current	$GND \le V_I \le V_{DDQ}$		–2		2	µA
I_{OZ}	Output Leakage Current	$GND \le V_I \le V_{DDQ}$, Output Disabled		–2		2	µA
V_{REF}	Input Reference Voltage[18]	Typical Value = 0.75V		0.68	0.75	0.95	V
I_{DD} [19]	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{max} = $1/t_{CYC}$	300 MHz			850	mA
			333 MHz			920	mA
			375 MHz			1020	mA
			400 MHz			1080	mA
I_{SB1}	Automatic Power Down Current	Max V_{DD}, Both Ports Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$ f = f_{max} = $1/t_{CYC}$, Inputs Static	300 MHz			250	mA
			333 MHz			260	mA
			375 MHz			290	mA
			400 MHz			300	mA

AC Input Requirements

Over the operating range [11]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage		$V_{REF} + 0.2$	–	$V_{DDQ} + 0.24$	V
V_{IL}	Input LOW Voltage		–0.24	–	$V_{REF} – 0.2$	V

Notes

15. Power up: Is based on a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
16. Outputs are impedance controlled. $I_{OH} = –(V_{DDQ}/2)/(RQ/5)$ for values of $175\Omega \le RQ \le 350\Omega$.
17. Outputs are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of $175\Omega \le RQ \le 350\Omega$
18. V_{REF} (min) = 0.68V or 0.46V_{DDQ}, whichever is larger, V_{REF} (max) = 0.95V or 0.54V_{DDQ}, whichever is smaller.
19. The operation current is calculated with 50% read cycle and 50% write cycle.

[+] Feedback

Capacitance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 1.8V V_{DDQ} = 1.5V	5	pF
C_{CLK}	Clock Input Capacitance		6	pF
C_O	Output Capacitance		7	pF

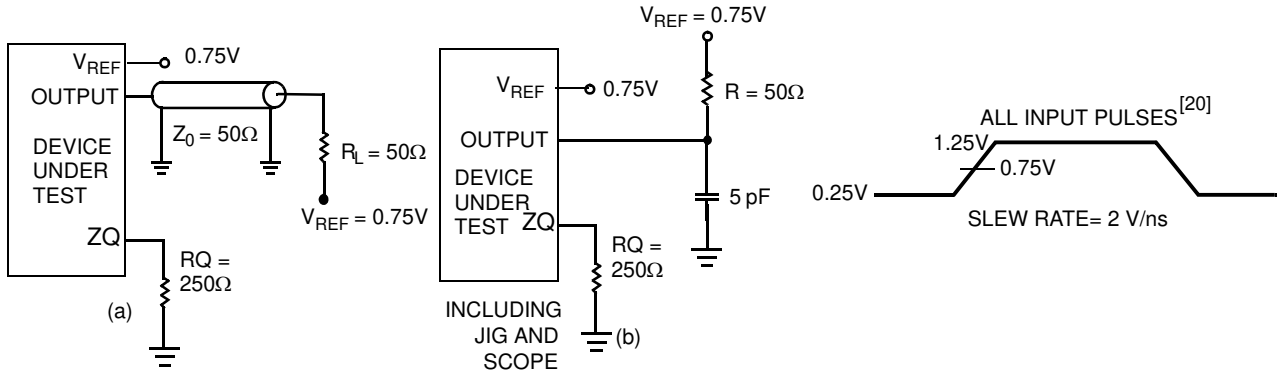
Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	165 FBGA Package	Unit
Θ_{JA}	Thermal Resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	17.2	°C/W
Θ_{JC}	Thermal Resistance (junction to case)		4.15	°C/W

AC Test Loads and Waveforms

Figure 6. AC Test loads and Waveforms



Note

20. Unless otherwise noted, test conditions are based on a signal transition time of 2V/ns, timing reference levels of 0.75V, V_{REF} = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC Test Loads and Waveforms.

[+] Feedback

Switching Characteristics

Over the operating range[20, 21]

Cypress Parameter	Consortium Parameter	Description	400 MHz		375 MHz		333 MHz		300 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{POWER}		V_{DD}(Typical) to the first Access[22]	1	–	1	–	1	–	1	–	ms
t_{CYC}	t_{KHKH}	K Clock Cycle Time	2.50	8.40	2.66	8.40	3.0	8.40	3.3	8.40	ns
t_{KH}	t_{KHKL}	Input Clock (K/$\overline{K}$) HIGH	0.4	–	0.4	–	0.4	–	0.4	–	t_{CYC}
t_{KL}	t_{KLKH}	Input Clock (K/$\overline{K}$) LOW	0.4	–	0.4	–	0.4	–	0.4	–	t_{CYC}
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K Clock Rise to $\overline{K}$ Clock Rise (rising edge to rising edge)	1.06	–	1.13	–	1.28	–	1.40	–	ns
Setup Times											
t_{SA}	t_{AVKH}	Address Setup to K Clock Rise	0.4	–	0.4	–	0.4	–	0.4	–	ns
t_{SC}	t_{IVKH}	Control Setup to K Clock Rise ($\overline{LD}$, R/$\overline{W}$)	0.4	–	0.4	–	0.4	–	0.4	–	ns
t_{SCDDR}	t_{IVKH}	Double Data Rate Control Setup to Clock (K/$\overline{K}$) Rise ($\overline{BWS}_0$, $\overline{BWS}_1$, $\overline{BWS}_2$, $\overline{BWS}_3$)	0.28	–	0.28	–	0.28	–	0.28	–	ns
t_{SD}	t_{DVKH}	$D_{[X:0]}$ Setup to Clock (K/$\overline{K}$) Rise	0.28	–	0.28	–	0.28	–	0.28	–	ns
Hold Times											
t_{HA}	t_{KHAX}	Address Hold after K Clock Rise	0.4	–	0.4	–	0.4	–	0.4	–	ns
t_{HC}	t_{KHIX}	Control Hold after K Clock Rise ($\overline{LD}$, R/$\overline{W}$)	0.4	–	0.4	–	0.4	–	0.4	–	ns
t_{HCDDR}	t_{KHIX}	Double Data Rate Control Hold after Clock (K/$\overline{K}$) Rise ($\overline{BWS}_0$, $\overline{BWS}_1$, $\overline{BWS}_2$, $\overline{BWS}_3$)	0.28	–	0.28	–	0.28	–	0.28	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ Hold after Clock (K/$\overline{K}$) Rise	0.28	–	0.28	–	0.28	–	0.28	–	ns
Output Times											
t_{CO}	t_{CHQV}	K/$\overline{K}$ Clock Rise to Data Valid	–	0.45	–	0.45	–	0.45	–	0.45	ns
t_{DOH}	t_{CHQX}	Data Output Hold after K/$\overline{K}$ Clock Rise (Active to Active)	–0.45	–	–0.45	–	–0.45	–	–0.45	–	ns
t_{CCQO}	t_{CHCQV}	K/$_K$ Clock Rise to Echo Clock Valid	–	0.45	–	0.45	–	0.45	–	0.45	ns
t_{CQOH}	t_{CHCQX}	Echo Clock Hold after K/$\overline{K}$ Clock Rise	–0.45	–	–0.45	–	–0.45	–	–0.45	–	ns
t_{CQD}	t_{CQHQV}	Echo Clock High to Data Valid	–	0.2	–	0.2	–	0.2	–	0.2	ns
t_{CQDOH}	t_{CQHQX}	Echo Clock High to Data Invalid	–0.2	–	–0.2	–	–0.2	–	–0.2	–	ns
t_{CQH}	t_{CQHCQL}	Output Clock (CQ/$\overline{CQ}$) HIGH[23]	0.81	–	0.88	–	1.03	–	1.15	–	ns
$t_{CQH\overline{CQ}H}$	$t_{CQH\overline{CQ}H}$	CQ Clock Rise to $\overline{CQ}$ Clock Rise[23] (rising edge to rising edge)	0.81	–	0.88	–	1.03	–	1.15	–	ns
t_{CHZ}	t_{CHQZ}	Clock (K/$\overline{K}$) Rise to High-Z (Active to High-Z)[24, 25]	–	0.45	–	0.45	–	0.45	–	0.45	ns
t_{CLZ}	t_{CHQX1}	Clock (K/$\overline{K}$) Rise to Low-Z[24, 25]	–0.45	–	–0.45	–	–0.45	–	–0.45	–	ns
t_{QVLD}	t_{QVLD}	Echo Clock High to QVLD Valid[26]	–0.20	0.20	–0.20	0.20	–0.20	0.20	–0.20	0.20	ns
DLL Timing											
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock Phase Jitter	–	0.20	–	0.20	–	0.20	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	DLL Lock Time (K)	2048	–	2048	–	2048	–	2048	–	Cycles
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K Static to DLL Reset[27]	30	–	30	–	30	–	30	–	ns

Notes

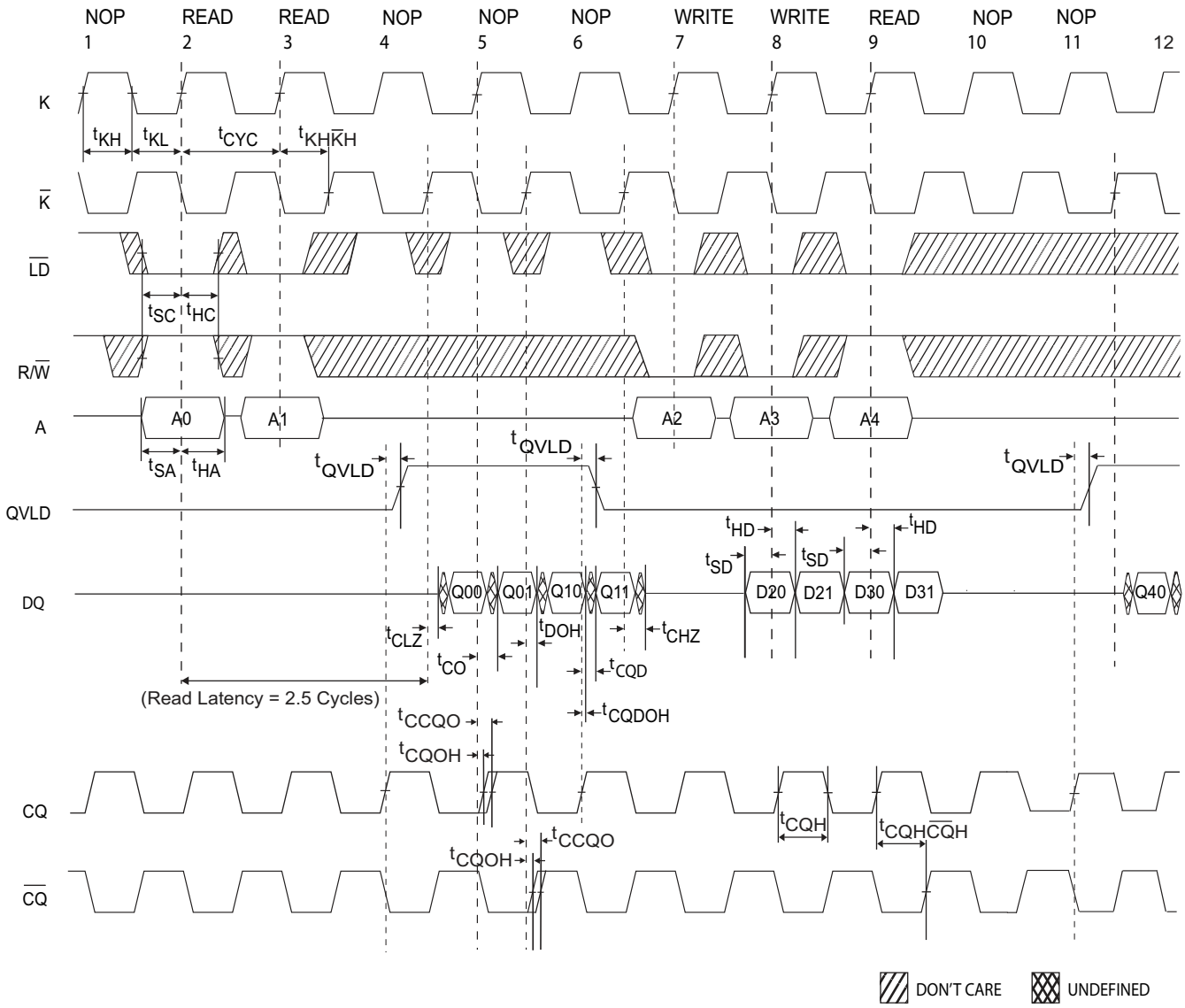
21. When a part with a maximum frequency above 300 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
22. This part has a voltage regulator internally; t_{POWER} is the time that the power must be supplied above V_{DD} minimum initially before a read or write operation can be initiated.
23. These parameters are extrapolated from the input timing parameters ($t_{KH\overline{K}H}$ - 250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps ($t_{KC\ Var}$) is already included in the $t_{KH\overline{K}H}$). These parameters are only guaranteed by design and are not tested in production.
24. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5 pF as in (b) of "AC Test Loads and Waveforms" on page 21. Transition is measured ± 100 mV from steady-state voltage.
25. At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.
26. t_{QVLD} spec is applicable for both rising and falling edges of QVLD signal.
27. Hold to $>V_{IH}$ or $<V_{IL}$.

[+] Feedback

Switching Waveform

Read/Write/Deselect Sequence

Figure 7. Waveform for 2.5 Cycle Read Latency[28, 29]



Notes

28. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, i.e., A0 + 1.
29. Outputs are disabled (High-Z) one clock cycle after a NOP.

[+] Feedback

Ordering Information

Not all of the speed, package and temperature ranges are available. Contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
400	CY7C1166V18-400BZC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1177V18-400BZC			
	CY7C1168V18-400BZC			
	CY7C1170V18-400BZC			
	CY7C1166V18-400BZXC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1177V18-400BZXC			
	CY7C1168V18-400BZXC			
	CY7C1170V18-400BZXC			
	CY7C1166V18-400BZI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1177V18-400BZI			
	CY7C1168V18-400BZI			
	CY7C1170V18-400BZI			
	CY7C1166V18-400BZXI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1177V18-400BZXI			
	CY7C1168V18-400BZXI			
	CY7C1170V18-400BZXI			
375	CY7C1166V18-375BZC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1177V18-375BZC			
	CY7C1168V18-375BZC			
	CY7C1170V18-375BZC			
	CY7C1166V18-375BZXC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1177V18-375BZXC			
	CY7C1168V18-375BZXC			
	CY7C1170V18-375BZXC			
	CY7C1166V18-375BZI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1177V18-375BZI			
	CY7C1168V18-375BZI			
	CY7C1170V18-375BZI			
	CY7C1166V18-375BZXI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1177V18-375BZXI			
	CY7C1168V18-375BZXI			
	CY7C1170V18-375BZXI			

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Ordering Information (continued)

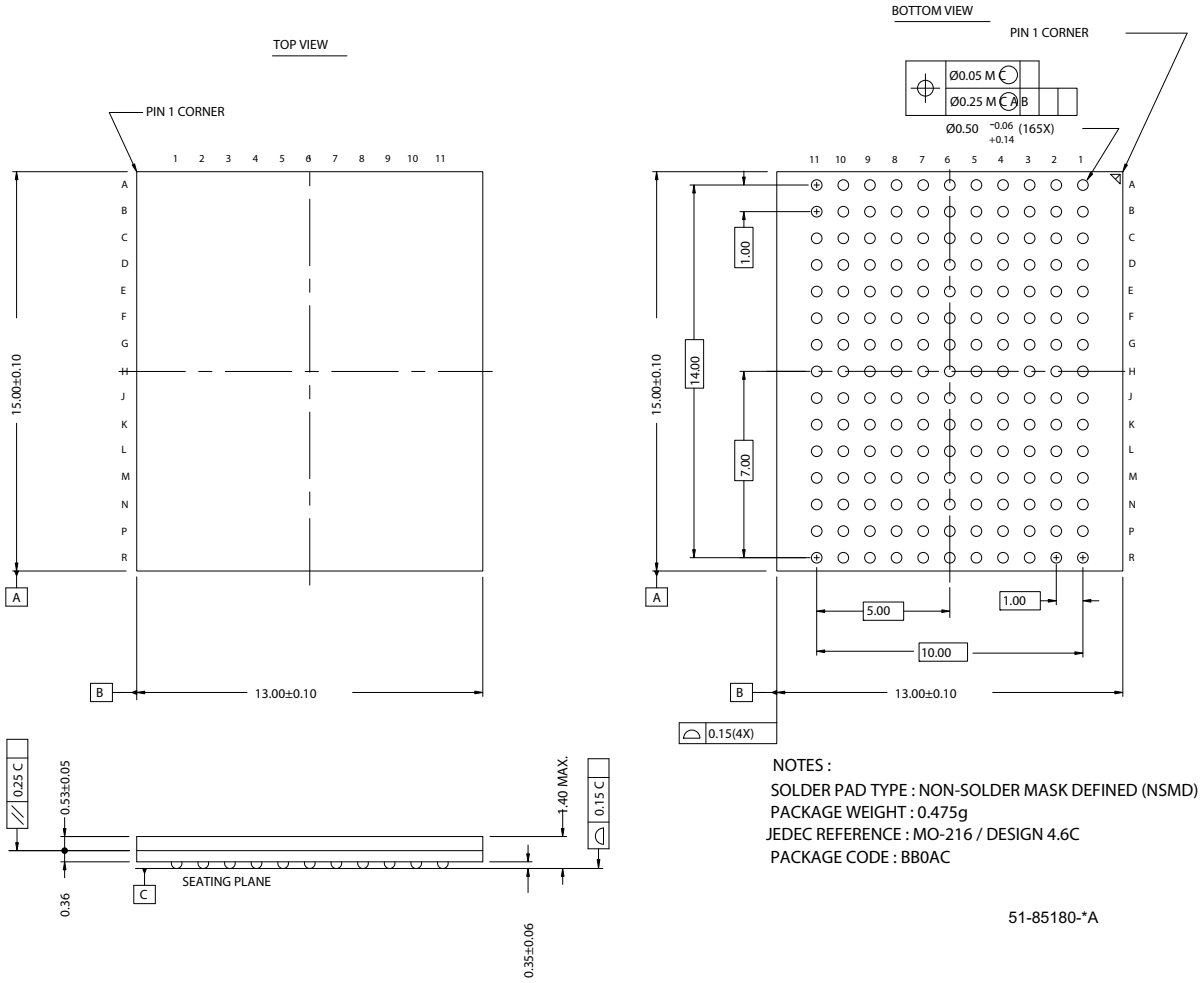
Not all of the speed, package and temperature ranges are available. Contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
333	CY7C1166V18-333BZC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1177V18-333BZC			
	CY7C1168V18-333BZC			
	CY7C1170V18-333BZC			
	CY7C1166V18-333BZXC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1177V18-333BZXC			
	CY7C1168V18-333BZXC			
	CY7C1170V18-333BZXC			
	CY7C1166V18-333BZI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1177V18-333BZI			
	CY7C1168V18-333BZI			
	CY7C1170V18-333BZI			
	CY7C1166V18-333BZXI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1177V18-333BZXI			
	CY7C1168V18-333BZXI			
	CY7C1170V18-333BZXI			
300	CY7C1166V18-300BZC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Commercial
	CY7C1177V18-300BZC			
	CY7C1168V18-300BZC			
	CY7C1170V18-300BZC			
	CY7C1166V18-300BZXC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1177V18-300BZXC			
	CY7C1168V18-300BZXC			
	CY7C1170V18-300BZXC			
	CY7C1166V18-300BZI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial
	CY7C1177V18-300BZI			
	CY7C1168V18-300BZI			
	CY7C1170V18-300BZI			
	CY7C1166V18-300BZXI	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	
	CY7C1177V18-300BZXI			
	CY7C1168V18-300BZXI			
	CY7C1170V18-300BZXI			

[+] Feedback

Package Diagram

Figure 8. 165-Ball FBGA (13 x 15 x 1.4 mm), 51-85180



[+] Feedback

Document History Page

Document Title: CY7C1166V18/CY7C1177V18/CY7C1168V18/CY7C1170V18, 18-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) Document Number: 001-06620				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	430351	See ECN	NXR	New data sheet
*A	461654	See ECN	NXR	Revised the MPNs from CY7C1177BV18 to CY7C1166V18 CY7C1168BV18 to CY7C1177V18 CY7C1170BV18 to CY7C1168V18 Changed t_{TH} and t_{TL} from 40 ns to 20 ns, changed t_{TMSS}, t_{TDIS}, t_{CS}, t_{TMSH}, t_{TDIH}, t_{CH} from 10 ns to 5 ns and changed t_{TDOV} from 20 ns to 10 ns in TAP AC Switching Characteristics table Modified Power Up waveform
*B	497629	See ECN	NXR	Changed the V_{DDQ} operating voltage to 1.4V to V_{DD} in the Features section, in Operating Range table and in the DC Electrical Characteristics table Added foot note in page 1 Changed the Maximum rating of Ambient Temperature with Power Applied from –10°C to +85°C to –55°C to +125°C Changed V_{REF} (max) spec from 0.85V to 0.95V in the DC Electrical Characteristics table and in the note below the table Updated foot note 21 to specify Overshoot and Undershoot Spec Updated Θ_{JA} and Θ_{JC} values Removed x9 part and its related information Updated foot note 24
*C	1175245	See ECN	VKN/KKVTMP	Converted from preliminary to final Added x8 and x9 parts Updated logic block diagram for x18 and x36 parts Changed I_{DD} values from 830 mA to 1080 mA for 400 MHz, 794 mA to 1020 mA for 375 MHz, 733 mA to 920 mA for 333 MHz, 685 mA to 850 mA for 300 MHz Changed I_{SB} values from 235 mA to 300 mA for 400 MHz, 227 mA to 290 mA for 375 MHz, 212 mA to 260 mA for 333 MHz, 201 mA to 250 mA for 300 MHz Changed $t_{CYC(max)}$ spec to 8.4 ns for all speed bins Changed Θ_{JA} value from 13.48 °C/W to 17.2 °C/W Updated Ordering Information table
*D	2199066	See ECN	VKN/AESA	Added footnote# 19 related to I_{DD}

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