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BCM4318/BCM4318E

AirForce One™ Chip 802.11g MAC/Baseband/Radio

GENERAL DESCRIPTION

The BCM4318/BCM4318E provide One Chip IEEE 802.11g MAC, Baseband, and Direct Conversion Radio functions to provide wireless LAN connectivity supporting data rates from 1 Mbps to 54 Mbps in the 2.4-GHz band. With the addition of the BCM2060, the solution can also support 802.11a for 1-Mbps to 54-Mbps connectivity in the 5-GHz band. In addition, the BCM4318E includes leading-edge Encore DSP technology for best-in-class receive sensitivity and extended range, enabling whole home coverage. The BCM4318E also supports high-speed performance mode (125-Mbps) that is backward-compatible with standard 802.11b/g. Broadcom's revolutionary One Chip architecture implemented in bulk CMOS process greatly reduces the external components typically required for 802.11a/g implementations, resulting in significant cost, power, and footprint savings.

State-of-the-art security is provided by industry standardized system support for WEP, WEP2, and AES encryption, coupled with TKIP and IEEE 802.1x support. Increased performance and a significant reduction in host-CPU utilization in both client and access device configurations are achieved through hardware support of encryption/decryption.

The BCM4318/BCM4318E employ a native 32-bit bus using a direct memory access architecture that results in significant performance improvements over competing solutions in both transfer rate and CPU utilization. Various system bus interfaces are included for maximum flexibility: Mini PCI, PCI, CardBus, PCMCIA/Compact Flash, and SDIO/SPI.

The BCM4318/BCM4318E employ adaptive equalization algorithms resulting in significant resistance to multipath, providing substantial improvements in real-world performance.

FEATURES

- Extreme Integration: IEEE 802.11a/g compliant CMOS MAC / Baseband and 2.4-GHz Direct Conversion Radio (802.11a radio support provided by an external BCM2060 5-GHz Direct Conversion Radio)
- BCM4318E includes Encore signal processing for industry-leading receive sensitivity and extended range:
  - –74 dBm at 54Mbps
  - –76 dBm with external LNA
- High level of integration with direct conversion radio architecture minimizes external circuitry, leading to lowest cost, lowest power, and smallest footprint implementation
- Flexible support for a variety of system bus interfaces including: PCI, Mini PCI, CardBus, PCMCIA/Compact Flash, and SDIO (4-wire, 1-wire, and SPI)
- Programmable data rates of 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54 Mbps
- Supports high-speed performance mode of 125-Mbps that is backward-compatible with standard 802.11b/g; BCM4318E in 196-pin package supports Afterburner mode (125-Mbps)
- 24-bit IV and 40-bit/104-bit key WEP encryption support
- 128-bit IV and 128-bit key WEP2 encryption support
- System support for 128-bit AES
- IEEE 802.1x support
- Programmable MAC with advanced DMA architecture and 32-bit bus interface
- Dynamic Power Management under driver control
- WHQL-certified drivers for Windows® XP, Windows® Me, Windows® 2000, Windows® 98SE, and Windows® 98 operating systems
- All drivers are portable for embedded operating systems such as Linux® and Windows® CE
- Meets PCI Power Management Interface version 1.1 (ACPI)
- Wi-Fi® compliant; supports SecureEZSetup™
- Support for Bluetooth® Coexistence Algorithm
- 3.3/1.8V supply, 3/5V PCI I/O
- 144-ball FBGA or 196-ball FBGA (adds UART, PCI/Cardbus and BCM2060 interfaces)

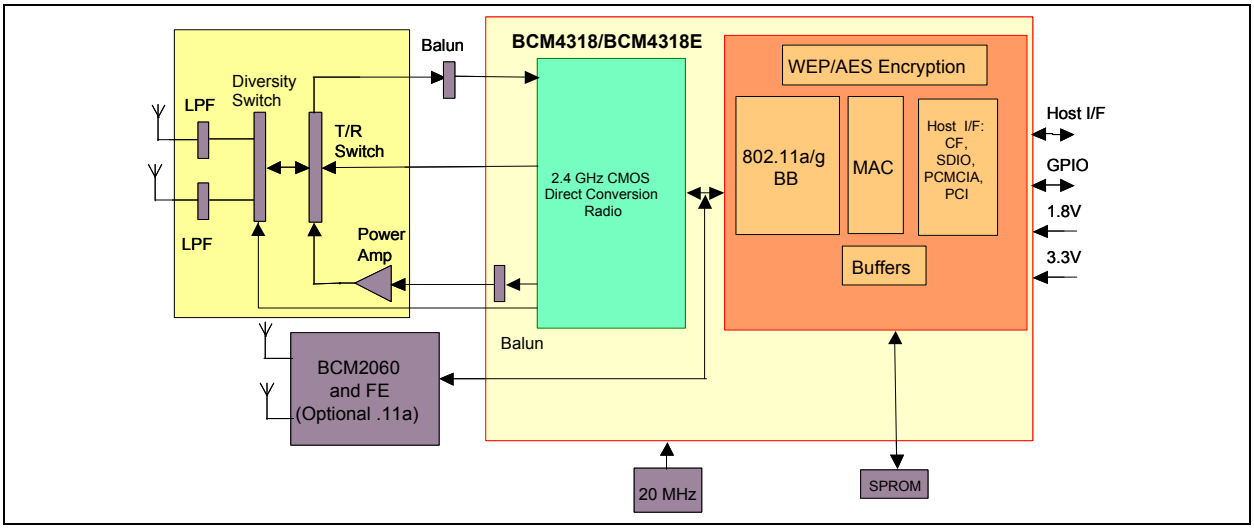

Figure 1: BCM4318/BCM4318E System Diagram

16215 Alton Parkway • P.O. Box 57013 • Irvine, California 92619-7013 • Phone: 949-450-8700 • Fax: 949-450-8710

REVISION HISTORY

Revision	*Date*	*Change Description*
4318_4318E-DS01-R	11/09/04	Updated ESD value in Table 13 on page 36.
4318_4318E-DS00-R	10/26/04	Initial release.

Broadcom Corporation
P.O. Box 57013
16215 Alton Parkway
Irvine, California 92619-7013

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Section 1: Functional Description

INTRODUCTION

The BCM4318/BCM4318E are highly integrated, single-chip, IEEE Std 802.11a/g MAC, baseband and 2.4-GHz direct conversion radios designed for client cards, modules, and WOMBO (Wireless On Motherboard) solutions. The revolutionary Broadcom® One Chip architecture greatly reduces the external components typically required for IEEE 802.11a/g implementations, resulting in significant savings in cost, power, and board space.

The BCM4318/BCM4318E offer flexible support for a variety of system bus interfaces including PCI, Mini PCI, CardBus, PCMCIA, Compact Flash, and SDIO/SPI. Customer-specified parameters, such as System Vendor ID and Wireless LAN MAC address, are stored in a small external SPROM.

In addition, the BCM4318E chip includes leading-edge Encore DSP technology for improved receive sensitivity, which extends the range and enables whole home coverage. The BCM4318E chip also supports a UART interface for WLAN design support.

The package options are 144 pin and 196 pin, as follows:

- The BCM4318 chip in the 196-pin package adds PCI, CardBus, and BCM2060 IEEE 802.11a radio interfaces, but does not support Encore DSP technology.
- The BCM4318E chip in the 196-pin package adds PCI, CardBus, and BCM2060 IEEE 802.11a radio interfaces. It includes Encore DSP technology, and it supports a UART interface.
- The BCM4318E chip in the 144-pin package provides PCMCIA, Compact Flash, and SDIO/SPI bus interfaces. It includes Encore DSP technology.

Table 1 lists differences between the BCM4318 and BCM4318E chips and between the 144-pin and 196-pin packages.

Table 1: Differences Among BCM4318/BCM4318E and 144-Pin/196-Pin Packages

Chip	*Package*	*(Mini) PCI*	*CardBus*	*PCMCIA*	*Compact Flash*	*SDIO/ SPI*	*SPROM*	*GPIO*	*IEEE 802.11a PHY*	*Encore and After-burner*
BCM4318	196-pin BCM4318KFBG	Yes	Yes	Yes	Yes	SDIO/ SPI	Yes	8	Yes	–
BCM4318E	196-pin BCM4318EKFBG	Yes	Yes	Yes	Yes	SDIO/ SPI/ UART[1]	Yes	8	Yes	Encore and After-burner
BCM4318E	144-pin BCM4318SKFBG	–	–	Yes	Yes	SDIO/ SPI	Yes	6	–	Encore

Notes:
1. The UART option is only available in the BCM4318E 196-pin package option, BCM4318EKFBG.

IEEE 802.11A/G MAC FEATURES

The IEEE 802.11a/g MAC features include:

- Programmable Access Point (AP) or station (STA) functionality
- Programmable Independent Basic Service Set (IBSS), or infrastructure mode
- Passive scanning, 802.11h (including radio detection)
- Network Allocation Vector (NAV), Interframe Space (IFS), and Timing Synchronization Function (TSF) functionality
- Backoff
- RTS/CTS procedure
- Transmission of response frames (ACK/CTS)
- Address filtering of RX frames as specified by IBSS rules
- Multirate support
- Programmable Target Beacon Transmission Time (TBTT), beacon transmission/cancellation, and programmable Announcement Traffic Indication Message (ATIM) window
- CF conformance: setting NAV for neighborhood Point Coordination Function (PCF) operation
- Privacy through a variety of Wired Equivalent Privacy (WEP) encryption schemes and dynamically programmable WEP keys
- Power management
- Statistics counters for MIB support

IEEE 802.11A/G MAC DESCRIPTION

The MAC core provides the support required for the transmission and reception of sequences of packets, together with related timing, without any packet-by-packet driver interaction. Time-critical tasks requiring response times of only a few milliseconds are handled in the MAC core. This achieves the required timing on the medium while keeping the host driver easier to write and maintain. Also, incoming packets are buffered in the MAC core, which allows the MAC driver to process them in bursts as and when it gets access to the buffers.

The MAC driver interacts with the MAC core to prepare queues of packets to transmit and to analyze and forward received packets. The internal blocks of the MAC core are connected to a Programmable State Machine (PSM) through an internal bus. See Figure 2.

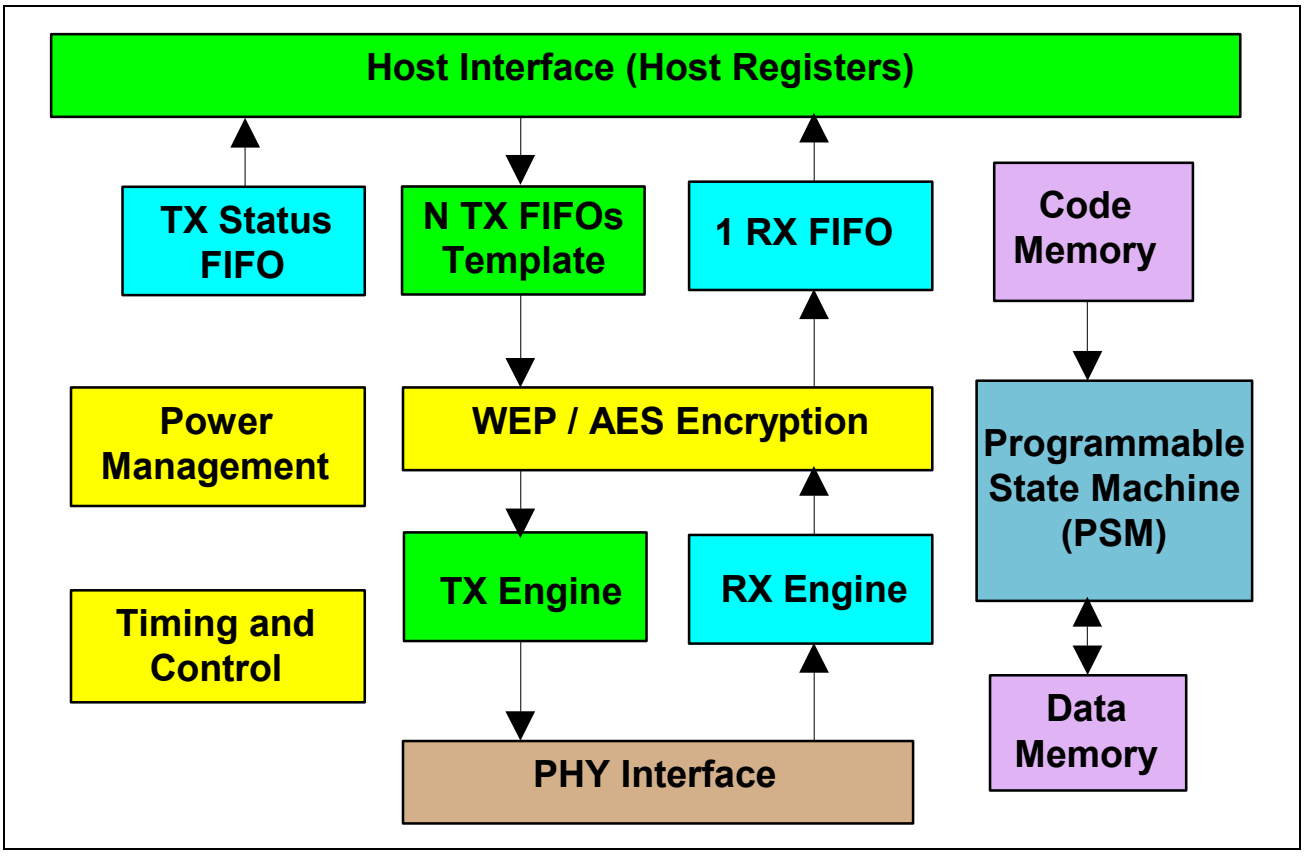


Figure 2: IEEE 802.11a/g MAC Block Diagram

The host interface consists of registers for controlling and monitoring the status of the MAC core and interfacing with the TX/RX FIFOs. There are four transmit FIFOs: asynchronous, priority, Broadcast/Multicast (BC/MC) and ATIM. Each transmit FIFO is 3-KB deep. In addition to the transmit FIFOs, there is a 1-KB template area for response frames. Whenever the host has a frame to transmit, the host queues the frame into one of the transmit FIFOs with a TX descriptor containing TX control information. The PSM schedules the transmission on the medium depending on the frame type, transmission rules in IEEE 802.11 protocol, and the current medium occupancy scenario. After the transmission is completed and an ACK is received, a TX status is returned to the host confirming the same in the TX status FIFO.

The MAC contains a single 4.5-KB RX FIFO. Whenever a frame is received, the frame is sent to the host along with an RX descriptor that contains additional information about the frame reception conditions.

The Power Management block maintains the information regarding the power management state of the core (and the associated STAs in case of an AP) to help in dynamic decisions by the core regarding frame transmission.

The WEP block performs the required WEP operation on the TX/RX frames. The WEP block supports separate transmit and receive keys with four shared keys and 50 link-specific keys. The link-specific keys are used to establish a secure link between any two STAs, with the required key being shared between only those two STAs, hence excluding all the other STAs in the same network from deciphering the communication between those two STAs. The WEP block supports the following encryption schemes that can be selected on a per-destination basis:

- None: the WEP block acts as a pass-through
- WEP: 40-bit secure key and 24-bit IV as defined in IEEE Std 802.11-1999

- WEP128: 104-bit secure key and 24-bit IV
- WEP2: 128-bit secure key and 128-bit IV
- TKIP: IEEE 802.11i draft
- AES: IEEE 802.11i draft

The transmit engine is responsible for the byte flow from the TX FIFO to the PHY interface through the WEP block and the addition of an FCS (CRC-32) as required by IEEE 802.11. Similarly, the receive engine is responsible for byte flow from the PHY interface to the RX FIFO through the WEP block and for detection of errors in the RX frame.

The timing block performs the TSF, NAV, and IFS functionality as described in IEEE 802.11-1999.

The Programmable State Machine (PSM) coordinates the operation of different hardware blocks required for both transmission and reception. The PSM also maintains the statistics counters required for MIB support.

IEEE 802.11A/G PHY FEATURES

The integrated IEEE 802.11a/g physical layer device (PHY) features include:

- Data rates of 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54 Mbps
- Both long and optional short preamble
- Resistance to multipath (>250 nanoseconds RMS delay spread) with maximal ratio combining rake receiver for data rates of 1 and 2 Mbps and adaptive equalization for data rates of 5.5 Mbps and 11 Mbps
- Programmable antenna selection
- Automatic Gain Control (AGC)
- Available per-packet channel quality and signal strength measurements
- Dedicated interface to the BCM2060 5-GHz Direct Conversion Radio for IEEE 802.11a support

IEEE 802.11A/G PHY DESCRIPTION

The Wireless Local Area Network (WLAN) PHY integrated on this IC provides baseband processing at data rates of 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54 Mbps, as specified in the Direct Sequence Spread Spectrum (DSSS) and Orthogonal Frequency Division Multiplexing (OFDM) portions of IEEE 802.11a/g. This core acts as an intermediary between the MAC on the one hand, and the integrated 2.4-GHz Radio or external 5-GHz radio (BCM2060) integrated circuit on the other, converting back and forth between packets and baseband waveforms.

An overview of the operations carried out by the PHY is shown in Figure 3. On transmission, physical layer framing is first added to a packet received from the MAC. The resulting bits are then scrambled, modulated, filtered, and finally sent to the RF via a pair of 80-MHz, 6-bit Digital-to-Analog Converters (DACs). Modulation is selected per packet as either Differential Binary Phase Shift Keying (DBPSK), Differential Quadrature Phase Shift Keying (DQPSK), or Complementary Code Keying (CCK). The first two types of modulation provide data rates of 1 Mbps and 2 Mbps, respectively, and require spreading the modulated symbols with a length 11 Barker code. CCK modulation is used for data rates of 5.5 Mbps and 11 Mbps and inherently includes the spreading.

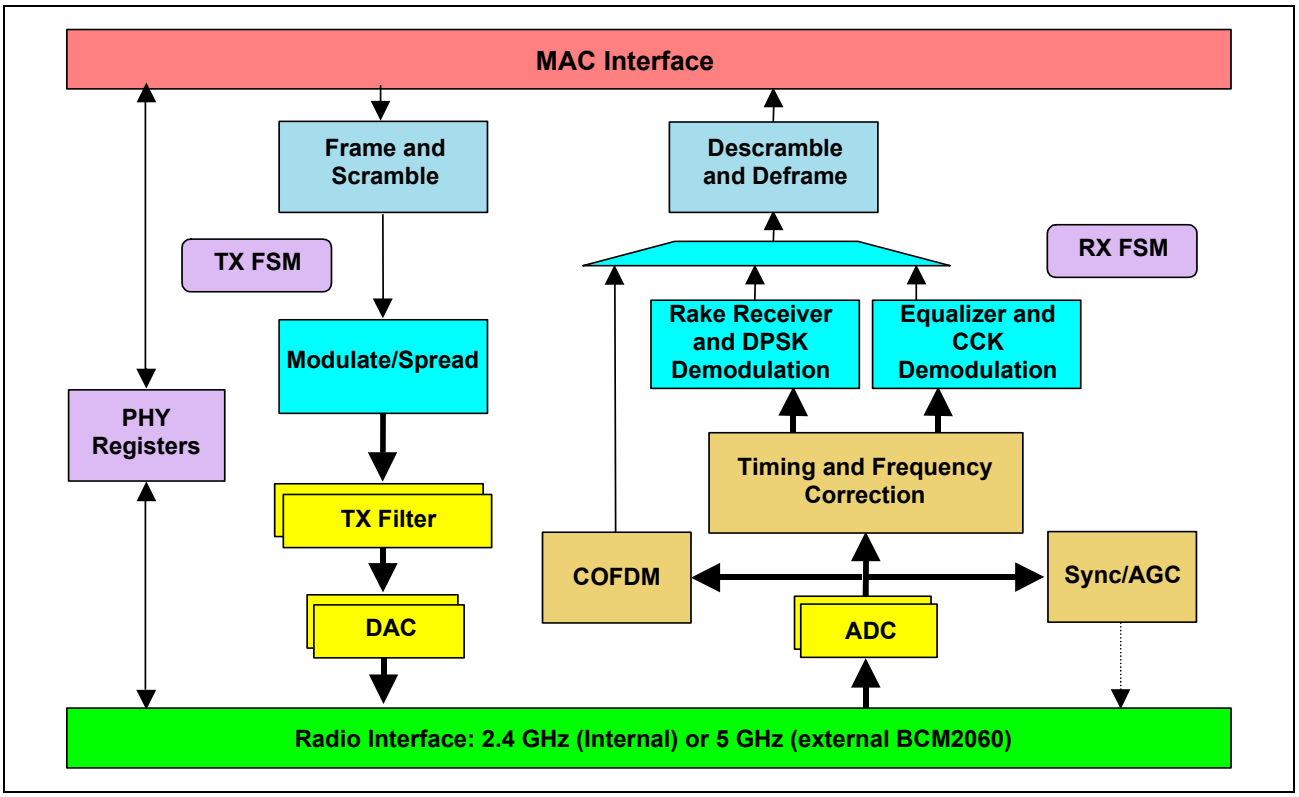


Figure 3: IEEE 802.11a/g PHY Block Diagram

On reception, the reverse operations are performed. The In-phase (I) and Quadrature (Q) baseband waveforms coming from a pair of 40-MHz, 6-bit Analog-to-Digital Converters (ADCs) are demodulated into bits and then descrambled and deframed. To improve the likelihood of correct reception, however, the waveforms are subjected to timing and frequency offset corrections (adapted throughout packet reception) prior to demodulation. Further, using a maximal ratio combining rake receiver for data rates of 1 Mbps and 2 Mbps and an adaptive equalizer at the higher bit rates, the PHY is able to work in extreme multipath channels, successfully receiving even at a data rate of 11 Mbps, with delay spreads exceeding 200 nanoseconds RMS.

Additionally, the receiver must perform synchronization at the start of packet reception, which includes Automatic Gain Control (AGC), antenna selection, and initial frequency offset and timing estimation. A state machine coordinates all of these activities (using information from the PHY framing) to decide how to handle the packet body.

A register interface accessible from both the MAC and the host allows programming of the PHY parameters, although information generally needed per packet is passed as part of the packet itself. For example, this is true of preamble type and data rate on transmission, as well as the channel metrics Signal Quality (SQ) and signal strength on reception. The internal 2.4-GHz radio and BCM2060 registers are accessed indirectly through the PHY registers.

Integrated Radio Transceiver

The BCM4318/BCM4318E include an integrated RF transceiver that has been optimized for use in 2.4-GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the

globally available 2.4-GHz unlicensed ISM band. With an external transmit power amplifier, it develops full output power per the IEEE 802.11b/g Specification. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

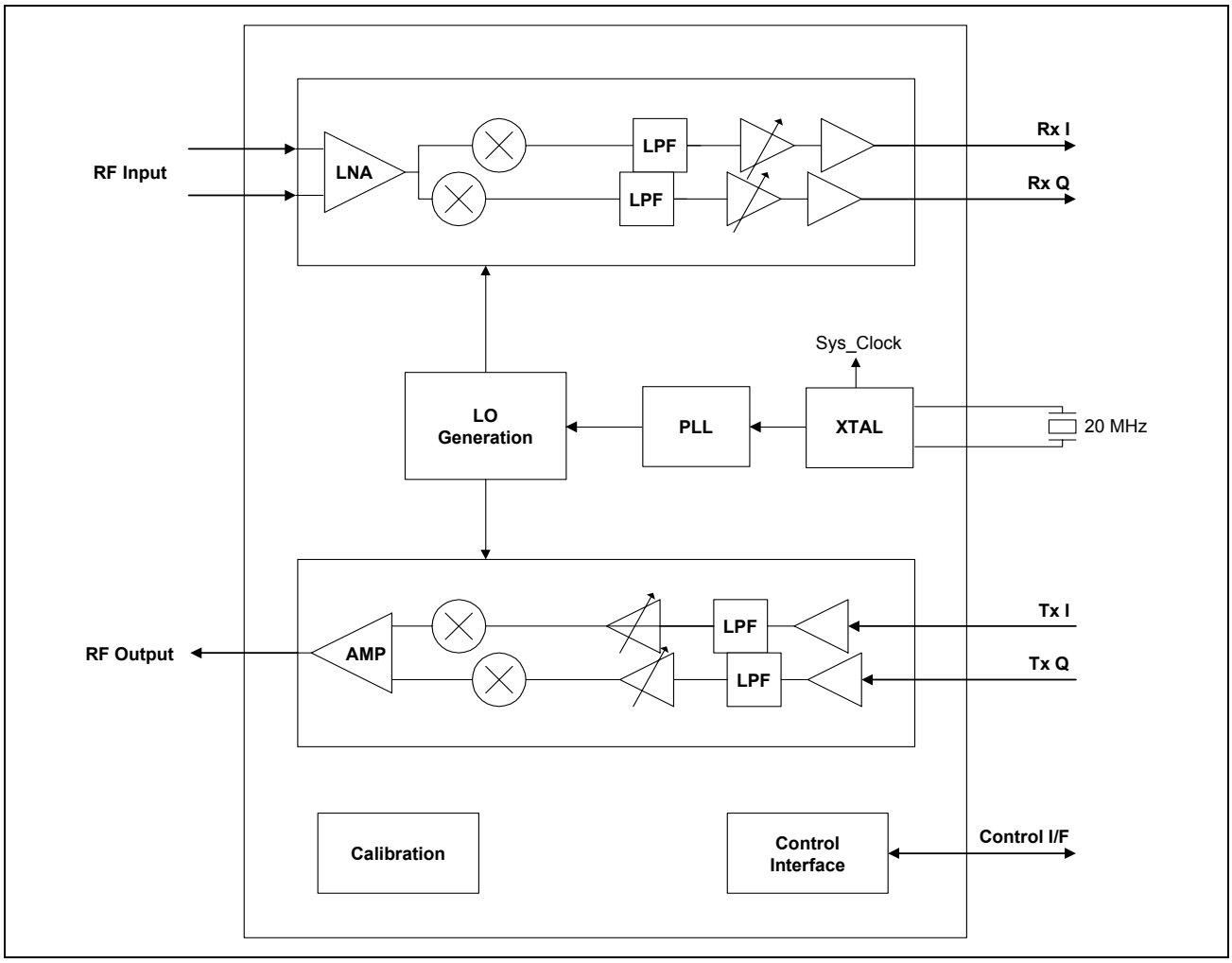


Figure 4: Radio Functional Block Diagram

RECEIVER PATH

The BCM4318/BCM4318E have a wide dynamic range, direct conversion receiver. The chip employs high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4-GHz ISM band. The excellent noise figure of the receiver makes an external LNA unnecessary.

Leading-edge Encore DSP technology is included on BCM4318E for improved receive sensitivity and extended range, enabling whole home coverage.

TRANSMITTER PATH

The BCM4318/BCM4318E include a linear transmitter capable of delivering up to +6 dBm while meeting the IEEE 802.11g specification. The output power is adjustable in 0.6-dB steps, down to –15 dBm. Baseband data is up-converted directly to the 2.4-GHz ISM band.

CALIBRATION

The BCM4318/BCM4318E feature on-chip calibration, eliminating process variation across components. This enables the device to be used in high-volume applications because calibration routines are not required during manufacturing test. These calibration routines are performed periodically in the course of normal radio operation. An example of this is automatic calibration of the baseband filters for optimum transmit and receive performance.

CRYSTAL OSCILLATOR

The recommended configuration for the crystal oscillator including all external components is shown in Figure 5.

Table 2: 20-MHz Crystal Requirements

Parameter	*Value*
Frequency	20.000 MHz
Mode	AT cut, fundamental
Load capacitance	16 pF
ESR	50Ω maximum
Frequency stability	±10 ppm at 25°C
	±10 ppm 0°C to +85°C
Aging	±3 ppm/year max first year, ±1 ppm thereafter
Drive level	300 µW maximum
Q-factor	40,000 minimum
Shunt capacitance	< 5 pf

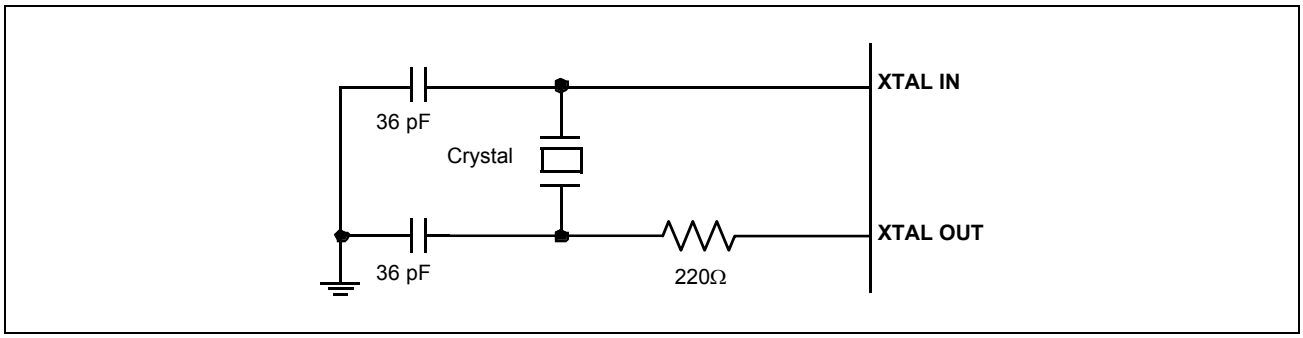


Figure 5: Recommended Oscillator Configuration

Section 2: Pin Assignments

144-PIN BGA ASSIGNMENTS

Figure 6 and Table 3 show the pin assignments for the 144-pin BGA device.

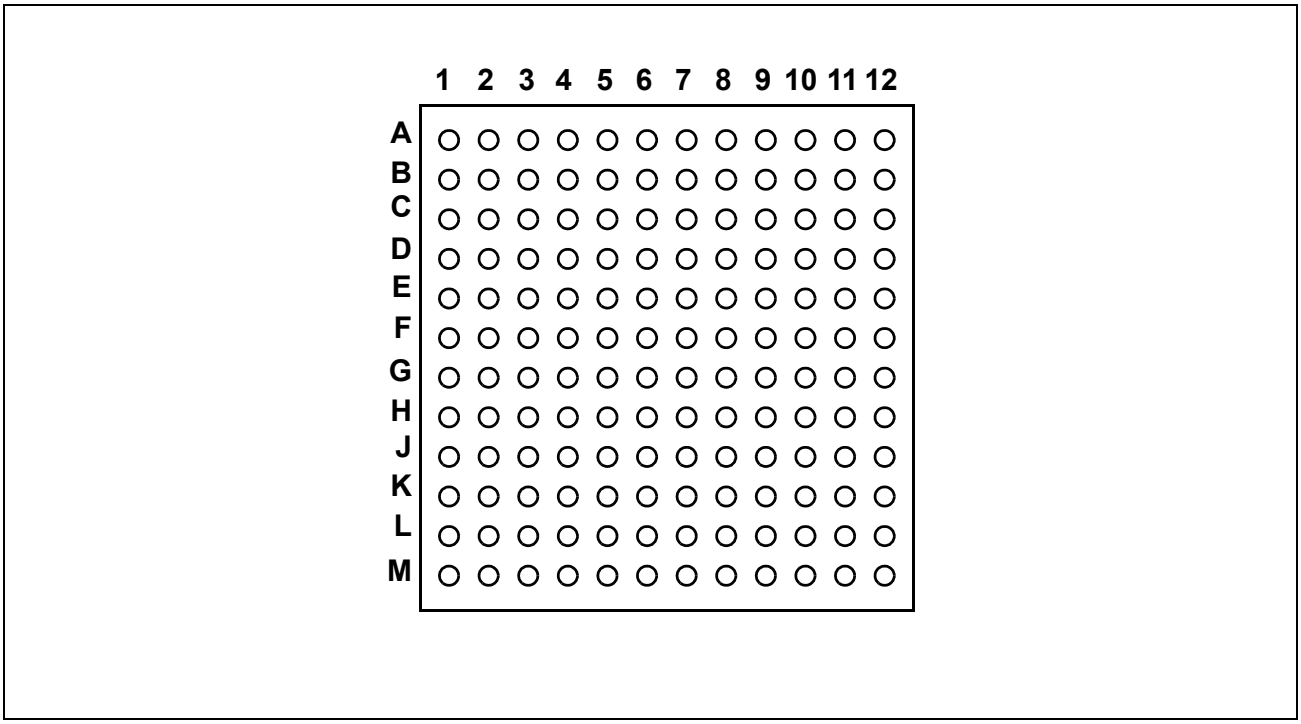


Figure 6: BCM4318/BCM4318E 144-Pin Top View Assignments

Table 3: 144-Pin Assignments

Pin	*Name*	*Pin*	*Name*	*Pin*	*Name*	*Pin*	*Name*
A1	RESERVED	B1	RESERVED	C1	XTSSI2	D1	RESERVED
A2	AVDD_DAC	B2	AVSS_DAC	C2	RESERVED	D2	RESERVED
A3	TDO	B3	PLLGND	C3	RESERVED	D3	RESERVED
A4	TCK	B4	$\overline{\text{EXT\_POR}}$	C4	RESERVED	D4	RESERVED
A5	$\overline{\text{RF\_DISABLE}}$	B5	TR_SW_RX_PU	C5	RX_PU	D5	RESERVED
A6	VDDIO	B6	GPHY_EXT_LNA_ GAIN	C6	TEST_SE	D6	ANT_SELP
A7	SPROM_CLK	B7	SPROM_DOUT	C7	SPROM_DIN	D7	ANT_SELN
A8	VDDIO	B8	VSS	C8	SPROM_CS	D8	SDIO_CLK
A9	SDIO_DATA_3	B9	SDIO_DATA_2	C9	SDIO_CMD	D9	D12

Table 3: 144-Pin Assignments (Cont.)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A10	SDIO_DATA_0	B10	D4	C10	$\overline{\text{IREQ}}$	D10	D6
A11	VDD	B11	D5	C11	D15	D11	VSS
A12	D11	B12	D13	C12	A10	D12	A11
E1	RGND	F1	RGND	G1	LNAINP	H1	LNAINN
E2	RGND	F2	VDDLF	G2	VDDRX	H2	RGND
E3	RGND	F3	RGND	G3	RGND	H3	RGND
E4	AVDD_ADC	F4	AVSS_ADC	G4	VSS	H4	VSS
E5	TDI	F5	$\overline{\text{JTAG\_TRST}}$	G5	PLLDVDD	H5	VSS
E6	TMS	F6	TR_SW_TX_PU	G6	GPIO_1	H6	VDD
E7	SDIO_DATA_1	F7	TX_PU	G7	D14	H7	GPIO_0
E8	D3	F8	VDDBUS	G8	GPIO_4	H8	GPIO_2
E9	D7	F9	$\overline{\text{CE0}}$	G9	A2	H9	VDDBUS
E10	$\overline{\text{CE1}}$	F10	A8	G10	A6	H10	A3
E11	$\overline{\text{OE}}$	F11	A7	G11	D2	H11	A4
E12	A9	F12	$\overline{\text{WAIT}}$	G12	A5	H12	$\overline{\text{REG}}$
J1	RGND	K1	VDDPA	L1	PA_OUT	M1	BGREF
J2	GNDPA	K2	VDDPA	L2	VDDDR	M2	VDDTX
J3	RGND	K3	GNDPA	L3	RGND	M3	VDDLO
J4	RGND	K4	RGND	L4	CP_FB	M4	RGND
J5	RGND	K5	VDDVCO	L5	VDDPLL	M5	XTALOUT
J6	RGND	K6	VDDPLL_REF	L6	VDDCP	M6	XTALIN
J7	RGND	K7	VDD4W	L7	VDDXTAL	M7	RGND
J8	RGND	K8	RGND	L8	RGND	M8	RGND
J9	A1	K9	GPIO_5	L9	VDD	M9	GPIO_3
J10	A0	K10	RESET	L10	VDDIO	M10	OTP_VDD
J11	D8	K11	$\overline{\text{INPACK}}$	L11	D10	M11	XTAL_PU
J12	D0	K12	D1	L12	D9	M12	$\overline{\text{WE}}$

196-PIN BGA ASSIGNMENTS

Figure 7 and Table 4 show the pin assignments for the 196-pin BGA device.

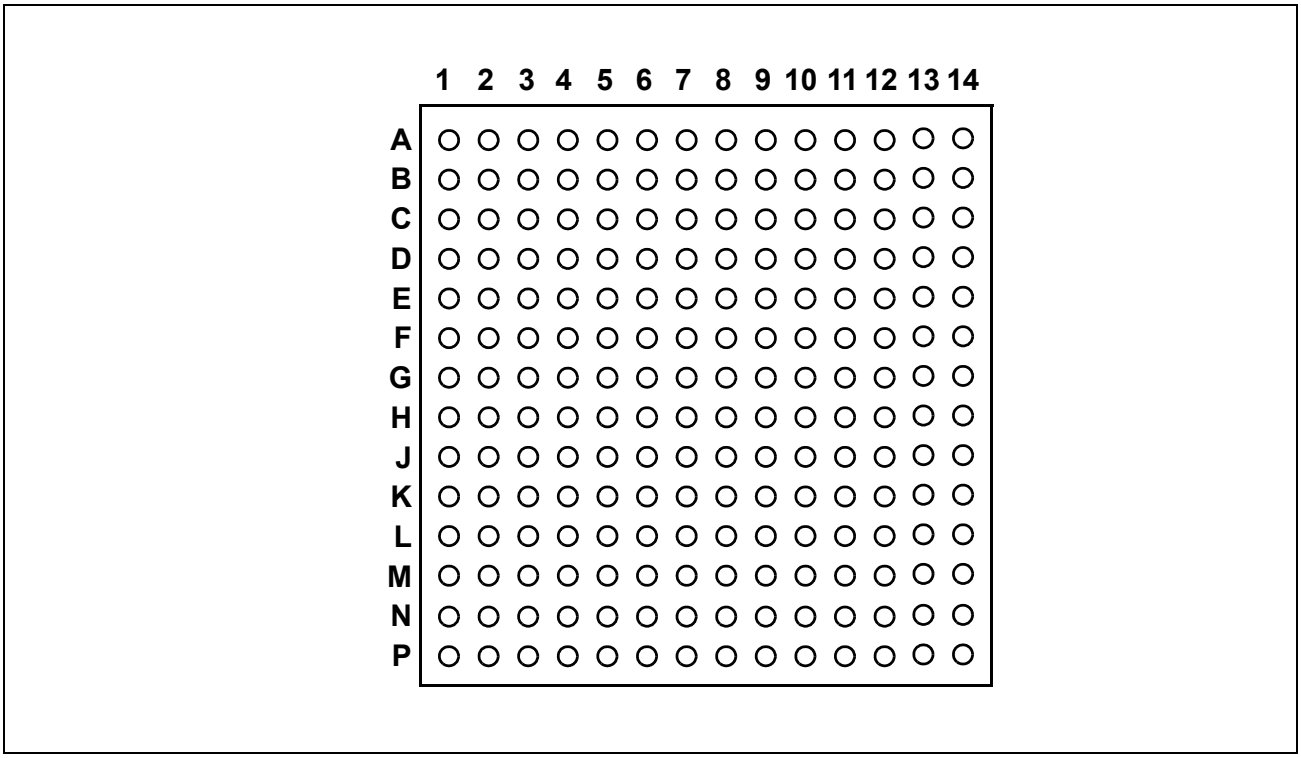


Figure 7: BCM4318/BCM4318E 196-Pin Top View Assignments

Table 4: 196-Pin Assignments

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	AVSS_DAC	B1	AVDD_DAC	C1	TXP_Q	D1	TXN_I
A2	FREF_2	B2	XTEMPRSSI	C2	TXN_Q	D2	TXP_I
A3	PLLGND	B3	PLLDVDD	C3	JTAG_TRST	D3	XNRSSI
A4	RX_PU	B4	TMS	C4	TCK	D4	XTSSI2
A5	PLLVDD	B5	TDI	C5	EXT_POR	D5	ANT_SELN
A6	TDO	B6	TR_SW_RX_PU	C6	TR_SW_TX_PU	D6	APHY_PA_PD
A7	TEST_SE	B7	ANT_SELP	C7	APHY_PA_CNTRL_0	D7	APHY_EXT_LNA_GAIN
A8	RF_DISABLE	B8	GPHY_EXT_LNA_GAIN	C8	APHY_SRI_E	D8	APHY_EXT_LNA_PU
A9	TX_PU	B9	APHY_SRI_DI	C9	APHY_SRI_DO	D9	SDIO_DATA_3/ UART_TX
A10	APHY_SYNTH_PU	B10	SPROM_DIN	C10	SDIO_DATA_1/ UART_DCD	D10	CSTSCHG
A11	APHY_SRI_C	B11	SPROM_CS	C11	PCI_INT	D11	PCI_AD_2
A12	SPROM_DOUT	B12	SDIO_DATA_0/ UART_CTS	C12	PCI_AD_5	D12	PCI_AD_4
A13	SDIO_DATA_2/ UART_DTR	B13	SDIO_CMD/ UART_RTS	C13	PCI_AD_6	D13	PCI_AD_7
A14	PCI_AD_0	B14	PCI_AD_1	C14	PCI_AD_3	D14	PCI_CBE_0
E1	XWRSSI	F1	RESERVED	G1	RGND	H1	RGND
E2	XTSSI5	F2	RESERVED	G2	RGND	H2	VDDLF
E3	AVDD_ADC	F3	RXP_I	G3	RGND	H3	RGND
E4	AVSS_ADC	F4	RXN_I	G4	RXN_Q	H4	RXP_Q
E5	UART_RX	F5	CMOUT	G5	VDDBUS	H5	VDDBUS
E6	VDD	F6	UART_RI	G6	VSS	H6	VSS
E7	UART_DSR	F7	VSS	G7	VSS	H7	VSS
E8	VDD	F8	VSS	G8	VSS	H8	VSS
E9	SPROM_CLK	F9	VSS	G9	VSS	H9	VSS
E10	SDIO_CLK/ UART_CLK	F10	PCI_AD_14	G10	PCI_AD_15	H10	PCI_AD_16
E11	VESD	F11	PCI_AD_11	G11	PCI_CBE_1	H11	PCI_CBE_2
E12	PCI_AD_10	F12	PCI_AD_13	G12	PCI_PERR	H12	PCI_TRDY
E13	PCI_AD_9	F13	PCI_PAR	G13	PCI_STOP	H13	PCI_CLK
E14	PCI_AD_8	F14	PCI_AD_12	G14	PCI_SERR	H14	PCI_DEVSEL

Table 4: 196-Pin Assignments (Cont.)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
J1	LNAINP	K1	LNAINN	L1	RGND	M1	VDDPA
J2	VDDRX	K2	RGND	L2	GNDPA	M2	VDDPA
J3	RGND	K3	RGND	L3	RGND	M3	GNDPA
J4	VDDBUS	K4	VDDIO	L4	RGND	M4	RGND
J5	VDDBUS	K5	VDDIO	L5	RGND	M5	VDDVCO
J6	VSS	K6	VDDIO	L6	RGND	M6	VDDPLL_REF
J7	VSS	K7	VDDIO	L7	RGND	M7	VDD4W
J8	GPIO_1	K8	GPIO_0	L8	RGND	M8	RGND
J9	VSS	K9	GPIO_6	L9	GPIO_5	M9	GPIO_2
J10	VSS	K10	$\overline{\text{PCI\_RST}}$	L10	OTP_VDD	M10	GPIO_7
J11	PCI_AD_17	K11	VDD	L11	PCI_AD_28	M11	$\overline{\text{PCI\_GNT}}$
J12	$\overline{\text{PCI\_FRAME}}$	K12	PCI_AD_20	L12	PCI_AD_23	M12	PCI_AD_24
J13	PCI_AD_18	K13	PCI_AD_21	L13	PCI_IDSEL	M13	PCI_AD_26
J14	$\overline{\text{PCI\_IRDY}}$	K14	PCI_AD_19	L14	PCI_AD_22	M14	$\overline{\text{PCI\_CBE\_3}}$

N1	PA_OUT	P1	BGREF
N2	VDDDR	P2	VDDTX
N3	RGND	P3	VDDLO
N4	CP_FB	P4	RGND
N5	VDDPLL	P5	XTALOUT
N6	VDDCP	P6	XTALIN
N7	VDDXTAL	P7	RGND
N8	RGND	P8	RGND
N9	GPIO_4	P9	GPIO_3
N10	PCMCIA_SEL	P10	XTAL_PU
N11	$\overline{\text{PCI\_CLKRUN}}$	P11	$\overline{\text{PCI\_PME}}$
N12	$\overline{\text{PCI\_REQ}}$	P12	PCI_AD_31
N13	PCI_AD_29	P13	PCI_AD_30
N14	PCI_AD_25	P14	PCI_AD_27

Section 3: Signal Descriptions

The signal name, type, and description of each pin in the BCM4318/BCM4318E 144-pin FBGA package are listed in Table 5. The symbols shown under *Type* indicate pin directions (*I/O = bidirectional*, *I = input, O = output*) and the internal pull-up/ pull-down characteristics (*PU = weak internal pull-up resistor* and *PD = weak internal pull-down resistor*), if any. See also Table 8 on page 31 for resistor strapping options.

144-Pin BGA Descriptions

Table 5: BCM4318/BCM4318E 144-Pin BGA Signal Descriptions

Signal Name	*Pin*	*Type*	*Description*
PCMCIA/Compact Flash			
D0	J12	In/Out (16 mA)	PCMCIA/Compact Flash Data Bus.
D1	K12	In/Out (16 mA)	
D2	G11	In/Out (16 mA)	
D3	E08	In/Out (16 mA)	
D4	B10	In/Out (16 mA)	
D5	B11	In/Out (16 mA)	
D6	D10	In/Out (16 mA)	
D7	E09	In/Out (16 mA)	
D8	J11	In/Out (16 mA)	
D9	L12	In/Out (16 mA)	
D10	L11	In/Out (16 mA)	
D11	A12	In/Out (16 mA)	
D12	D09	In/Out (16 mA)	
D13	B12	In/Out (16 mA)	
D14	G07	In/Out (16 mA)	
D15	C11	In/Out (16 mA)	

Table 5: BCM4318/BCM4318E 144-Pin BGA Signal Descriptions (Cont.)

Signal Name	*Pin*	*Type*	*Description*
A0	J10	In	PCMCIA/Compact Flash Address Bus.
A1	J09	In	
A2	G09	In	
A3	H10	In	
A4	H11	In	
A5	G12	In	
A6	G10	In	
A7	F11	In	
A8	F10	In	
A9	E12	In	
A10	C12	In	
A11	D12	In	
$\overline{\text{IREQ}}$	C10	Out (16 mA)	**Interrupt Request.** Asserted by the BCM4318/BCM4318E to indicate to the host system that the BCM4318/BCM4318E requires host software service. The interrupt signal at the interface is routed by the system to one of the interrupt request signals on the system's internal bus. The signal is negated when no interrupt is requested.
$\overline{\text{CE0}}$	F09	In	**Card Enable.** The CE0 input enables even-numbered address bytes, and CE1 enables odd-numbered address bytes. A multiplexing scheme based on A0 and CE0 allows 8-bit hosts to access all data on D[7:0], if desired. The Card Enable pins are used to access both Common and Attribute Memory and to access I/O.
$\overline{\text{CE1}}$	E10	In	
$\overline{\text{OE}}$	E11	In	**Output Enable.** Used to gate Memory Read data from memory. Hosts must negate the OE signal during write operations.
$\overline{\text{WAIT}}$	F12	Out (16 mA)	**Extend Bus Cycle**. Asserted to delay completion of the memory access or I/O access cycle then in progress. This pin is also sampled asynchronously at powerup to determine various bus modes. See Table 8 on page 31 for details.
$\overline{\text{REG}}$	H12	In	**Attribute Memory Select.** When this signal is asserted, access is limited to attribute memory. The REG signal is kept negated for all common memory accesses.
$\overline{\text{INPACK}}$	K11	Out (16 mA)	**Input Port Acknowledge.** Asserted when the device is selected and can respond to an I/O read cycle at the address on the address bus. This signal is used by the host to control the enable of any input data buffer between the card and the host system data bus. This signal must be inactive until the card is configured.
$\overline{\text{WE}}$	M12	In	**Write Enable.** Used for strobing Memory Write data into memory.
RESET	K10	In	**Card Reset.** Clears the Configuration Option register, placing the device in an unconfigured (Memory Only interface) state. It also signals the beginning of any additional card initialization. The system must place the RESET signal in a High-Z state during card powerup. The signal must remain high-impedance for at least 1 ms after VDDBUS becomes valid.

Table 5: BCM4318/BCM4318E 144-Pin BGA Signal Descriptions (Cont.)

Signal Name	Pin	Type	Description
SDIO Bus Interface			
SDIO_DATA_0	A10	In/Out (8 mA) PU	**SDIO Data line 0** (see Table 9 on page 31).
SDIO_DATA_1	E07	In/Out (8 mA) PU	**SDIO Data line 1** (see Table 9 on page 31).
SDIO_DATA_2	B09	In/Out (8 mA) PU	**SDIO Data line 2** (see Table 9 on page 31).
SDIO_DATA_3	A09	In/Out (8 mA) PU	**SDIO Data line 3** (see Table 9 on page 31).
SDIO_CLK	D08	In PU	**SDIO Clock** (see Table 9 on page 31).
SDIO_CMD	C09	In/Out (8 mA) PU	**SDIO Command Line** (see Table 9 on page 31).
SPROM Bus Interface			
SPROM_DIN	C07	In PD	**SPROM Data In.** Must be connected to the DOUT signal of the SPROM. This pin is also used as a strapping option to determine SPROM mode. See Table 7 on page 30 for details.
SPROM_DOUT	B07	In/Out (4 mA) PD	**SPROM Data Out.** Must be connected to the DIN signal of the SPROM (see note below). This pin is also used as a strapping option to determine SPROM mode. See Table 7 on page 30 for details.
SPROM_CLK	A07	In/Out (4 mA) PD	**Serial Data Clock.** Must be connected to the serial clock input of the SPROM (typically called SK). This pin is also used as a strapping option to determine SPROM mode. See Table 7 on page 30 for details.
SPROM_CS	C08	Out (4 mA) PU	**SPROM Chip Select.** Must be connected to the chip select input of the SPROM (typically called CS). This pin is also used as a strapping option to determine SPROM mode. See Table 7 on page 30 for details.
JTAG Interface			
TMS	E06	In PU	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, these pins can be left unconnected (NC), as they have internal pull-ups. TCK is typically an 8-MHz clock
TCK	A04	In PU	
TDI	E05	In PU	
TDO	A03	Out (8 mA) PU	
$\overline{\text{JTAG\_TRST}}$	F05	PU	
GPIO Interface			
GPIO_0	H07	In/Out (8 mA)	**General Purpose Interface Pins.** These pins are High-Z on powerup and reset. Subsequently, they become inputs or outputs through software control.
GPIO_1	G06	In/Out (8 mA)	
GPIO_2	H08	In/Out (8 mA)	
GPIO_3	M09	In/Out (8 mA)	
GPIO_4	G08	In/Out (8 mA)	
GPIO_5	K09	In/Out (8 mA)	
Crystal Oscillator			
XTALOUT	M05		**20-MHz XTAL output.**
XTALIN	M06		**20-MHz XTAL input**.

Table 5: BCM4318/BCM4318E 144-Pin BGA Signal Descriptions (Cont.)

Signal Name	Pin	Type	Description
Misc. Control			
BGREF	M01		**Bandgap reference.** Connect to GND through an external 2.87-kΩ resistor.
CP_FB	L04		**Feedback Filter.** Refer to reference design.
$\overline{\text{EXT\_POR}}$	B04	PU	**External Power-on Reset.** Allows connection of the external power-on reset circuit. The internal POR can be used as the default without requiring an external circuit. EXT_POR must be left open for normal operation.
$\overline{\text{RF\_DISABLE}}$	A05	PU	**Radio Disable.** Asserting this pin low disables the internal 2.4-GHz radio by shutting off everything (including the synthesizer) in the radio other than the oscillator.
TEST_SE	C06	PU	**Scan Enable Input.** No Connect (NC).
XTAL_PU	M11		**XTAL Powerup.** Pull high for normal operation.
Reserved Signals			
RESERVED	A01		No Connect (NC).
RESERVED	B01		No Connect (NC).
RESERVED	C02		No Connect (NC).
RESERVED	C03		No Connect (NC).
RESERVED	C04		No Connect (NC).
RESERVED	D01		No Connect (NC).
RESERVED	D02		No Connect (NC).
RESERVED	D03		No Connect (NC).
RESERVED	D04		No Connect (NC).
RESERVED	D05		No Connect (NC)
2.4-GHz RF Analog Interface (IEEE 802.11g)			
ANT_SELN	D07	Out (12 mA)	**Antenna Select Negative.** Used to drive a diversity switch to select which of the two antennas should be currently in use (for switched diversity operation). ANT_SELN is the inverse of ANT_SELP.
ANT_SELP	D06	Out (12 mA)	**Antenna Select Positive.** Used to drive a diversity switch to select which of the two antennas should be currently in use (for switched diversity operation).
GPHY_EXT_LNA_GAIN	B06	Out (12 mA)	**External LNA gain control.**
LNAINN	H01	In	**LNA Differential Input.**
LNAINP	G01	In	**LNA Differential Input.**
PA_OUT	L01	Out	2.4-GHz Transmitter Output. Output frequency = 2402–2495 MHz.
TR_SW_RX_PU	B05	Out (12 mA)	**Receive Powerup Control Output for External TR Switch.**
TR_SW_TX_PU	F06	Out (12 mA)	**Transmit Powerup Control Output for External TR Switch.**
TX_PU	F07	Out (12 mA)	**External Power Amplifier Powerup.**
XTSSI2	C01	In	**2.4-GHz Transmit Signal Strength Indicator.**
RX_PU	C05	Out (8 mA)	**External LNA Powerup.**

Table 5: BCM4318/BCM4318E 144-Pin BGA Signal Descriptions (Cont.)

Signal Name	Pin	Type	Description
3.3V Digital			
OTP_VDD	M10		Connect to 3.3V digital supply.
VDDBUS	F08		
VDDBUS	H09		
VDDIO	A06		
VDDIO	A08		
VDDIO	L10		
1.8V Analog VDD Filter Group 1			
AVDD_ADC	E04		Connect this group of pins to a separately filtered 1.8V supply.
AVDD_DAC	A02		
PLLDVDD	G05		
1.8V Analog VDD Filter Group 2			
VDD4W	K07		Connect this group of pins to a separately filtered 1.8V supply.
VDDPLL	L05		
VDDPLL_REF	K06		
VDDXTAL	L07		
1.8V Analog VDD Filter Group 3			
VDDCP	L06		Connect this group of pins to a separately filtered 1.8V supply.
VDDLF	F02		
VDDLO	M03		
VDDVCO	K05		
1.8V Analog VDD Filter Group 4			
VDDDR	L02		Connect this group of pins to a separately filtered 1.8V supply.
VDDRX	G02		
VDDTX	M02		
VDD 1.8V Digital			
VDD	A11		Connect to 1.8V digital supply.
VDD	H06		
VDD	L09		
1.8V Analog			
VDDPA	K01		Connect to filtered 1.8V supply.
VDDPA	K02		

Table 5: BCM4318/BCM4318E 144-Pin BGA Signal Descriptions (Cont.)

Signal Name	*Pin*	*Type*	*Description*
RF Ground			
GNDPA	J02		RF GND.
GNDPA	K03		
PLLGND	B03		
RGND	E01		
RGND	E02		
RGND	E03		
RGND	F01		
RGND	F03		
RGND	G03		
RGND	H02		
RGND	H03		
RGND	J01		
RGND	J03		
RGND	J04		
RGND	J05		
RGND	J06		
RGND	J07		
RGND	J08		
RGND	K04		
RGND	K08		
RGND	L03		
RGND	L08		
RGND	M04		
RGND	M07		
RGND	M08		
Digital Ground			
AVSS_ADC	F04		Digital GND.
AVSS_DAC	B02		
VSS	B08		
VSS	D11		
VSS	G04		
VSS	H04		
VSS	H05		

196-PIN BGA DESCRIPTIONS

The signal name, type, and description of each pin in the BCM4318/BCM4318E 196-pin FBGA package are listed in Table 6. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor, and PD = weak internal pull-down resistor), if any. See also Table 8 on page 31 for resistor strapping options.

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions

Signal Name	*Pin*	*Type*	*Description*
PCI Bus and CardBus Interface (supports connections to PCI and CardBus systems)			
PCI_AD_0	A14	In/Out (16 mA)	**Multiplexed 32-Bit Address and Data Lines**.
PCI_AD_1	B14	In/Out (16 mA)	
PCI_AD_2	D11	In/Out (16 mA)	
PCI_AD_3	C14	In/Out (16 mA)	
PCI_AD_4	D12	In/Out (16 mA)	
PCI_AD_5	C12	In/Out (16 mA)	
PCI_AD_6	C13	In/Out (16 mA)	
PCI_AD_7	D13	In/Out (16 mA)	
PCI_AD_8	E14	In/Out (16 mA)	
PCI_AD_9	E13	In/Out (16 mA)	
PCI_AD_10	E12	In/Out (16 mA)	
PCI_AD_11	F11	In/Out (16 mA)	
PCI_AD_12	F14	In/Out (16 mA)	
PCI_AD_13	F12	In/Out (16 mA)	
PCI_AD_14	F10	In/Out (16 mA)	
PCI_AD_15	G10	In/Out (16 mA)	
PCI_AD_16	H10	In/Out (16 mA)	
PCI_AD_17	J11	In/Out (16 mA)	
PCI_AD_18	J13	In/Out (16 mA)	
PCI_AD_19	K14	In/Out (16 mA)	
PCI_AD_20	K12	In/Out (16 mA)	
PCI_AD_21	K13	In/Out (16 mA)	
PCI_AD_22	L14	In/Out (16 mA)	
PCI_AD_23	L12	In/Out (16 mA)	
PCI_AD_24	M12	In/Out (16 mA)	
PCI_AD_25	N14	In/Out (16 mA)	
PCI_AD_26	M13	In/Out (16 mA)	
PCI_AD_27	P14	In/Out (16 mA)	
PCI_AD_28	L11	In/Out (16 mA)	
PCI_AD_29	N13	In/Out (16 mA)	

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions (Cont.)

Signal Name	*Pin*	*Type*	*Description*
PCI_AD_30	P13	In/Out (16 mA)	**Multiplexed 32-Bit Address and Data Lines**.
PCI_AD_31	P12	In/Out (16 mA)	
PCI_CBE_0	D14	In/Out (16 mA)	**Multiplexed Command/Byte Enables.**
PCI_CBE_1	G11	In/Out (16 mA)	
PCI_CBE_2	H11	In/Out (16 mA)	
PCI_CBE_3	M14	In/Out (16 mA)	
PCI_CLK	H13	In	**PCI Bus Clock.**
PCI_CLKRUN	N11	In/Out (16 mA)	As an input, this signal is driven low to indicate that PCI_CLK is running; deasserted to indicate a request to stop PCI_CLK. As an output, this signal is driven low to request that PCI_CLK continue running. Supports Mini PCI.
PCI_DEVSEL	H14	In/Out (16 mA)	Asserted when a device indicates it is the destination for the current bus cycle.
PCI_FRAME	J12	In/Out (16 mA)	**Cycle Framing Signal.**
PCI_GNT	M11	In	**Arbitration Signal Granting Access to the Bus.**
PCI_IDSEL	L13	In	Indicates that this device is the target of configuration bus cycles.
PCI_INT	C11	OD (16 mA)	**PCI INTA Interrupt Signal.**
PCI_IRDY	J14	In/Out (16 mA)	**Master Ready Signal.**
PCI_PAR	F13	In/Out (16 mA)	Even parity signal for PCI_AD[31:0] and PCI_CBE[3:0].
PCI_PERR	G12	In/Out (16 mA)	**Parity Error.**
PCI_PME	P11	OD (16 mA)	Used to request a change in the device or system power state. The assertion and deassertion of PCI_PME is asynchronous to PCI_CLK. This signal has an open-drain output structure as specified in the *PCI Bus Local Bus Specification*, Revision 2.2.
PCI_REQ	N12	In/Out (16 mA)	**Arbitration Signal Requesting Access to the Bus.**
PCI_RST/RESET	K10	In	**PCI Bus (System) Reset.** The pin becomes RESET for PC card when in PCMCIA mode. The system must place the RESET signal in a high-impedance state during card powerup. It must remain in high-impedance state for at least 1 ms after VDDBUS becomes valid.
PCI_SERR/WAIT	G14	In/Out (16 mA)	**PCI System Error** or **PCMCIA /WAIT**. In PCI mode, this pin becomes the System Error signal. In PCMCIA mode, this pin becomes the Extend Bus Cycle (wait). It is asserted by the device to delay completion of the memory or I/O access cycles when in progress. This pin is also used as a strapping option to determine various bus interface modes. See Table 8 on page 31 for details.
PCI_STOP	G13	In/Out (16 mA)	**Cycle Stop Signal.** Asserted by the Target for Retry, Disconnect, and Abort.
PCI_TRDY	H12	In/Out (16 mA)	**Target Ready Signal.**

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions (Cont.)

Signal Name	Pin	Type	Description
PCMCIA / Compact Flash (multifunction pins shared with PCI)			
D0	P14	In/Out (16 mA)	**PCMCIA/Compact Flash Data Bus.**
D1	N13	In/Out (16 mA)	
D2	J12	In/Out (16 mA)	
D3	A14	In/Out (16 mA)	
D4	B14	In/Out (16 mA)	
D5	C14	In/Out (16 mA)	
D6	C12	In/Out (16 mA)	
D7	D13	In/Out (16 mA)	
D8	L11	In/Out (16 mA)	
D9	P13	In/Out (16 mA)	
D10	P12	In/Out (16 mA)	
D11	D11	In/Out (16 mA)	
D12	D12	In/Out (16 mA)	
D13	C13	In/Out (16 mA)	
D14	G13	In/Out (16 mA)	
D15	E14	In/Out (16 mA)	
A0	M13	In	**PCMCIA/Compact Flash Address Bus.**
A1	N14	In	
A2	M12	In	
A3	L12	In	
A4	L14	In	
A5	K13	In	
A6	K12	In	
A7	J13	In	
A8	G11	In	
A9	F10	In	
A10	E13	In	
A11	F14	In	
A12	H11	In	
A13	F13	In	
A14	G12	In	
$\overline{\text{IREQ}}$	C11	Out (16 mA)	**Interrupt Request.** Asserted by the BCM4318/BCM4318E to indicate to the host system that the device requires host software service. The interrupt signal at the interface is routed by the system to one of the interrupt request signals on the system's internal bus. The signal is negated when no interrupt is requested.
PCMCIA_SEL	N10	In	**Bus Mode Select.** This pin is used as a strapping option to determine various bus interface modes. See Table 8 on page 31 for details.

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions (Cont.)

Signal Name	*Pin*	*Type*	*Description*
$\overline{CE0}$	D14	In	**Card Enable.** The CE0 input enables even-numbered address bytes, and CE1 enables odd-numbered address bytes. A multiplexing scheme based on A0 and CE0 allows 8-bit hosts to access all data on D[7:0], if desired. The Card Enable pins are used to access both Common and Attribute Memory and to access I/O.
$\overline{CE1}$	E12	In	
$\overline{OE}$	F11	In	**Output Enable.** Used to gate Memory Read data from memory. Hosts must negate the OE signal during write operations.
$\overline{REG}$	M14	In	**Attribute Memory Select.** When this signal is asserted, access is limited to attribute memory. The REG signal is kept negated for all common memory accesses.
$\overline{INPACK}$	N12	Out (16 mA)	**Input Port Acknowledge.** Asserted when the BCM4318/ BCM4318E is selected and can respond to an I/O read cycle at the address on the address bus. This signal is used by the host to control the enable of any input data buffer between the card and the host system data bus. This signal must be inactive until the card is configured.
$\overline{WE}$	M11	In	**Write Enable.** Used for strobing Memory Write data into memory.
WP	N11		**Write Protect.** Used to reflect the status of the Write Protect switch of the PC card. If the Write Protect switch is present, PCMCIA_WP is asserted by the card when the switch is enabled, and it is negated when the switch is disabled. If the memory card has no Write Protect switch, the card connects this line to VSS or VDDBUS, depending on the condition of the card memory.

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions (Cont.)

Signal Name	Pin	Type	Description
SDIO/UART Bus Interfaces			
SDIO_CLK/ UART_CLK[1]	E10	In PU	This pin has dual functions: • In SDIO mode, it becomes the **SDIO Clock** (see Table 9 on page 31). • In nonSDIO mode, it becomes the input from the **UART Clock**.
SDIO_CMD/ $\overline{\text{UART\_RTS}}$[1]	B13	In/Out (8 mA) PU	This pin has dual functions: • In SDIO mode, it becomes the **SDIO Command** line (see Table 9 on page 31). • In nonSDIO mode, it becomes the output for the **UART Request to Send** line.
SDIO_DATA_0/ $\overline{\text{UART\_CTS}}$[1]	B12	In/Out (8 mA) PU	This pin has dual functions: • In SDIO mode, it becomes **SDIO Data Line 0** (see Table 9 on page 31). • In nonSDIO mode, it becomes the **UART Clear to Send** line.
SDIO_DATA_1/ $\overline{\text{UART\_DCD}}$[1]	C10	In/Out (8 mA) PU	This pin has dual functions: • In SDIO mode, it becomes **SDIO Data Line 1** (see Table 9 on page 31)**.** • In nonSDIO mode, it becomes the **UART Data Carrier Detect** line.
SDIO_DATA_2/ $\overline{\text{UART\_DTR}}$[1]	A13	In/Out (8 mA) PU	This pin has dual functions: • In SDIO mode, it becomes **SDIO Data Line 2** (see Table 9 on page 31)**.** • In nonSDIO mode, it becomes the **UART Data Terminal Ready** line. This pin is also used as a strapping option to determine various bus interface modes. See Table 8 on page 31 for details.
SDIO_DATA_3/ UART_TX[1]	D09	In/Out (8 mA) (PU/PD)	This pin has dual functions: • In SDIO mode, it becomes **SDIO Data Line 3** (see Table 9 on page 31). • In nonSDIO mode, it becomes the output for the **UART Serial Transmitter** line. This pin is also used as a strapping option to select UART clock mode. See Table 8 on page 31 for details.
UART_RX[1,2]	E05	In (4 mA) PU	**UART Serial Input**
$\overline{\text{UART\_RI}}$[1,2]	F06	In (PU)	**UART Ring Indicator**
$\overline{\text{UART\_DSR}}$[1,2]	E07	In (PU)	**UART Data Set Ready**

Notes:
1. The UART option is only available on BCM4318E.
2. On BCM4318, pins E05, E07, and F06 have no internal connection.

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions (Cont.)

Signal Name	Pin	Type	Description
SPROM Bus Interface			
SPROM_DIN	B10	In PD	**SPROM Data In.** Must be connected to the DOUT signal of the SPROM. This pin is also used as a strapping option to determine SPROM mode. See Table 7 on page 30 for details.
SPROM_DOUT	A12	In/Out (4 mA) PD	**SPROM Data Out.** Must be connected to the DIN signal of the SPROM (see note below). This pin is also used as a strapping option to determine SPROM mode. See Table 7 on page 30 for details.
SPROM_CLK	E09	In/Out (4 mA) PD	**Serial Data Clock.** Must be connected to the serial clock input of the SPROM (typically called SK). This pin is also used as a strapping option to determine SPROM mode. See Table 7 on page 30 for details.
SPROM_CS	B11	Out (4 mA) PU	**SPROM Chip Select.** Must be connected to the chip select input of the SPROM (typically called CS). This pin is also used as a strapping option to determine SPROM mode. See Table 7 on page 30 for details.
JTAG Interface			
TMS	B04	In (PU)	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, these pins can be left unconnected (NC), as they have internal pull-ups. TCK is typically an 8-MHz clock.
TCK	C04	In PU	
TDI	B05	In PU	
TDO	A06	Out (8 mA) PU	
$\overline{\text{JTAG\_TRST}}$	C03	In PU	
GPIO Interface			
GPIO_0	K08	In/Out (8 mA)	**General Purpose Interface Pins.** These pins are High-Z on powerup and reset. Subsequently, they become inputs or outputs through software control.
GPIO_1	J08	In/Out (8 mA)	
GPIO_2	M09	In/Out (8 mA)	
GPIO_3	P09	In/Out (8 mA)	
GPIO_4	N09	In/Out (8 mA)	
GPIO_5	L09	In/Out (8 mA)	
GPIO_6	K09	In/Out (8 mA)	
GPIO_7	M10	In/Out (8 mA)	
Crystal Oscillator			
XTALOUT	P05		**20-MHz XTAL Output.**
XTALIN	P06		**20-MHz XTAL input**.
Misc. Control			
BGREF	P01		**Bandgap Reference.** Connect to GND through an external 2.87-kΩ resistor.
CP_FB	N04		**Feedback Filter.** Refer to reference design.
CSTSCHG	D10	Out	**Optional CardBus Interrupt.** Indicates a change in the status of the card. This pin is different from pin C11.
$\overline{\text{EXT\_POR}}$	C05	In (PU)	**External Power-on Reset.** Allows connection of the external power-on reset circuit. The internal POR can be used as the default without requiring an external circuit. $\overline{\text{EXT\_POR}}$ must be left open for normal operation.

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions (Cont.)

Signal Name	Pin	Type	Description
RF_DISABLE	A08	PU	**Radio Disable.** Asserting this pin low disables the BCM4318/ BCM4318E's internal 2.4-GHz radio and the BCM2060 5-GHz radio by shutting off everything (including the synthesizer) other than the oscillator.
TEST_SE	A07	PD	**Scan Enable Input.** No Connect (NC)
XTAL_PU	P10		**XTAL Powerup.** Pull high for normal operation.
Reserved Signals			
RESERVED	F01		No Connect (NC)
RESERVED	F02		No Connect (NC)
IEEE 802.11a Interface to BCM2060			
APHY_EXT_LNA_ GAIN	D07	Out (12 mA)	**External 5-GHz LNA gain control.**
APHY_EXT_LNA_PU	D08	Out (12 mA)	**External 5-GHz LNA powerup enable.**
APHY_PA_CNTRL_0	C07	NC	**Power Amplifier Control.** Power control signal to the BCM2060 radio. Leave unconnected.
APHY_PA_PD	D06	Out (12 mA)	**Power Amplifier Powerdown.**
APHY_SRI_C	A11	Out (4 mA)	**Serial Interface Clock.** Connected to the BCM2060 radio.
APHY_SRI_DI	B09	Out (4 mA)	**Data Output to the SRI_DI Pin on the BCM2060 IEEE 802.11a Radio Device.** Must be connected to the SRI_DI pin on the BCM2060 radio.
APHY_SRI_DO	C09	In	**Data Input from the SRI_DO Pin on the BCM2060 IEEE 802.11b/g Radio Device.** Must be connected to the SRI_DO pin on the BCM2060 radio.
APHY_SRI_E	C08	Out (4 mA)	**Serial Interface Enable.** Connected to the BCM2060 radio.
APHY_SYNTH_PU	A10		**Synthesizer Powerup.** Signal to the BCM2060 radio.
CMOUT	F05	Out	**Common Mode Voltage Output.** Sets the common mode input voltage of the ADC of the radio.
RXN_I	F04	In	**Receive Differential Input, In-Phase Negative Component from the BCM2060 Radio.**
RXN_Q	G04	In	**Receive Differential Input, Quadrature Negative Component from the BCM2060 Radio.**
RXP_I	F03	In	**Receive Differential Input, In-Phase Positive Component from the BCM2060 Radio.**
RXP_Q	H04	In	**Receive Differential Input, Quadrature Positive Component from the BCM2060 Radio.**
TXN_I	D01	Out	**Transmit Differential Output, In-Phase Negative Component to the BCM2060 Radio.**
TXN_Q	C02	Out	**Transmit Differential Output, Quadrature Negative Component to the BCM2060 Radio.**
TXP_I	D02	Out	**Transmit Differential Output, In-Phase Positive Component to the BCM2060 Radio.**
TXP_Q	C01	Out	**Transmit Differential Output, Quadrature Positive Component to the BCM2060 Radio.**
XNRSSI	D03	In	**Narrowband Receive Signal Strength Indicator.** Input signal from the BCM2060 radio.

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions (Cont.)

Signal Name	*Pin*	*Type*	*Description*
XTEMPRSSI	B02	In	**Broadcom Corporation Temperature Sense Input from the BCM2060 Radio.**
XTSSI5	E02	In	**Transmit Signal Strength Indication from the BCM2060 Radio.** If used, connect to the output power detector of the connected 5-GHz power amplifier. If not used, leave unconnected.
XWRSSI	E01	In	**Wideband Receive Signal Strength Indication from the BCM2060 Radio.**
FREF_2	A02	In	**Input Clock.** Reference clock from the BCM2060 radio.
Shared RF signals			
ANT_SELN	D05	Out (12 mA)	**Antenna Select Negative.** Used to drive a diversity switch to select which of the two antennas should be currently in use (for switched diversity operation). ANT_SELN is the inverse of ANT_SELP. This signal is shared and is used by both the 2.4-GHz (IEEE 802.11g) and 5-GHz (IEEE 802.11a) RF front ends.
ANT_SELP	B07	Out (12 mA)	**Antenna Select Positive.** Used to drive a diversity switch to select which of the two antennas should be currently in use (for switched diversity operation). This signal is shared and is used by both the 2.4-GHz (IEEE 802.11g) and 5-GHz (IEEE 802.11a) RF front ends.
TR_SW_RX_PU	B06	Out (12 mA)	**Receive Powerup Control Output for External TR Switch.** This signal is shared and is used by both the 2.4-GHz (IEEE 802.11g) and 5-GHz (IEEE 802.11a) RF front ends.
TR_SW_TX_PU	C06	Out (12 mA)	**Transmit Powerup Control Output for External TR Switch.** This signal is shared and is used by both the 2.4-GHz (IEEE 802.11g) and 5-GHz (IEEE 802.11a) RF front ends.
2.4-GHz RF Analog Interface (IEEE 802.11g)			
GPHY_EXT_LNA_GAIN	B08	Out (12 mA)	**External LNA Gain Control.**
LNAINN	K01	In	**LNA Differential Input.**
LNAINP	J01	In	**LNA Differential Input.**
PA_OUT	N01	Out	**2.4-GHz Transmitter Output.** Output frequency = 2402–2495 MHz.
XTSSI2	D04	In	**2.4-GHz Transmit Signal Strength Indicator.**
TX_PU	A09	Out (12 mA)	**External Power Amplifier Powerup Enable.**
RX_PU	A04	Out (8 mA)	**External LNA Powerup Enable.**
3.3V Digital			
OTP_VDD	L10		Connect to 3.3V digital supply.
VDDBUS	G05		
VDDBUS	H05		
VDDBUS	J04		
VDDBUS	J05		
VDDIO	K04		
VDDIO	K05		
VDDIO	K06		
VDDIO	K07		

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions (Cont.)

Signal Name	*Pin*	*Type*	*Description*
VESD	E11		**ESD Bias.** For a PCI bus, this pin should be connected to one of the VIO pins on the PCI connector (PCI pins A10, A16, A59, B19, or B59). For Mini PCI adapters, there are no VIO pins on the Mini PCI edge connector, so these pins should be connected to VDDBUS.
1.8V Analog VDD Filter Group 1			
AVDD_ADC	E03		Connect this group of pins to a separately filtered 1.8V supply.
AVDD_DAC	B01		
PLLVDD	A05		
PLLDVDD	B03		
1.8V Analog VDD Filter Group 2			
VDD4W	M07		Connect this group of pins to a separately filtered 1.8V supply.
VDDPLL	N05		
VDDPLL_REF	M06		
VDDXTAL	N07		
1.8V Analog VDD Filter Group 3			
VDDCP	N06		Connect this group of pins to a separately filtered 1.8V supply.
VDDLF	H02		
VDDLO	P03		
VDDVCO	M05		
1.8V Analog VDD Filter Group 4			
VDDDR	N02		Connect this group of pins to a separately filtered 1.8V supply.
VDDRX	J02		
VDDTX	P02		
VDD 1.8V Digital			
VDD	K11		Connect to 1.8V digital supply.
VDD	E06		
VDD	E08		
1.8V Analog			
VDDPA	M01		Connect to filtered 1.8V supply.
VDDPA	M02		

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions (Cont.)

Signal Name	Pin	Type	Description
RF Ground			
GNDPA	L02		RF GND.
GNDPA	M03		
PLLGND	A03		
RGND	G01		
RGND	G02		
RGND	G03		
RGND	H01		
RGND	H03		
RGND	J03		
RGND	K02		
RGND	K03		
RGND	L01		
RGND	L03		
RGND	L04		
RGND	L05		
RGND	L06		
RGND	L07		
RGND	L08		
RGND	M04		
RGND	M08		
RGND	N03		
RGND	N08		
RGND	P04		
RGND	P07		
RGND	P08		
Digital Ground			
AVSS_ADC	E04		Digital GND.
AVSS_DAC	A01		
VSS	F07		
VSS	F08		
VSS	F09		

Table 6: BCM4318/BCM4318E 196-Pin BGA Signal Descriptions (Cont.)

Signal Name	Pin	Type	Description
VSS	G06		Digital GND.
VSS	G07		
VSS	G08		
VSS	G09		
VSS	H06		
VSS	H07		
VSS	H08		
VSS	H09		
VSS	J06		
VSS	J07		
VSS	J09		
VSS	J10		

STRAPPING OPTIONS

The pins listed in Table 7 and Table 8 are asynchronously sampled at powerup to determine the various operating modes. Each pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU to VDDIO or PD to GND. Sampling occurs within a few milliseconds following internal POR or deassertion of external POR. After sampling, each pin assumes the function specified in the Signal Descriptions table, Table 5: "BCM4318/BCM4318E 144-Pin BGA Signal Descriptions," on page 14 or Table 6: "BCM4318/BCM4318E 196-Pin BGA Signal Descriptions," on page 20.

Table 7: SPROM Mode and Size

SPROM Mode—The SPROM pins are asynchronously sampled at powerup to determine SPROM mode and size. Mode is selected using the SPROM_CS and SPROM_DIN pins as follows:.		
SPROM_CS (also called CS) (PU)	**SPROM_DIN (PD)**	**Result**
0	0	SPROM present, normal operation
0	1	SPROM present, locked (no writes allowed)
1	0	Reserved
1	1	Host Mode—SPROM absent
SPROM Size—SPROM size is selected using the SPROM_CLK and SPROM_DOUT pins as follows:.		
SPROM_CLK (also called SK) (PD)	**SPROM_DOUT (PD)**	**Result**
1	0	16 kbit
0	1	4 kbit
0	0	1 kbit

Table 8: Bus Mode Configurations

Bus Mode	*PCMCIA_SEL*	*$\overline{\text{PCI\_SERR}}$*	*SDIO_DATA2 (PU)*
Mini/PCI	0	X	1
CardBus	0	X	0
SDIO	1	0	X
PCMCIA/Compact Flash	1	1	X

Note: X = do not care

SDIO PIN DESCRIPTIONS

Table 9: SDIO Pin Descriptions

SD 4-Bit Mode		*SD 1-Bit Mode*		*SPI Mode*	
SDIO_DATA_0	Data line 0	DATA	Data line	DO	Data output
SDIO_DATA_1	Data line 1 or Interrupt (optional)	IRQ	Interrupt	IRQ	Interrupt
SDIO_DATA_2	Data line 2 or Read Wait (optional)	RW	Read Wait (optional)	NC	Not used
SDIO_DATA_3	Data line 3	N/C	Not used	CS	Card Select
SDIO_CLK	Clock	CLK	Clock	SCLK	Clock
SDIO_CMD	Command line	CMD	Command line	DI	Data input

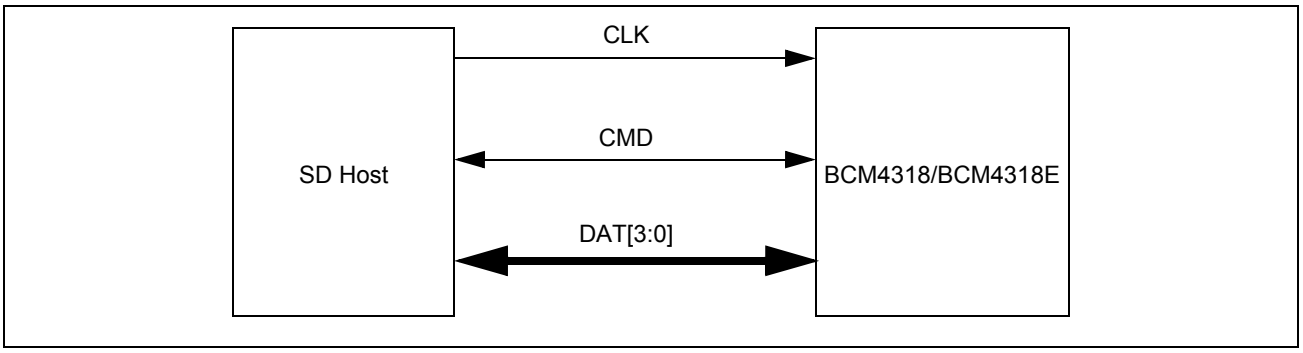


Figure 8: Signal Connections to SDIO Card (SD 4-Bit Mode)

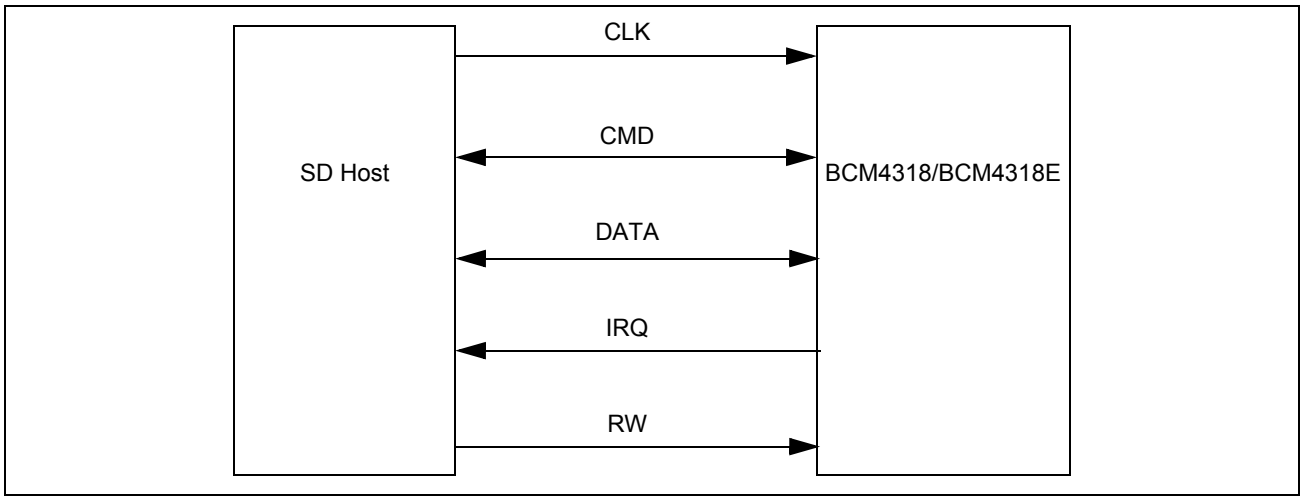


Figure 9: Signal Connections to SDIO Card (SD 1-Bit Mode)

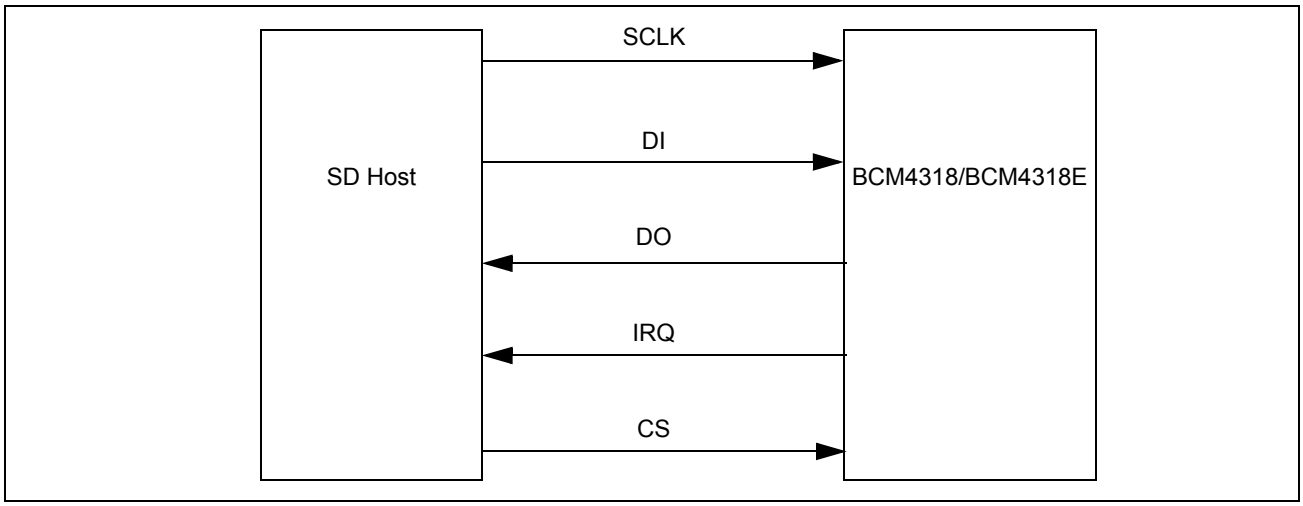


Figure 10: Signal Connections to SDIO Card (SPI Mode)

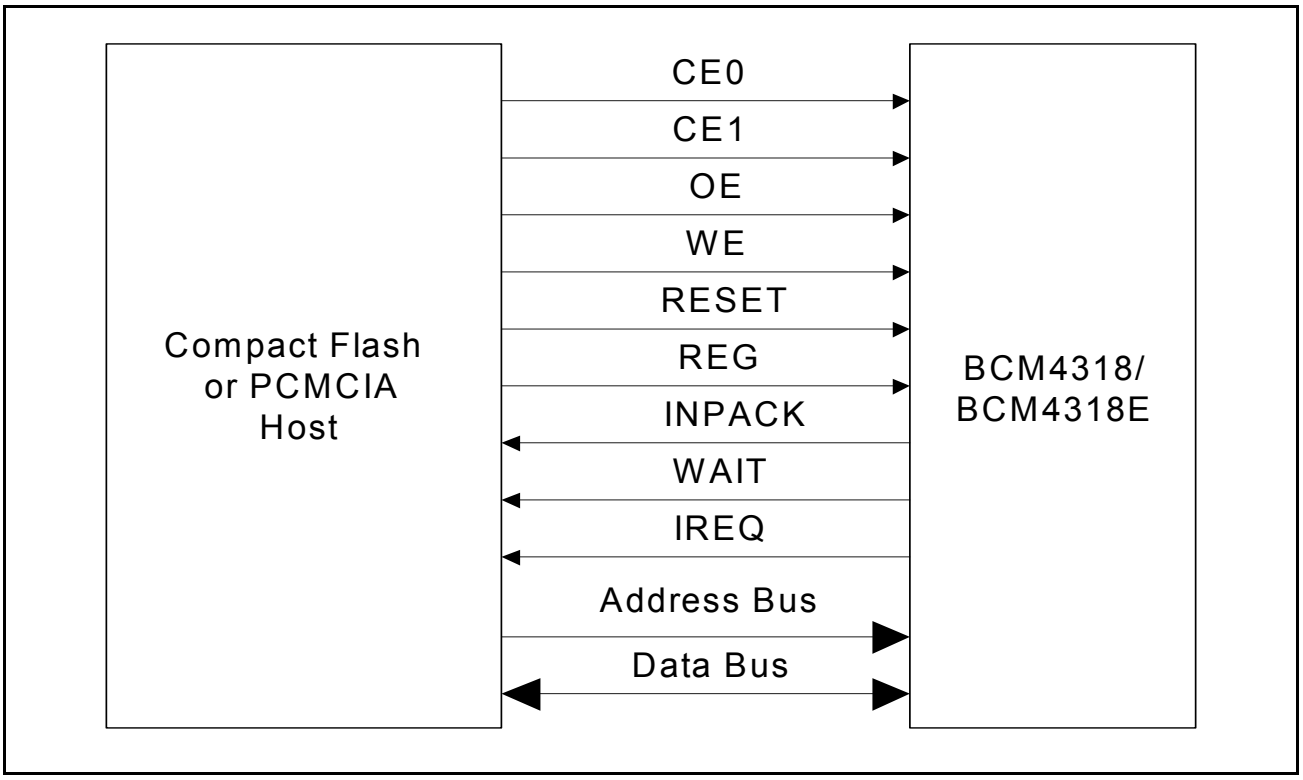


Figure 11: Signal Connections to PCMCIA/Compact Flash

Section 4: Electrical Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

RECOMMENDED OPERATING CONDITIONS

Table 10: Recommended Operating Conditions

Parameter	*Minimum*	*Typical*	*Maximum*	*Units*	*Conditions/Comments*
Supply Voltage					
• VDDIO, VDDBUS	3.0	3.3	3.6	V	
• VDDCORE, PLLVDD, AVDD	1.71	1.8	1.89	V	
Logic Inputs					
• V_{INH}, Input High Voltage	2.0			V	
• V_{INL}, Input Low Voltage			0.8	V	
Logic Outputs					
• V_{OH}, Output High Voltage	2.4			V	Current is determined by the specified pad.
• V_{OL}, Output Low Voltage			0.4	V	Current is determined by the specified pad.

CURRENT CONSUMPTION

Table 11: Current Consumption

Parameter	*Typical Average Current Consumption*	*Typical Peak Current Consumption*	*Units*
• 3.3V Supply—Total[a]	–	75	mA
• 1.8V Supply—Total[a]	–	320	mA
Receive			
• Receive (54 Mbps)—1.8V Supply[b]	TBD	–	mA
• Receive (54 Mbps)—3.3V Supply[b]	TBD	–	mA
• Receive (11 Mbps)—1.8V Supply[b]	TBD	–	mA
• Receive (11 Mbps)—3.3V Supply[b]	TBD	–	mA
Transmit			
• Transmit (54 Mbps)—1.8V Supply[b]	TBD	–	mA
• Transmit (54 Mbps)—3.3V Supply[b]	TBD	–	mA
• Transmit (11 Mbps)—1.8V Supply[b]	TBD	–	mA
• Transmit (11 Mbps)—3.3V Supply[b]	TBD	–	mA
Power Saving			
• Power Save Mode, 500 msec DTIM—1.8V Supply[c]	TBD	–	mA
• Power Save Mode, 500 msec DTIM—3.3V Supply[c]	TBD	–	mA

a. For use in power supply design considerations. Specified numbers are worst case values for worst case conditions: Vcc = 1.89V and 3.6V respectively, ambient temperature = 75°C, and absolute highest TX Output power (Internal attenuators forced to zero).

b. For use in battery life calculations. The values are typical average currents while a packet is being transmitted or received. The values do not represent average current over a specified time where there will be periods of no packets. For example, if the device is in power management mode and packets are only being transmitted/received 50% of the time over a period of time, the average current over that time span would be closer to 50% of the value shown above. In other words, real world typical power consumption will be lower than these values. These values are provided to make it easier to calculate time averaged current based on a target application's traffic characteristics. This only applies in power management mode. If the BCM4318/BCM4318E is not in power management mode then standby RX consumption is the same as consumption during packet reception. Also note that these numbers assume typical TX output power under the software driver's TX power control.

c. For use in battery life calculations. These values are for current averaged over a 5 second interval.

LOCAL OSCILLATOR SPECIFICATIONS

Table 12: Local Oscillator Specifications

Parameter	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
Reference Input Frequency Range	–	–	20	–	MHz
Clock Frequency Tolerance	–	–	–	±20	ppm
VCO Frequency Range	–	2412	–	2484	MHz
Reference Spurs	–	–	–	–34	dBc
Local Oscillator Phase Noise, single-sided from 1–300 kHz offset	–	–	–	–86.5	dBc/Hz

ENVIRONMENTAL CHARACTERISTICS

Table 13: Environmental Characteristics

Parameter	*Value*	*Units*	*Conditions/Comments*
Ambient Temperature (T_A)	0 to 75	°C	Operation
Storage Temperature	less than 30	°C	–
Relative Humidity	less than 60	%	Storage
	less than 85	%	Operation
ESD	+1 / –1.75	kV	Human Body Model

Section 5: RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

GENERAL RF SPECIFICATIONS

Table 14: General RF Specifications

Parameter	Condition	Minimum	Typical	Maximum	Unit
Tx/Rx Switch Time	Including Tx ramp down	–	5	10	µs
Rx/Tx Switch Time	Including Tx ramp up	–	5	5	µs

RECEIVER RF SPECIFICATIONS

Table 15: Receiver RF Specifications

Parameter	Condition	Minimum	Typical	Maximum	Unit
Cascaded Noise Figure		–	6	TBD	dB
Maximum Receive Level[a]	@ 1, 2 Mbps	–4	–	–	dBm
	@ 5.5, 11 Mbps	–10	–	–	dBm
	@ 54 Mbps	–10	–	–	dBm
Input IP3	Maximum Gain	–	–16	–	dBm
	Minimum Gain	–	–2	–	dBm
LPF 3-dB Bandwidth		8	8.5	9	MHz
PGA DC Rejection Servo Loop Bandwidth	WB Mode	–	1	–	MHz
	NB Mode	120 Hz	–	230 kHz	
LPF DC Rejection Servo Loop Bandwidth	WB Mode		500		kHz
	NB Mode	120 Hz	–	230 kHz	
Adjacent Channel Power Rejection	At 14-MHz offset	–	38	–	dBc
Alternate Channel Power Rejection	At 25-MHz offset	–	65	–	dBc
Maximum Receiver Gain		–	88	–	dB
Gain Control Step		–	3	–	dB/Step

a. When using a suitable external switch.

TRANSMITTER RF SPECIFICATIONS

Table 16: Transmitter RF Specifications

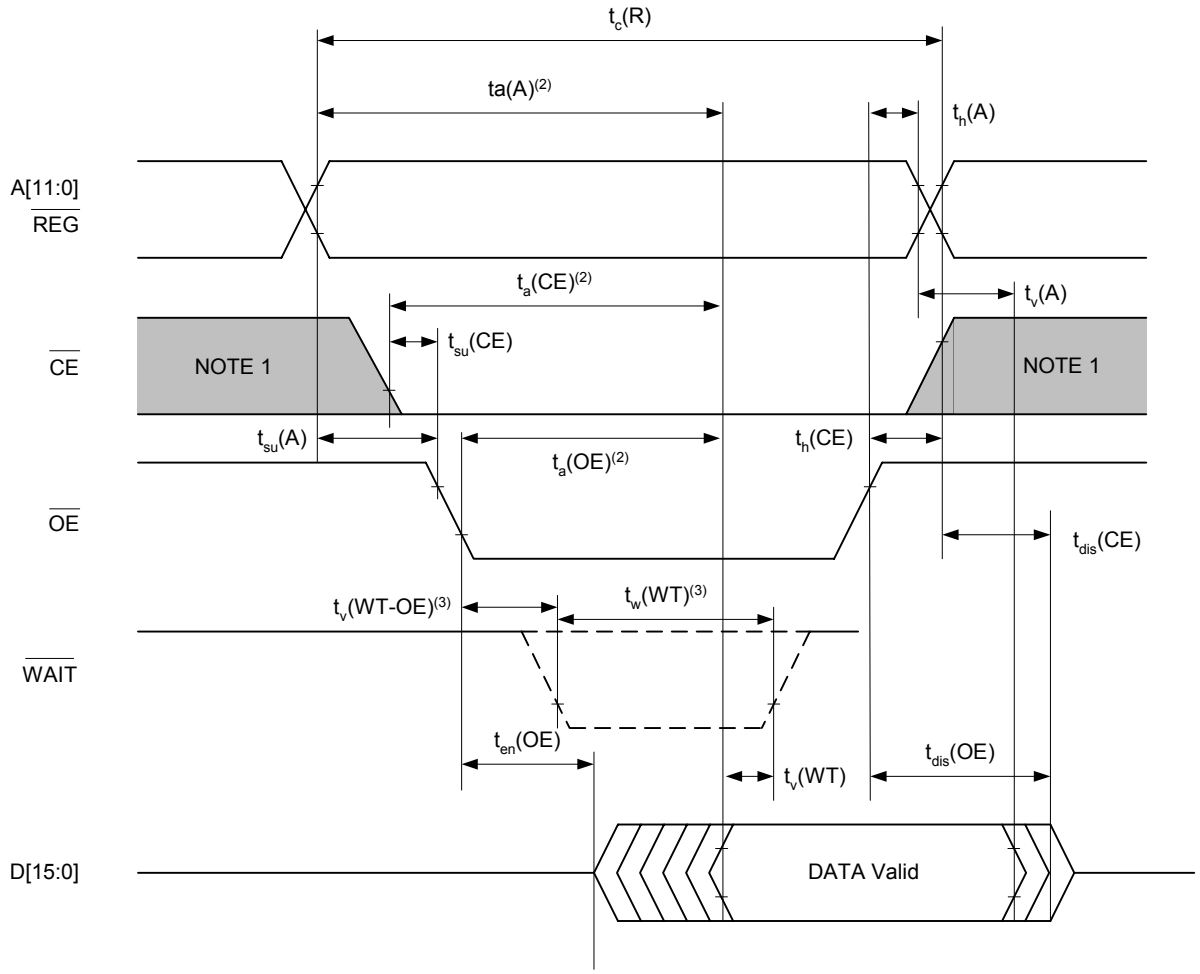
Parameter	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
RF Output Frequency Range		2400	–	2500	MHz
Output Power	Maximum Gain	–	+6	–	dBm
Gain Flatness	Maximum Gain	–	–	2	dB
Output IP3	Maximum Gain	–	+18	–	dBm
Output P1dB		–	+7	–	dBm
Output Power[a]	Minimum Gain	–	–15	–	dBm
Carrier Suppression		15	–	–	dBr
Tx Spectrum mask @ maximum gain	fc – 22MHz < f < fc – 11MHz	–	–	–30	dBr
	fc + 11MHz < f < fc + 22MHz	–	–	–30	dBr
	f < fc – 22MHz; and f > fc + 22MHz	–	–	–50	dBr
Tx Modulation Accuracy (EVM) @ maximum gain	802.11b mode	–		35%	
	802.11g mode			5%	
Gain Control Step Size		–	0.6	–	dB/step
I/Q Baseband Bandwidth	802.11b mode	7	8.5	–	MHz
	802.11g mode	–	15	–	MHz
Amplitude Balance[b]	DC Input	–1	–	1	dB
Phase Balance[b]	DC Input	–1.5	–	1.5	° (degrees)
Baseband Differential Input Voltage	Shaped Pulse	–	0.6	–	Vpp
Tx Power Ramp Up	90% of final Power	–	–	2	µsec
Tx Power Ramp Down	10% of final Power	–	–	2	µsec

a. IEEE 802.11(15.4.7.2) requires the minimum transmit power shall be no less than 1 mW at the antenna port.
b. At a 3 MHz offset from the carrier frequency.

Section 6: Timing Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

PCMCIA/COMPACT FLASH TIMING



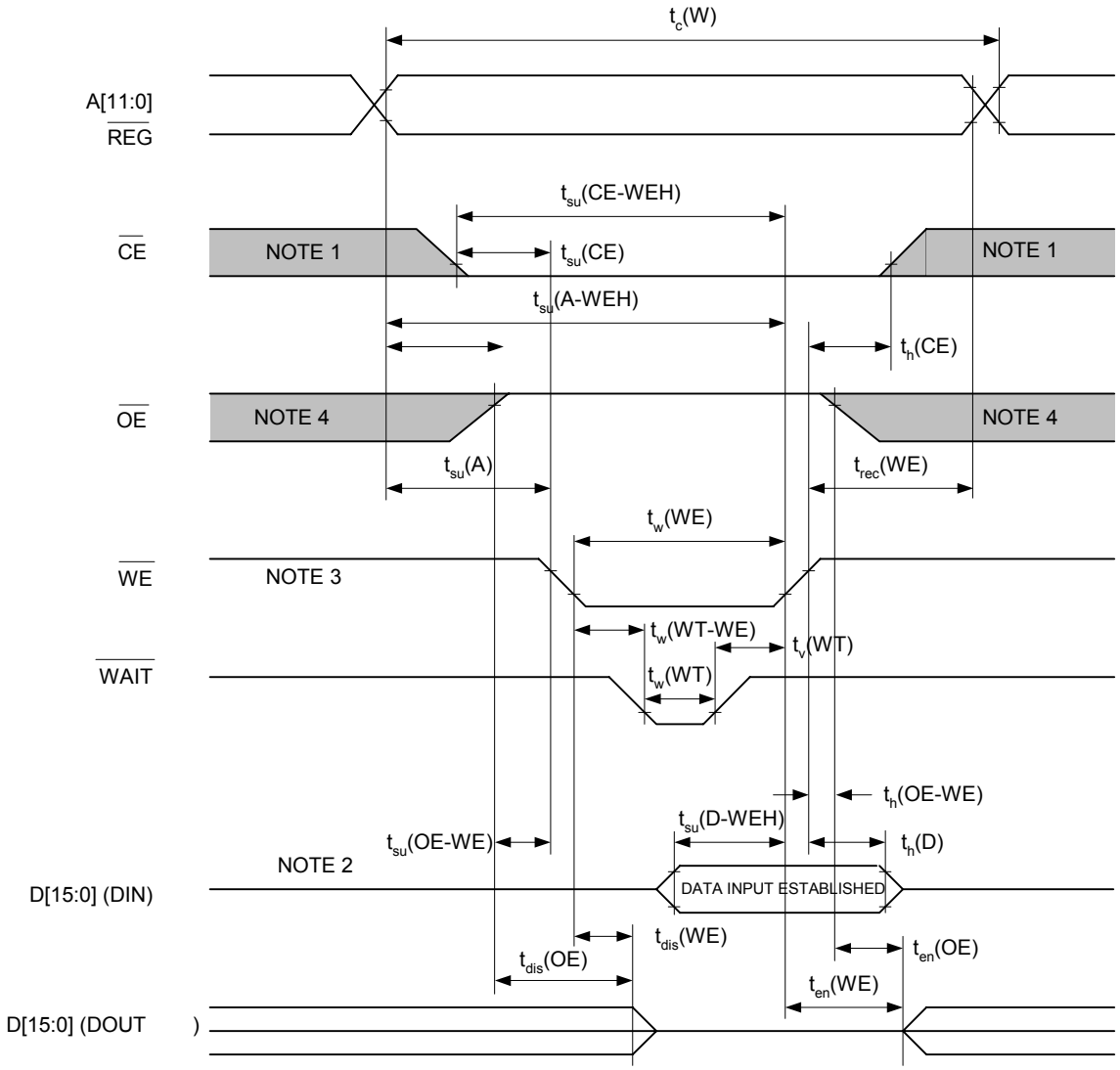
1. Shaded area can be high or low.
2. Applies to card only when $\overline{\text{WAIT}}$ is negated by card.
   However, the host must always provide at least this access time before sampling data.
3. Applies only when $\overline{\text{WAIT}}$ is asserted by card.

Figure 12: PCMCIA/Compact Flash Read Timing Diagram

Table 17: PCMCIA/Compact Flash Read Timing Characteristics

Parameter	*Min*	*Max*	*Units*
t_c(R)	250	–	ns
t_a(A)[2]	–	200	ns
t_h(A)	20	–	ns
t_a(CE)[2]	–	200	ns
t_{su}(CE)	0	–	ns
t_v(A)	0	–	ns
t_{su}(A)	20	–	ns
t_a(OE)[2]	–	125	ns
t_h(CE)	20	–	ns
t_v(WT–OE)[3]	–	35	ns
t_w(WT)[3]	0.01	3.0	µs
t_{dis}(CE)	–	30	ns
t_{en}(OE)	10	–	ns
t_v(WT)	20	–	ns
t_{dis}(OE)	–	60	ns

See Figure 12 for footnotes.



1. Shaded area can be high or low.
2. When the data I/O pin is in the output state, no signals can be applied to the data pins (D[15:0]) by the host system.
3. Minimum write pulse width must be met whether or not $\overline{\text{WAIT}}$ is asserted by card.
4. Can be high or low for write timing, but restrictions on $\overline{\text{OE}}$ apply.

Figure 13: PCMCIA/Compact Flash Write Timing Diagram

Table 18: PCMCIA/Compact Flash Write Timing Characteristics

Parameter	*Min*	*Max*	*Units*
t_c(W)	250	–	ns
t_{su}(CE-WEH)	180	–	ns
t_{su}(CE)	0	–	ns
t_{su}(A-WEH)	180	–	ns
t_h(CE)	20	–	ns
t_{su}(A)	20	–	ns
t_w(WE)	150	–	ns
t_{rec}(WE)	30	–	ns
t_v(WT-WE)	–	35	ns
t_w(WT)	0.01	3.0	µs
t_v(WT)	20	–	ns
t_{su}(OE-WE)	10	–	ns
t_{su}(D-WEH)	80	–	ns
t_h(OE-WE)	10	–	ns
t_h(D)	30	–	ns
t_{dis}(OE)	–	100	ns
t_{dis}(WE)	–	100	ns
t_{en}(WE)	5	–	ns
t_{en}(OE)	5	–	ns

SPROM TIMING

Table 19: SPROM Timing Characteristics

Signal Name	*Period*	*Output Max*	*Output Min*	*Setup*	*Hold*
SPROM_CLK	1.92 µsec	–	–	–	–
SPROM_CLK falling edge to SPROM_DOUT	–	0.5 µs	0.3 µs	–	–
SPROM_CLK falling edge to SPROM_CS	–	0.5 µs	0.3 µs	–	–
SPROM_CLK rising edge to SPROM_DIN	–	–	–	0.5 µs	–0.3 µs

JTAG TIMING

Table 20: JTAG Timing Characteristics

Signal Name	Period	Output Max	Output Min	Setup	Hold
JTAG_TCK	125 ns	–	–	–	–
JTAG_TDI	–	–	–	20 ns	0 ns
JTAG_TMS	–	–	–	20 ns	0 ns
JTAG_TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

Section 7: Package Specifications

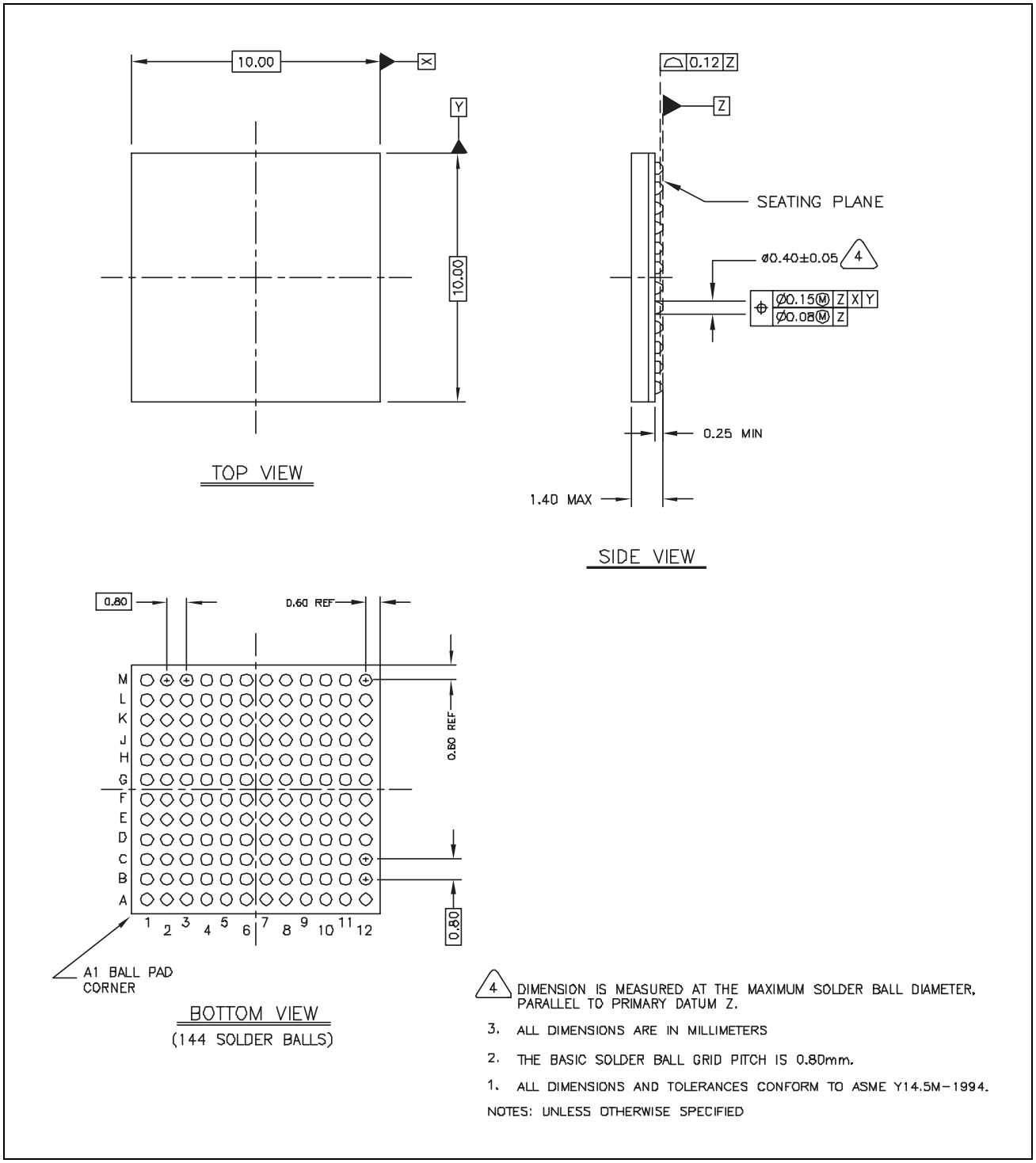


Figure 14: BCM4318/BCM4318E 144-Pin FBGA

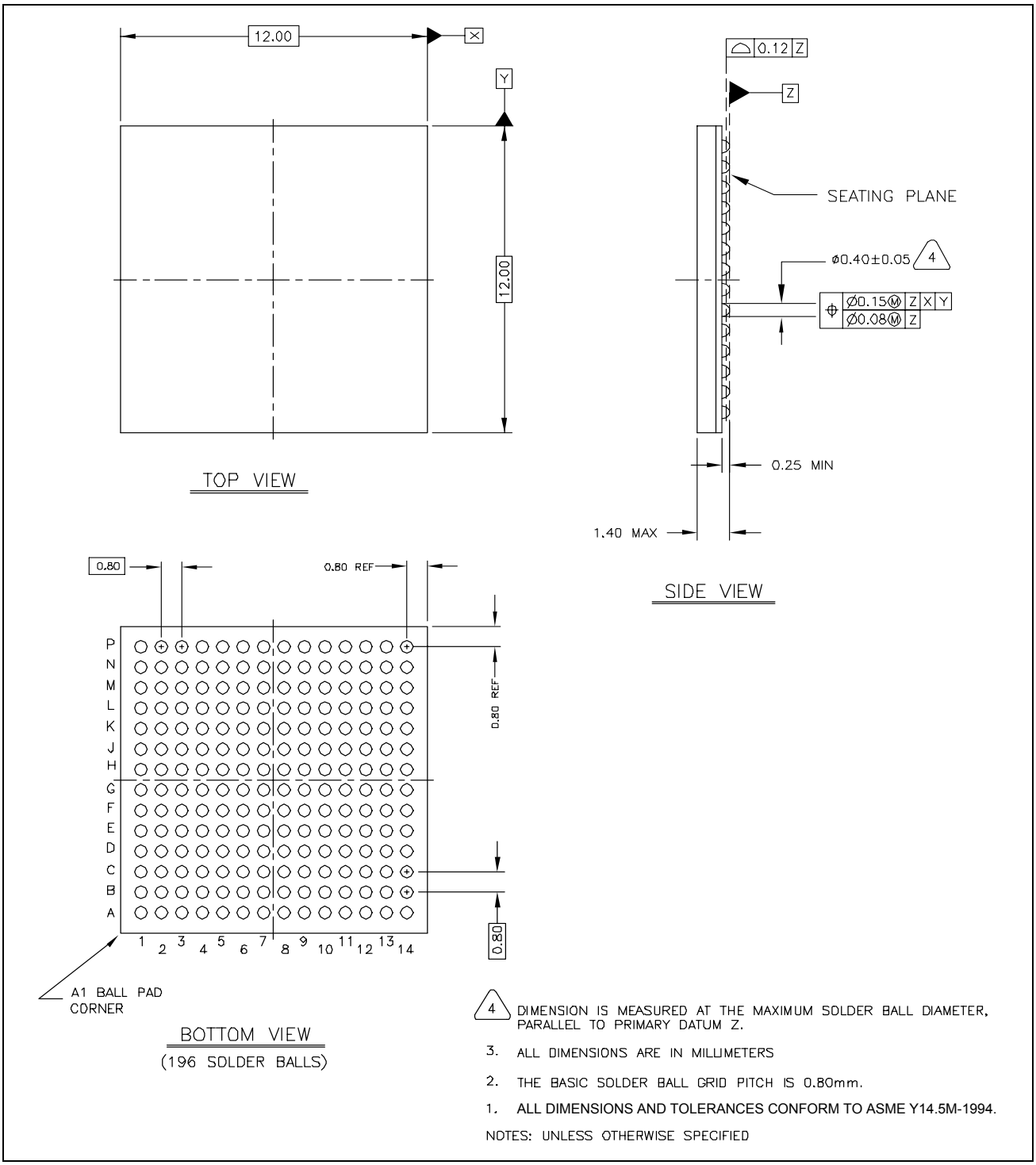


Figure 15: BCM4318/BCM4318E 196-Pin FBGA

Section 8: Ordering Information

Table 21: BCM4318/BCM4318E Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM4318KFBG	196-pin FBGA (Lead Free)	0°C to 75°C
BCM4318EKFBG	196-pin FBGA (Lead Free)	0°C to 75°C
BCM4318SKFBG	144-pin FBGA (Lead Free)	0°C to 75°C

Broadcom Corporation

16215 Alton Parkway
P.O. Box 57013
Irvine, California 92619-7013
Phone: 949-450-8700
Fax: 949-450-8710