



74LVX132

Low Voltage Quad 2-Input NAND Schmitt Trigger

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

General Description

The LVX132 contains four 2-input NAND Schmitt Trigger Gates. The pin configuration and function are the same as the LVX00 but the inputs have hysteresis between the positive-going and negative-going input thresholds, which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals, thus providing greater noise margins than conventional gates.

The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Ordering Information

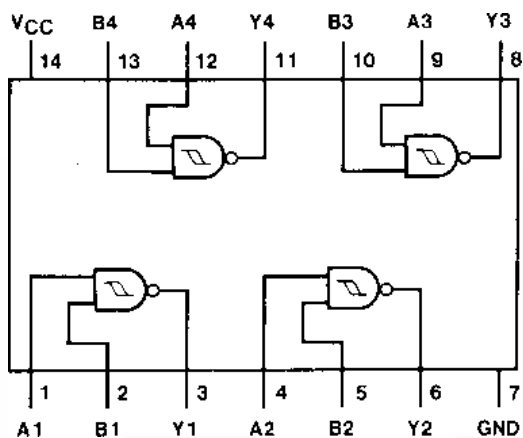
Order Number	Package Number	Package Description
74LVX132M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX132SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX132MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

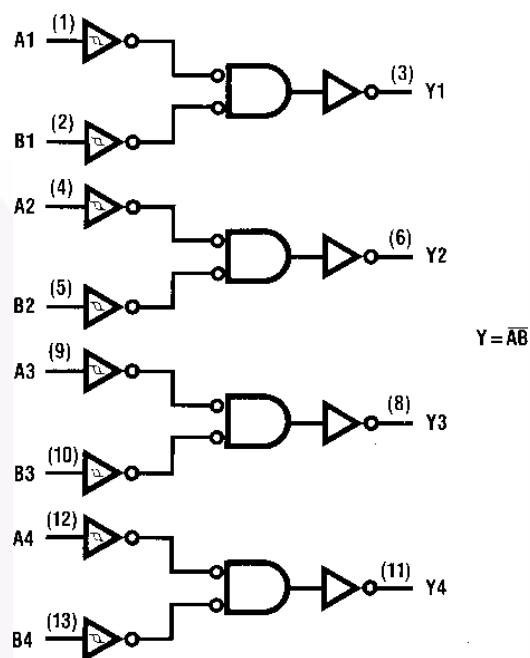
Connection Diagram



Pin Description

Pin Names	Descriptions
A_n, B_n	Inputs
Y_n	Outputs

Logic Diagram



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +7.0V
I_{IK}	DC Input Diode Current, $V_I = -0.5V$	-20mA
V_I	DC Input Voltage	-0.5V to 7V
I_{OK}	DC Output Diode Current $V_O = -0.5V$	-20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	$\pm 25mA$
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	$\pm 50mA$
T_{STG}	Storage Temperature	-65°C to +150°C
P	Power Dissipation	180mW

Recommended Operating Conditions⁽¹⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to 3.6V
V_I	Input Voltage	0V to 5.5V
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	-40°C to +85°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0ns/V to 100ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C			T _A = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V _{I+}	Positive Threshold	3.0				2.2		2.2	V
V _{I-}	Negative Threshold	3.0		0.9			0.9		V
V _H	Hysteresis	3.0		0.3		1.2	0.3	1.2	V
V _{OH}	HIGH Level Output Voltage	2.0	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -50μA	1.9	2.0		1.9		V
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -50μA	2.9	3.0		2.9		
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -4mA	2.58			2.48		
V _{OL}	LOW Level Output Voltage	2.0	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 50 μA		0.0	0.1		0.1	V
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 50 μA		0.0	0.1		0.1	
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 4 mA			0.36		0.44	
I _{IN}	Input Leakage Current	3.6	V _{IN} = 5.5V or GND			±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	3.6	V _{IN} = V _{CC} or GND			2.0		20	μA

Noise Characteristics⁽²⁾

Symbol	Parameter	V _{CC} (V)	C _L (pF)	T _A = 25°C		Units
				Typ.	Limit	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	50	0.3	0.5	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	50	-0.3	-0.5	V
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	3.3	50		2.0	V
V _{ILD}	Maximum LOW Level Dynamic Input Voltage	3.3	50		0.8	V

Note:

2. Input t_r = t_f = 3ns

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	C _L (pF)	T _A = +25°C			T _A = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t _{PLH} , t _{PHL}	Propagation Delay Time	2.7	15		7.0	11.5	1.0	13.0	ns
			50		10.5	16.0	1.0	18.7	
		3.3 ± 0.3	15		6.1	10.6	1.0	12.5	
			50		9.0	15.4	1.0	17.5	
t _{OSLH} , t _{OSHL}	Output to Output Skew ⁽³⁾	2.7	50			1.5		1.5	ns
		3.3				1.5		1.5	

Note:

3. Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	T _A = +25°C			T _A = -40°C to +85°C		Units
		Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance		4	10		10	pF
C _{PD}	Power Dissipation Capacitance ⁽⁴⁾		18				pF

Note:

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{6 \text{ (per Gate)}}$

Physical Dimensions

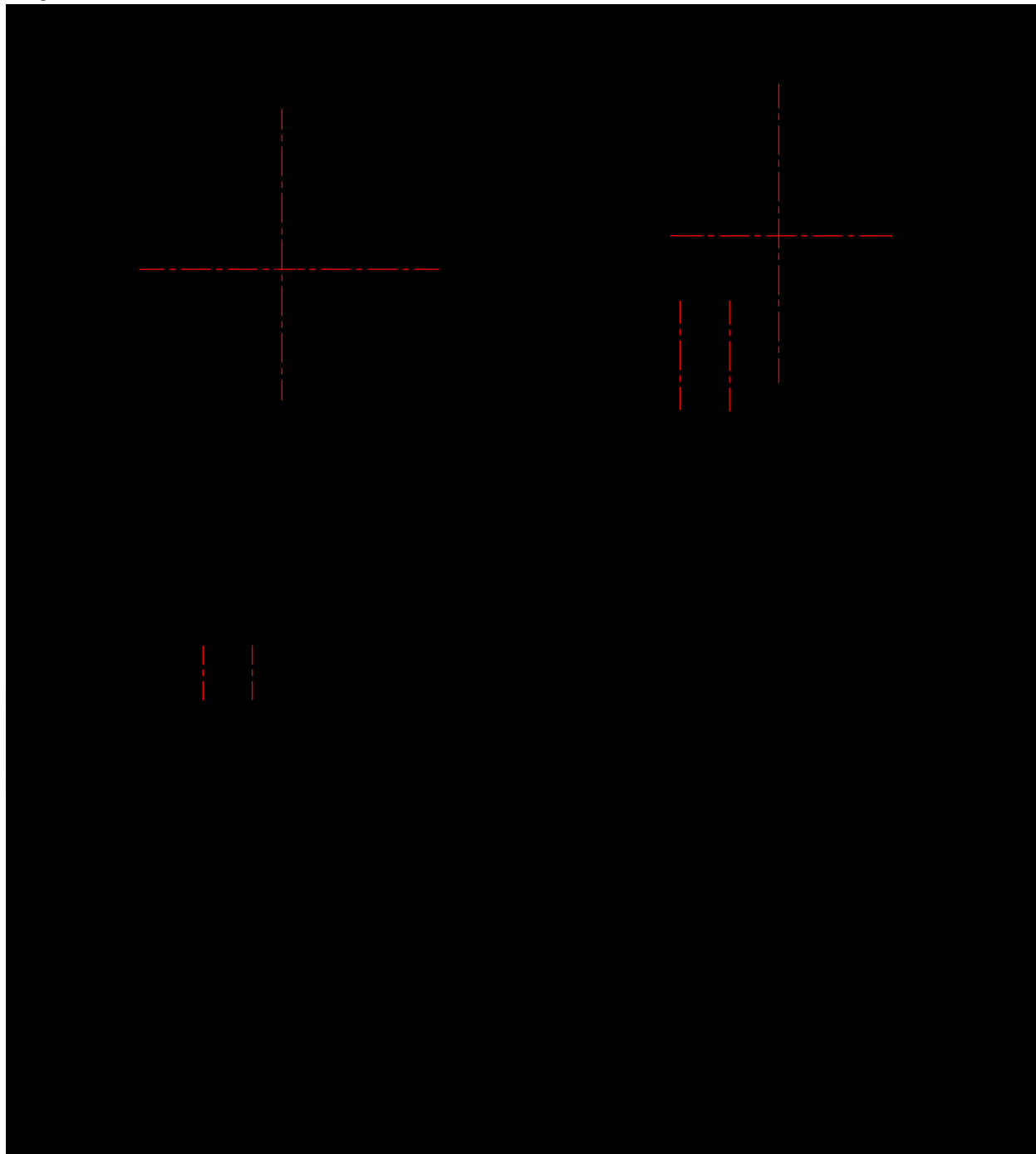


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)**Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

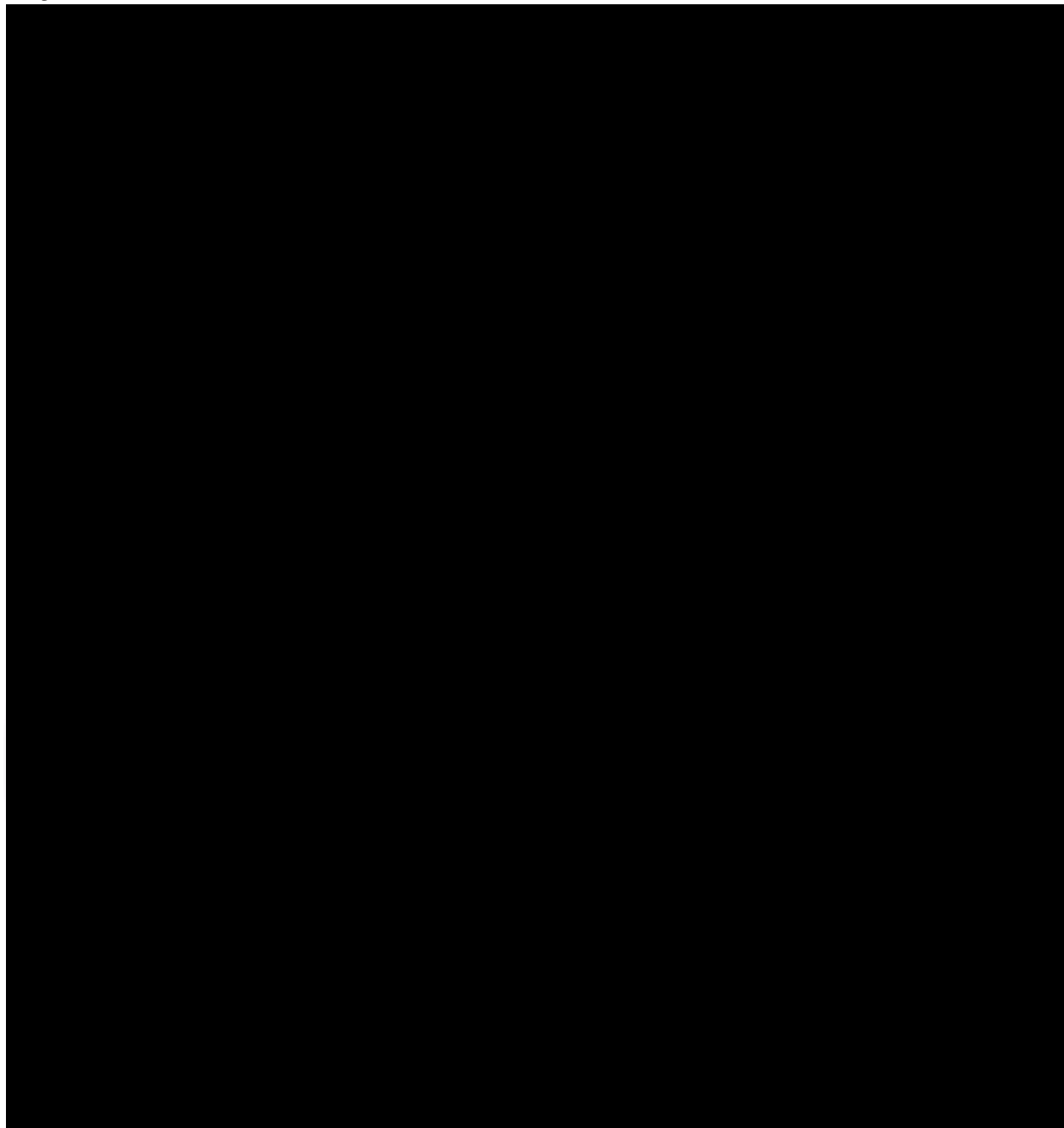
Physical Dimensions (Continued)

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



subsidaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx [®]	FPS [™]	PDP-SPM [™]	SupreMOS [™]
Build it Now [™]	FRFET [®]	Power220 [®]	SyncFET [™]
CorePLUS [™]	Global Power Resource SM	POWEREDGE [®]	SYSTEM [®]
CROSSVOLT [™]	Green FPS [™]	Power-SPM [™]	GENERAL
CTL [™]	Green FPS [™] e-Series [™]	PowerTrench [®]	The Power Franchise [®]
Current Transfer Logic [™]	GTO [™]	Programmable Active Droop [™]	the
EcoSPARK [®]	i-Lo [™]	QFET [®]	power [®]
EZSWITCH [™] *	IntelliMAX [™]	QS [™]	franchise
E ² [™]	ISOPLANAR [™]	QT Optoelectronics [™]	TinyBoost [™]
F [®]	MegaBuck [™]	Quiet Series [™]	TinyBuck [™]
Fairchild [®]	MICROCOUPLER [™]	RapidConfigure [™]	TinyLogic [®]
Fairchild Semiconductor [®]	MicroFET [™]	SMART START [™]	TINYOPTO [™]
FACT Quiet Series [™]	MicroPak [™]	SPM [®]	TinyPower [™]
FACT [®]	MillerDrive [™]	STEALTH [™]	TinyPWM [™]
FAST [®]	Motion-SPM [™]	SuperFET [™]	TinyWire [™]
FastvCore [™]	OPTOLOGIC [®]	SuperSOT [™] 3	SerDes [™]
FlashWriter [®] *	OPTOPLANAR [®]	SuperSOT [™] 6	UHC [®]
		SuperSOT [™] 8	Ultra FRFET [™]
			UniFET [™]
			VCX [™]

* EZSWITCH[™] and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.