SN54ABTH162245, SN74ABTH162245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS712A - FEBRUARY 1998 - REVISED APRIL 1999

SN54ABTH162245 . . . WD PACKAGE **Members of the Texas Instruments** SN74ABTH162245 . . . DGG, DGV, OR DL PACKAGE Widebus[™] Family (TOP VIEW) A-Port Outputs Have Equivalent 25- Ω Series Resistors, So No External Resistors 48 10E 1DIR 1 Are Required 1B1 2 47 1A1 State-of-the-Art *EPIC-*II*B*[™] BiCMOS Design 1B2 3 46 1A2 Significantly Reduces Power Dissipation GND 4 45 GND Typical VOLP (Output Ground Bounce) 1B3 🛛 5 44 A 1A3 < 1 V at V_{CC} = 5 V, T_A = 25°C 1B4 🛛 6 43 🛛 1A4 42 V_{CC} V_{CC} [] 7 Distributed V_{CC} and GND Pin Configuration **Minimizes High-Speed Switching Noise** 1B5 8 41 1A5 1B6 🛛 9 40 **1**A6 Flow-Through Architecture Optimizes PCB 39 GND GND 10 Layout 1B7 🛛 38 **1**A7 11 **Bus Hold on Data Inputs Eliminates the** 1B8 12 37 1A8 Need for External Pullup/Pulldown 2B1 13 36 2A1 Resistors 2B2 14 35 2A2 Latch-Up Performance Exceeds 500 mA Per GND 15 34 GND **JESD 17** 2B3 🛛 16 33 2A3 ESD Protection Exceeds 2000 V Per 2B4 17 32 2A4 MIL-STD-833, Method 3015; Exceeds 200 V 31 🛛 V_{CC} 18 VccL Using Machine Model (C = 200 pF, R = 0) 2B5 🛛 19 30 2A5 Package Options Include Plastic Thin 2B6 20 29 2A6 Shrink Small-Outline (DGG), Thin Very GND 21 28 GND Small-Outline (DGV), and Shrink 2B7 222 27 2A7 Small-Outline (DL) Packages and 380-mil 2B8 23 26 2A8 Fine-Pitch Ceramic Flat (WD) Package 2DIR 24 25 20E Using 25-mil Center-to-Center Spacings

description

The 'ABTH162245 devices are 16-bit noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 25- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABTH162245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABTH162245 is characterized for operation from -40°C to 85°C.



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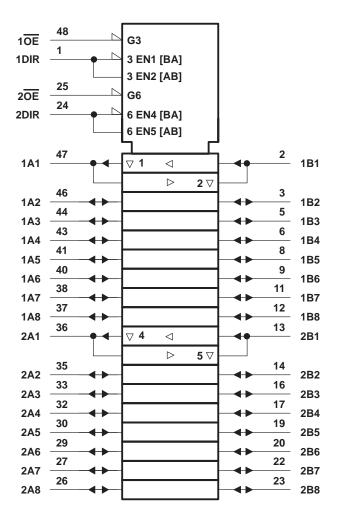
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FUNCTION TABLE

	(each 8-bit section)									
INP	UTS									
OE	DIR	OPERATION								
L	L	B data to A bus								
L	Н	A data to B bus								
н	Х	Isolation								

logic symbol[†]

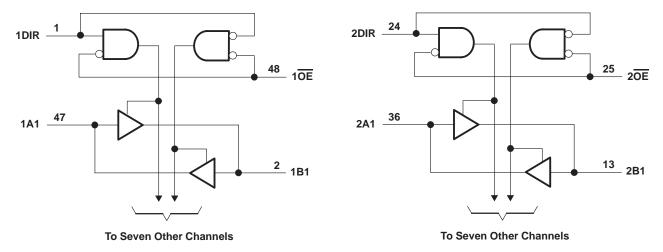


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	. -0.5 V to 7 V
Input voltage range, V _I (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high or power-off state, V _O	–0.5 V to 5.5 V
Current into any output in the low state, I _O : SN54ABTH162245 (B port)	96 mA
SN74ABTH162245 (B port)	128 mA
SN54/74ABTH162245 (A port)	30 mA
Input clamp current, I _{IK} (V _I < 0)	–18 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	89°C/W
DGV package	93°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	–65°C to 150°C
reases beyond these listed under "absolute maximum retings" may source permanent demore to the device. These are stre	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

			SN54ABTH	1162245	SN74ABTH	162245	UNIT
			MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2	2	2		V
VIL	Low-level input voltage			.8		0.8	V
VI	Input voltage		0	Vcc	0	VCC	V
lau	High lovel output current	B port	4	-24		-32	mA
ЮН	High-level output current	A port	20	-12		-12	IIIA
1.0.	Low-level output current	B port	20	48		64	mA
IOL		A port	44	12		12	MA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEAT AANDITIA		SN54	ABTH16	2245	SN74	ABTH16	2245		
PAR	AMETER	TEST CONDITIO						TYP [†]	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	lj = -18 mA			-1.2			-1.2	V	
		V _{CC} = 5 V,	I _{OH} = -1 mA	2.5			2.5				
			I _{OH} = -1 mA	3			3				
A port	$V_{CC} = 4.5 V$	I _{OH} = -3 mA	3			3.1					
		I _{OH} = -12 mA				2.6			N		
VOH		V _{CC} = 5 V,	I _{OH} = -3 mA	3			3			V	
	Deart		I _{OH} = -3 mA	2.5			2.5				
B port	$V_{CC} = 4.5 V$	I _{OH} = -24 mA	2								
			I _{OH} = -32 mA				2				
	A port		I _{OL} = 12 mA			0.8			0.8		
V _{OL} B port	$V_{CC} = 4.5 V$	I _{OL} = 48 mA			0.45			0.45	V		
	в роп		I _{OL} = 64 mA			A			0.55		
V _{hys}					100	ЕŅ		100		mV	
I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND			PREL	±1			±1	μA	
A or B ports				6	±20			±20			
		V _{CC} = 4.5 V	VI = 0.8 V	100	2		100			A	
l(hold)		VCC = 4.5 V	V _I = 2 V	-100)		-100			μA	
loff		$V_{CC} = 0,$ $V_{I} \text{ or } V_{O} = 0 \text{ to } 4.5 \text{ V}$		Q.					±100	μA	
la†	A port			-25		-90	-25		-100		
IO‡	B port	V _{CC} = 5.5 V,	V _O = 2.5 V	-50		-180	-50		-180	mA	
ICEX		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50			50	μΑ	
		V _{CC} = 5.5 V,	Outputs high			2			2		
ICC	A or B ports	$I_{O} = 0,$	Outputs low			32			32	mA	
		$V_{I} = V_{CC}$ or GND	Outputs disabled			2			2		
∆ICC§	Data inputs	$V_{CC} = 5.5 V$, One input at 3.4 V, Other inputs at V_{CC} or GND				2			2	mA	
Control		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5			1.5		
Ci		VI = 2.5 V or 0.5 V			3			3		pF	
Cio		V _O = 2.5 V or 0.5 V			6			6		pF	

[†] All typical values are at $V_{CC} = 5$ V.

[‡]Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABTH162245		SN74ABTH162245		UNIT
		(001101)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
^t PLH	А	В	1	2.2	3.4	1	4.1	1	3.9	ns
^t PHL	~	В	1	2.3	3.7	1	4.4	1	4.2	115
^t PLH	В	А	1	2.7	4.1	1	4.9	1	4.6	ns
^t PHL	D	A	1.5	3.1	4.6	1.5	5.2	1.5	5.1	115
^t PZH	OE	В	1	3.6	5.2	1	6.4	1	6.3	ns
^t PZL	ÛE		1	3.7	5.4	14	6.5	1	6.4	115
^t PHZ	ŌE	В	2	4.4	5.8	2	6.4	2	6.3	ns
^t PLZ	UE	В	1.5	3.3	4.7	9.5	5.6	1.5	5.2	115
^t PZH		٨	1.5	4.1	6	4 1.5	7.2	1.5	7.1	
^t PZL	ŌĒ	A	1.5	4.3	6.1	1.5	7.3	1.5	7	ns
^t PHZ	ŌĒ	А	2	4.5	6.1	2	6.8	2	6.6	
^t PLZ	UE	A	1.5	3.7	5.1	1.5	6.1	1.5	5.7	ns

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7 V **S1** O Open **500** Ω From Output $\Lambda \Lambda A$ TEST **S**1 **Under Test** GND C Open tPLH/tPHL $C_1 = 50 \text{ pF}$ tPLZ/tPZL 7 V **500** Ω (see Note A) tPHZ/tPZH Open LOAD CIRCUIT 3 V **Timing Input** 1.5 V 0 V tw th t_{su} 3 V 3 V 1.5 V Input 1.5 V Data Input 1.5 V 1.5 V 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PULSE DURATION SETUP AND HOLD TIMES 3 V 3 V Output 1.5 V 1.5 V 1.5 V 1.5 V Input Control 0 V 0 V **t**PLH ^tPHL ^tPZL ⁻ - tplz Output VOH 3.5 V Waveform 1 1.5 V 1.5 V Output 1.5 V V_{OL} + 0.3 V S1 at 7 V VOL VOL (see Note B) **t**PLH ^tPHZ tPHL · tp7H Output VOH ۷он V_{OH} – 0.3 V Waveform 2 1.5 V 1.5 V 1.5 V Output S1 at Open 0 V VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES ENABLE AND DISABLE TIMES** INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING

PARAMETER MEASUREMENT INFORMATION

NOTES: A. $\ensuremath{\mathsf{C}}\xspace_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns. t_f ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABTH162245DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH162245	Samples
SN74ABTH162245DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH162245	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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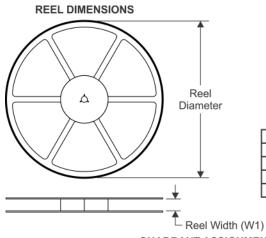
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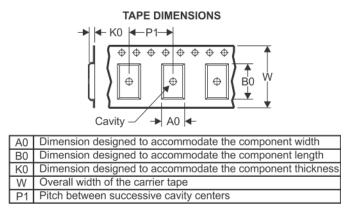
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All o	dimensions	are	nominal
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Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH162245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1



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PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH162245DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0



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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
SN74ABTH162245DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

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