

## N-Channel Power MOSFET

700V, 3A, 1.4Ω

### FEATURES

- Super-Junction technology
- High performance, small  $R_{DS(on)} * Q_g$  figure of merit (FOM)
- High ruggedness performance
- 100% UIS and  $R_g$  tested
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

### KEY PERFORMANCE PARAMETERS

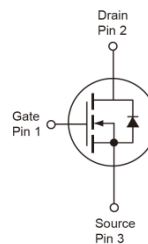
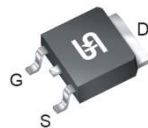
PARAMETER	VALUE	UNIT
$V_{DS}$	700	V
$R_{DS(on)}$ (max)	1.4	Ω
$Q_g$	7.4	nC

### APPLICATION

- Power Supply
- AC/DC LED Lighting



TO-252 (DPAK)



**Note:** MSL 3 (Moisture Sensitivity Level) per J-STD-020

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	700	V
Gate-Source Voltage	$V_{GS}$	±30	V
Continuous Drain Current <sup>(Note 1)</sup>	$I_D$	$T_C = 25^\circ\text{C}$	3
		$T_C = 100^\circ\text{C}$	1.8
Pulsed Drain Current <sup>(Note 2)</sup>	$I_{DM}$	9	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_{DTOT}$	28	W
Single Pulsed Avalanche Energy <sup>(Note 3)</sup>	$E_{AS}$	26	mJ
Single Pulsed Avalanche Current <sup>(Note 3)</sup>	$I_{AS}$	0.6	A
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	°C

### THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	4.4	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	°C/W

**Thermal Performance Note:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	$BV_{DSS}$	700	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	2	--	4	V
Gate Body Leakage	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = 700\text{V}, V_{GS} = 0\text{V}$	$I_{DSS}$	--	--	1	$\mu\text{A}$
Drain-Source On-State Resistance (Note 4)	$V_{GS} = 10\text{V}, I_D = 1.2\text{A}$	$R_{DS(ON)}$	--	1.1	1.4	$\Omega$
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$V_{DS} = 380\text{V}, I_D = 3\text{A},$ $V_{GS} = 10\text{V}$	$Q_g$	--	7.4	--	nC
Gate-Source Charge		$Q_{gs}$	--	1.8	--	
Gate-Drain Charge		$Q_{gd}$	--	2.4	--	
Input Capacitance	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$	$C_{iss}$	--	317	--	pF
Output Capacitance		$C_{oss}$	--	42	--	
Gate Resistance	$f = 1.0\text{MHz}$	$R_g$	--	3.2	--	$\Omega$
<b>Switching</b> (Note 6)						
Turn-On Delay Time	$V_{DD} = 380\text{V},$ $R_{GEN} = 25\Omega,$ $I_D = 3\text{A}, V_{GS} = 10\text{V},$	$t_{d(on)}$	--	16	--	ns
Turn-On Rise Time		$t_r$	--	15	--	
Turn-Off Delay Time		$t_{d(off)}$	--	26	--	
Turn-Off Fall Time		$t_f$	--	8	--	
<b>Source-Drain Diode</b>						
Forward On Voltage (Note 4)	$I_S = 3\text{A}, V_{GS} = 0\text{V}$	$V_{SD}$	--	--	1.4	V
Reverse Recovery Time	$V_R = 200\text{V}, I_S = 2\text{A}$ $di_f/dt = 100\text{A}/\mu\text{s}$	$t_{rr}$	--	137	--	ns
Reverse Recovery Charge		$Q_{rr}$	--	0.7	--	$\mu\text{C}$

**Notes:**

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3.  $L = 144\text{mH}, I_{AS} = 0.6\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega,$  Starting  $T_J = 25^\circ\text{C}$
4. Pulse test:  $PW \leq 300\mu\text{s},$  duty cycle  $\leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

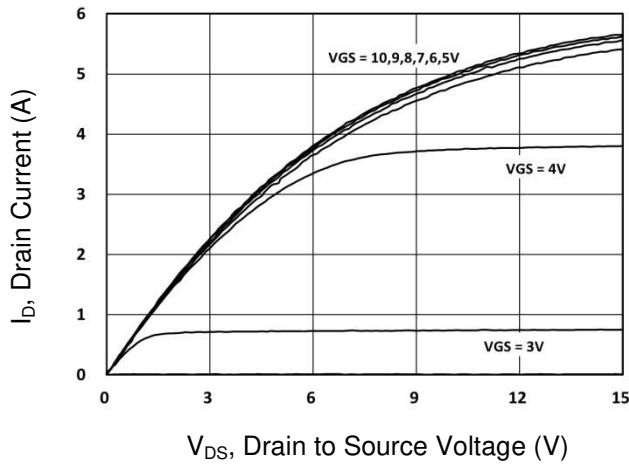
**ORDERING INFORMATION**

PART NO.	PACKAGE	PACKING
TSM70NB1R4CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

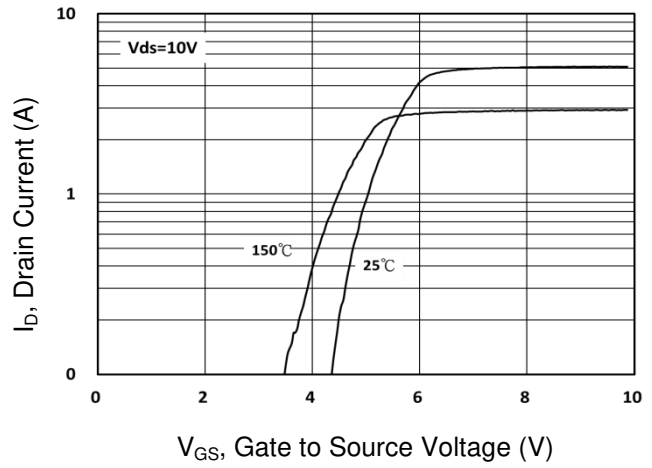
**CHARACTERISTICS CURVES**

( $T_c = 25^\circ\text{C}$  unless otherwise noted)

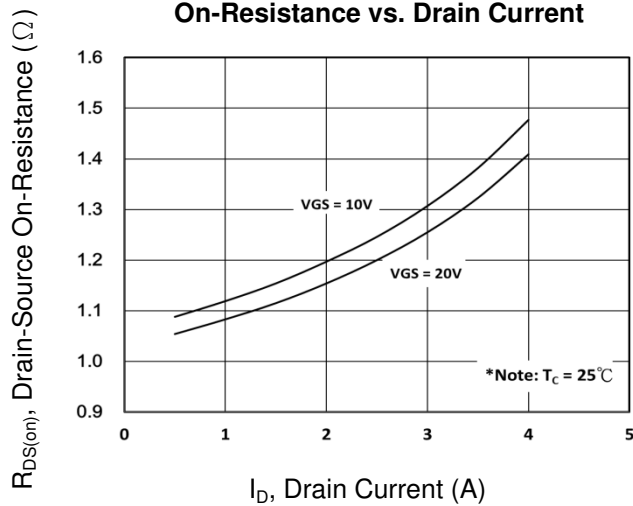
**Output Characteristics**



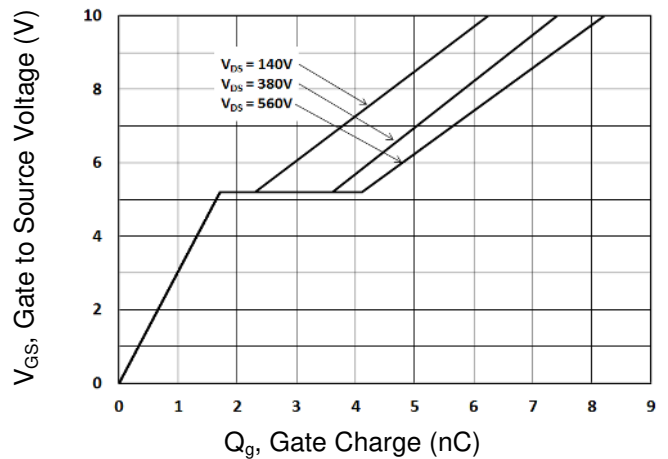
**Transfer Characteristics**



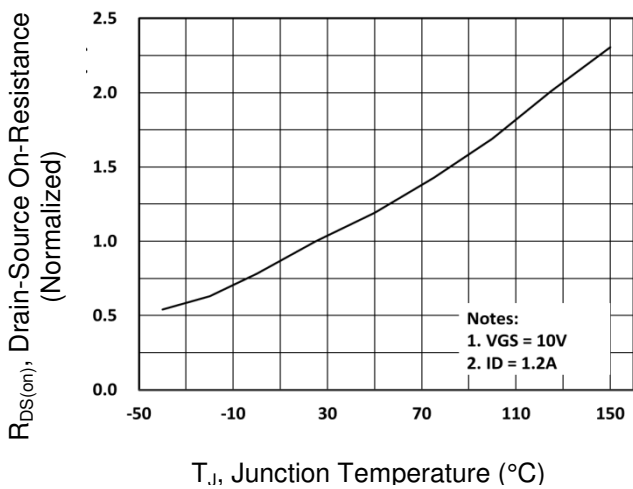
**On-Resistance vs. Drain Current**



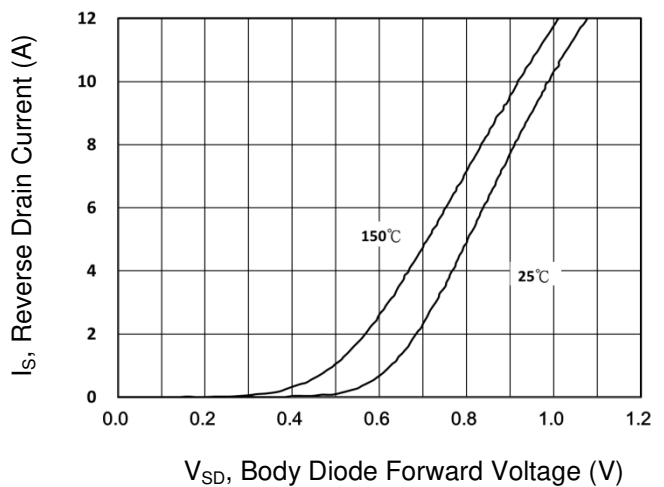
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**



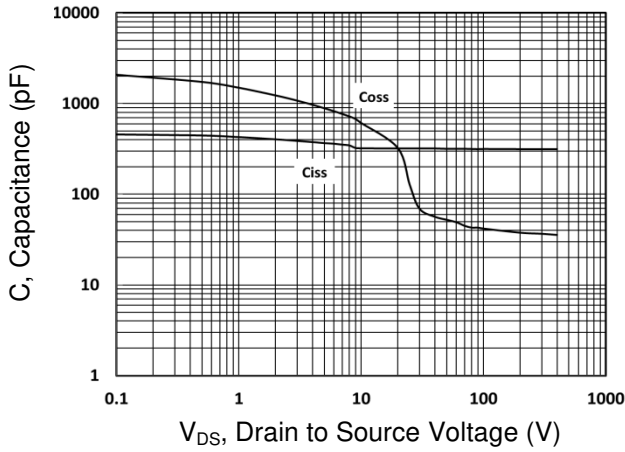
**Source-Drain Diode Forward Current vs. Voltage**



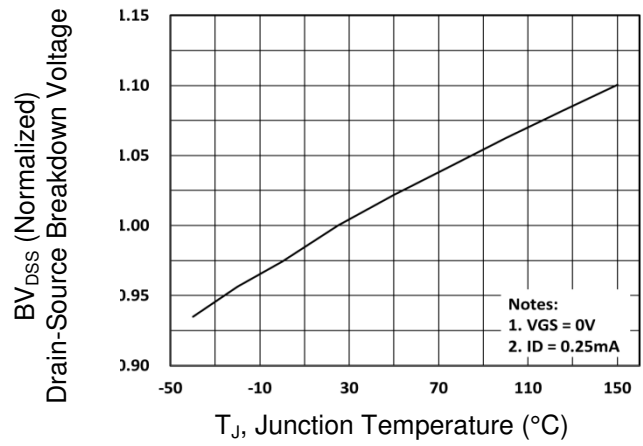
**CHARACTERISTICS CURVES**

( $T_C = 25^\circ\text{C}$  unless otherwise noted)

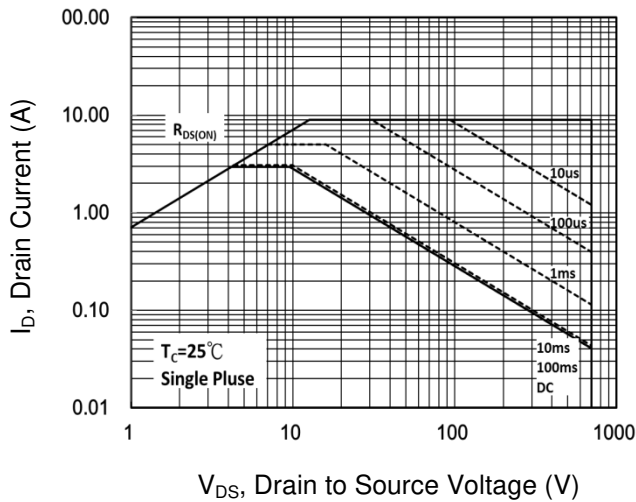
**Capacitance vs. Drain-Source Voltage**



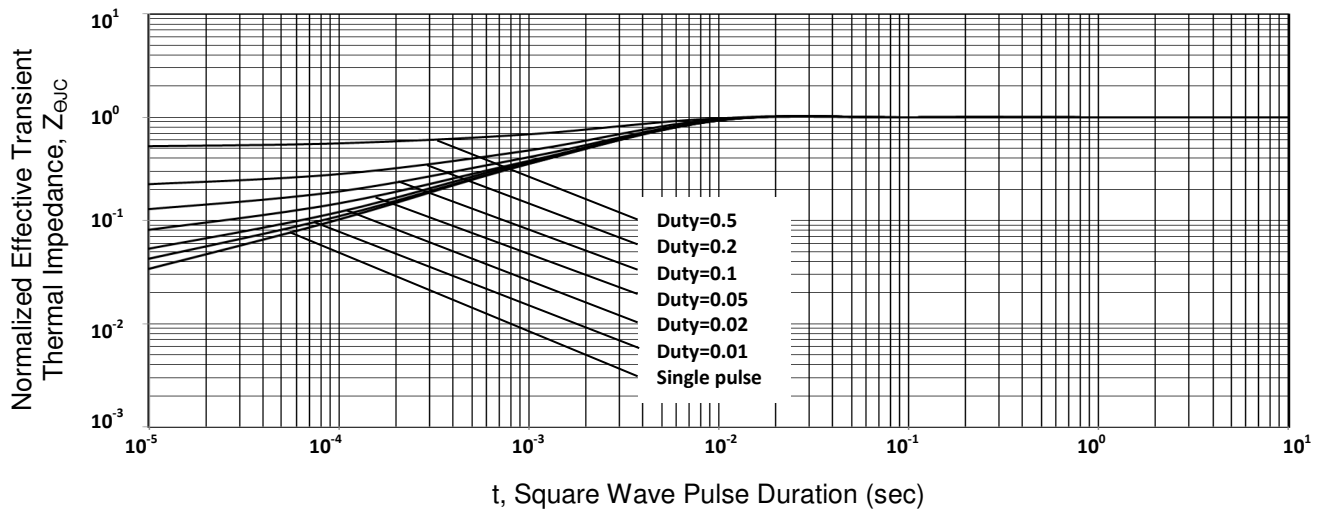
**$BV_{DSS}$  vs. Junction Temperature**



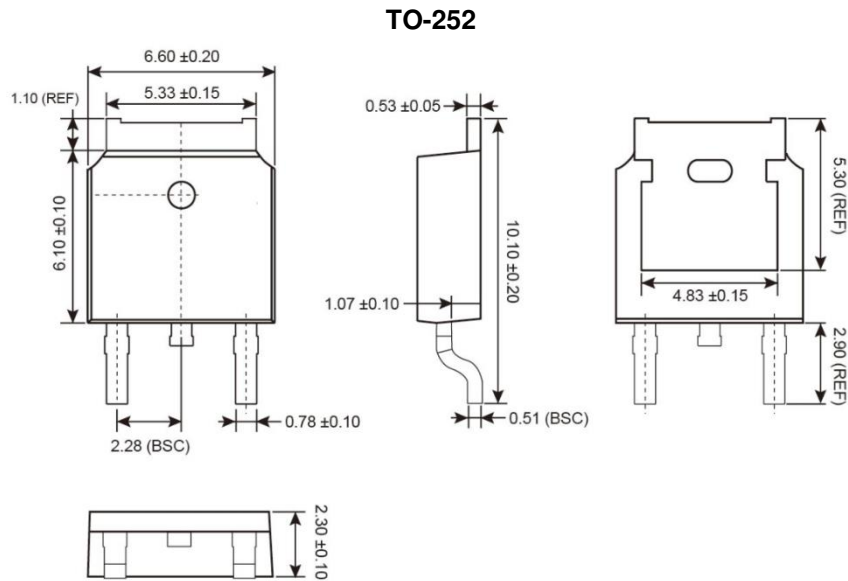
**Maximum Safe Operating Area**



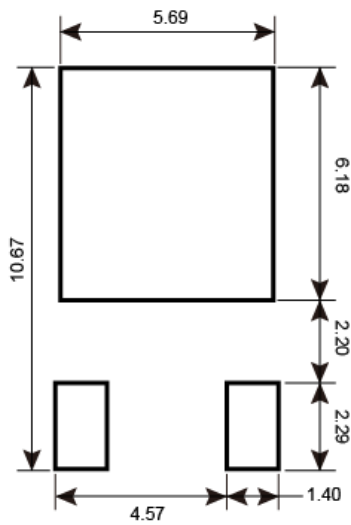
**Normalized Thermal Transient Impedance, Junction-to-Case**



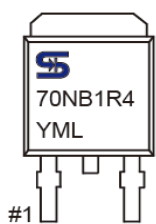
**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)



**SUGGESTED PAD LAYOUT**



**MARKING DIAGRAM**



- Y** = Year Code
- M** = Month Code
- O** =Jan    **P** =Feb    **Q** =Mar    **R** =Apr
- S** =May    **T** =Jun    **U** =Jul    **V** =Aug
- W** =Sep    **X** =Oct    **Y** =Nov    **Z** =Dec
- L** = Lot Code (1~9, A~Z)

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