PCM1802 Single-Ended Analog-Input 24-Bit, 96-kHz Stereo A/D Converter

1 Features

- 24-Bit Delta-Sigma Stereo A/D Converter
- Single-Ended Voltage Input: 3 V_{P-P}
- Antialiasing Filter Included
- Oversampling Decimation Filter
  - Oversampling Frequency: ×64, ×128
  - Pass-Band Ripple: ±0.05 dB
  - Stop-Band Attenuation: –65 dB
  - On-Chip High-Pass Filter: 0.84 Hz (44.1 kHz)
- High Performance
  - THD+N: 96 dB (Typical)
  - SNR: 105 dB (Typical)
  - Dynamic Range: 105 dB (Typical)
- PCM Audio Interface
  - Master and Slave Mode Selectable
  - Data Formats: 24-Bit Left-Justified; 24-Bit I^2S; 20-bit or 24-Bit Right-Justified
- Sampling Rate: 16 kHz to 96 kHz
- System Clock: 256 f_S, 384 f_S, 512 f_S, 768 f_S
- Dual Power Supplies: 5 V (Analog), 3.3 V (Digital)
- Package: 20-Pin SSOP

2 Applications

- AV Amplifier Receivers
- MD Players
- CD Recorders
- Multitrack Receivers
- Electric Musical Instruments

3 Description

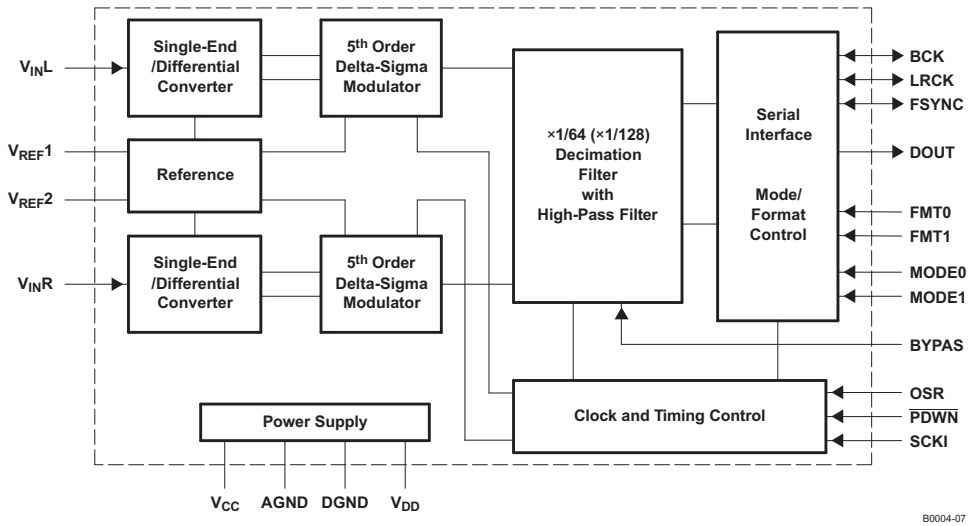
The PCM1802 is a high-performance, low-cost, single-chip stereo analog-to-digital converter with single-ended analog voltage input. The PCM1802 uses a delta-sigma modulator with 64-times or 128-times oversampling, and includes a digital decimation filter and high-pass filter (HPF), which removes the DC component of the input signal. For various applications, the PCM1802 supports master and slave modes and four data formats in serial interface. The PCM1802 is suitable for a wide variety of cost-sensitive consumer applications where good performance, 5-V analog supply, and 3.3-V digital supply operation is required. The PCM1802 is fabricated using a highly advanced CMOS process and is available in the DB 20-pin SSOP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM1802	SSOP (20)	7.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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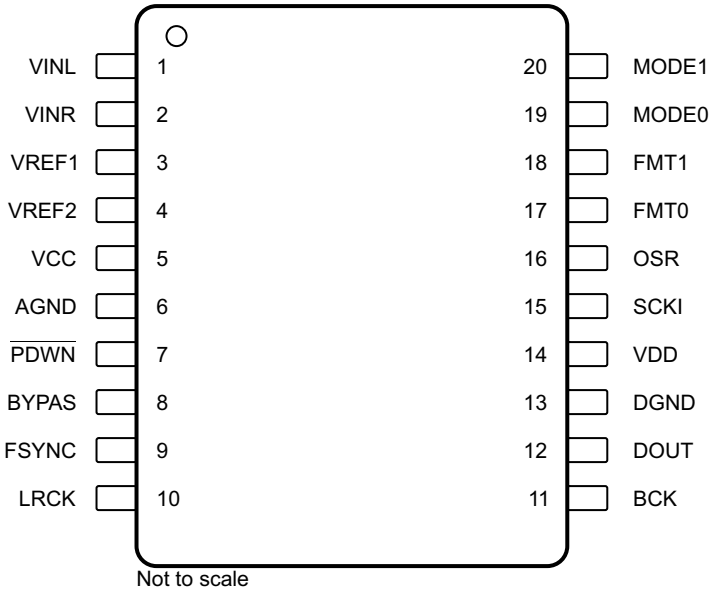
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2005) to Revision D	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Deleted Lead temperature (soldering), 260°C for 5 s, from *Absolute Maximum Ratings* table	4
• Added *Thermal Information* table	5
• Changed Thermal resistance, $R_{\theta JA}$, value in *Thermal Information* table From: 115°C/W To: 80.8°C/W	5

5 Pin Configuration and Functions

DB Package
20-Pin SSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	6	—	Analog GND
BCK	11	I/O	Bit clock input and output (1)
BYPAS	8	I	HPF bypass control. Low: normal mode (DC cut); High: bypass mode (through) (2)
DGND	13	—	Digital GND
DOUT	12	O	Audio data output
FMT0	17	I	Audio data format select 0 (see *Data Format*) (2)
FMT1	18	I	Audio data format select 1 (see *Data Format*) (2)
FSYNC	9	I/O	Frame synchronous clock input and output (1)
LRCK	10	I/O	Sampling clock input and output (1)
MODE0	19	I	Mode select 0 (see *Interface Mode*) (2)
MODE1	20	I	Mode select 1 (see *Interface Mode*) (2)
OSR	16	I	Oversampling ratio select. Low: ×64 f_S; High: ×128 f_S (2)
$\overline{\text{PDWN}}$	7	I	Power-down control, active-low (2)
SCKI	15	I	System clock input; 256 f_S, 384 f_S, 512 f_S, or 768 f_S (3)
VCC	5	—	Analog power supply, 5 V
VDD	14	—	Digital power supply, 3.3 V
VINL	1	I	Analog input, L-channel
VINR	2	I	Analog input, R-channel
VREF1	3	—	Reference-1 decoupling capacitor
VREF2	4	—	Reference-2 voltage input, normally connected to V_{CC}

(1) Schmitt-Trigger input
(2) Schmitt-Trigger input with internal pulldown (50 kΩ typically), 5-V tolerant
(3) Schmitt-Trigger input, 5-V tolerant

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VCC		6.5	V
	VDD		4	
Ground voltage differences	AGND and DGND		±0.1	V
Supply voltage difference (V_{CC} – V_{DD})	VCC and VDD		3 V	V
Digital input voltage	FSYNC, LRCK, BCK, and DOUT	–0.3	V_{DD} + 0.3	V
	$\overline{PDWN}$, BYPAS, SCKI, OSR, FMT0, FMT1, MODE0, and MODE1	–0.3	6.5	
Analog input voltage	VINL, VINR, VREF1, and VREF2	–0.3	V_{CC} + 0.3	V
Input current (any pins except supplies)			±10	mA
Ambient temperature under bias		–40	125	°C
Junction temperature			150	°C
Package temperature (IR reflow, peak)			260	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Analog supply voltage, V_{CC}			5		V
Digital supply voltage, V_{DD}			3.3		V
Analog input voltage, full-scale (–0 dB)			3		V_{P-P}
Digital input logic family			TTL		
Digital input clock frequency	Sampling clock	8.192		49.152	MHz
	System clock	32		96	kHz
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		PCM1802 DB (SSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			24		Bits
DATA FORMAT						
	Audio data interface format			Left-justified, I²S, or right-justified		
	Audio data bit length			20 or 24		Bits
	Audio data format			MSB first or 2s complement		
f_S	Sampling frequency		16	44.1	96	kHz
	System clock frequency	256 f_S	4.096	11.2896	24.576	MHz
		384 f_S	6.144	16.9344	36.864	
		512 f_S	8.192	22.5792	49.152	
		768 f_S[1]	12.288	33.8688		
INPUT LOGIC						
V_{IH}	Input logic level[2]		2		V_{DD}	VDC
V_{IL}			0		0.8	
V_{IH}	Input logic level[3]		2		5.5	
V_{IL}			0		0.8	
I_{IH}	Input logic current[4]	V_{IN} = V_{DD}			±10	µA
I_{IL}		V_{IN} = 0 V			±10	
I_{IH}	Input logic current[5]	V_{IN} = V_{DD}		65	100	
I_{IL}		V_{IN} = 0 V			±10	
OUTPUT LOGIC						
V_{OH}	Output logic level[6]	I_{OUT} = –1 mA	2.8			VDC
V_{OL}		I_{OUT} = 1 mA			0.5	
DC ACCURACY						
	Gain mismatch, channel-to-channel			±1%	±4%	FSR
	Gain error			±2%	±6%	FSR
	Bipolar zero error	HPF bypassed[7]		±2%		FSR

(1) Maximum system clock frequency is not applicable at 768 f_S, f_S = 96 kHz (see *System Clock*).
(2) Applies to FSYNC, LRCK, BCK (Schmitt-trigger input in slave mode) pins.
(3) Applies to PDWN, BYPAS, SCKI, OSR, FMT0, FMT1, MODE0, MODE1 (Schmitt-trigger input, 5-V tolerant) pins.
(4) Applies to FSYNC, LRCK, BCK (Schmitt-trigger input in slave mode), SCKI (Schmitt-trigger input) pins.
(5) Applies to PDWN, BYPAS, OSR, FMT0, FMT1, MODE0, MODE1 (Schmitt-trigger input, with 50-kΩ typical pulldown resistor) pins.
(6) Applies to FSYNC, LRCK, BCK (in master mode), DOUT pins.
(7) High-pass filter

Electrical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE(8)							
THD+N	Total harmonic distortion + noise		f_S = 44.1 kHz, V_{IN} = –0.5 dB		0.0015%	0.003%	
			f_S = 96 kHz, V_{IN} = –0.5 dB, system clock = 256 f_S, oversampling ratio = ×64(9)		0.0025%		
			f_S = 44.1 kHz, V_{IN} = –60 dB		0.7%		
			f_S = 96 kHz, V_{IN} = –60 dB, system clock = 256 f_S, oversampling ratio = ×64(9)		1.2%		
	Dynamic range		f_S = 44.1 kHz, A-weighted	100	105		dB
			f_S = 96 kHz, A-weighted, system clock = 256 f_S, oversampling ratio = ×64(9)		103		
	Signal to noise ratio		f_S = 44.1 kHz, A-weighted	100	105		dB
			f_S = 96 kHz, A-weighted, system clock = 256 f_S, oversampling ratio = ×64(9)		103		
	Channel separation		f_S = 44.1 kHz	96	103		dB
			f_S = 96 kHz, system clock = 256 f_S, oversampling ratio = ×64(9)		98		
ANALOG INPUT							
	Input voltage				0.6 × V_{CC}		V_{P-P}
$V_{REF}1$	Center voltage				0.5 × V_{CC}		V
	Input impedance				20		kΩ
	Antialiasing filter frequency response		–3 dB		300		kHz
DIGITAL FILTER PERFORMANCE							
	Pass band					0.454 f_S	Hz
	Stop band			0.583 f_S			Hz
	Pass-band ripple					±0.05	dB
	Stop-band attenuation			–65			dB
	Delay time				17.4 / f_S		s
	HPF frequency response		–3 dB		0.019 f_S		mHz
POWER SUPPLY REQUIREMENTS							
V_{CC}	Voltage			4.5	5	5.5	VDC
V_{DD}				2.7	3.3	3.6	
I_{CC}	Supply current(10)		V_{CC} = 5 V, V_{DD} = 3.3 V		24	30	mA
I_{DD}			f_S = 44.1 kHz V_{CC} = 5 V, V_{DD} = 3.3 V		8.3	10	
			f_S = 96 kHz, V_{CC} = 5 V, V_{DD} = 3.3 V(8)		17		
P_D	Power dissipation	Operation	f_S = 44.1 kHz, V_{CC} = 5 V, V_{DD} = 3.3 V		147	183	mW
			f_S = 96 kHz, V_{CC} = 5 V, V_{DD} = 3.3 V(8)		176		
		Power down	V_{CC} = 5 V, V_{DD} = 3.3 V		0.5		

(8) Analog performance specifications are tested with System Two™ audio measurement system by Audio Precision™, using 400-Hz HPF, 20-kHz LPF for 44.1-kHz operation or 40-kHz LPF for 96-kHz operation in RMS mode.
(9) f_S = 96 kHz, system clock = 256 f_S, oversampling ratio = ×64.
(10) Minimum load on DOUT, BCK, LRCK, and FSYNC.

6.6 Typical Characteristics

T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, Master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, and 24-bit data (unless otherwise noted).

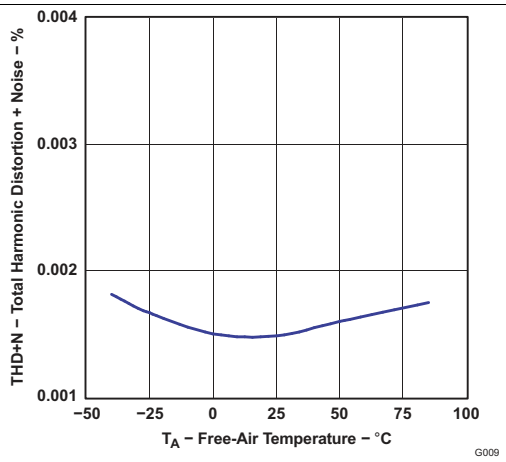


Figure 1. Total Harmonic Distortion + Noise vs Free-Air Temperature

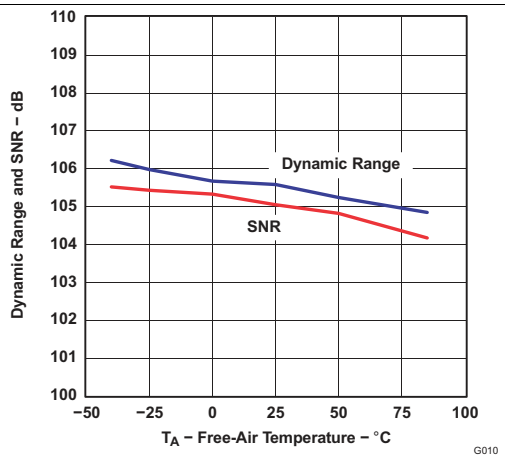


Figure 2. Dynamic Range and SNR vs Free-Air Temperature

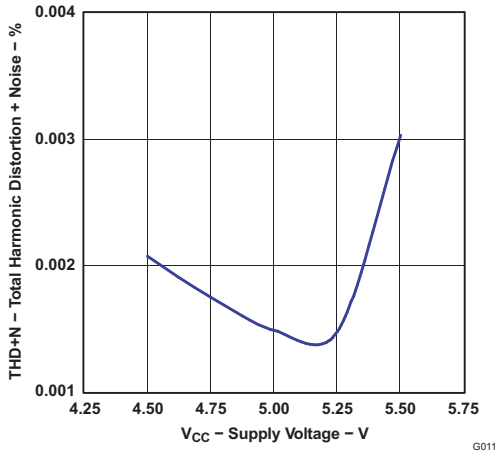


Figure 3. Total Harmonic Distortion + Noise vs Supply Voltage

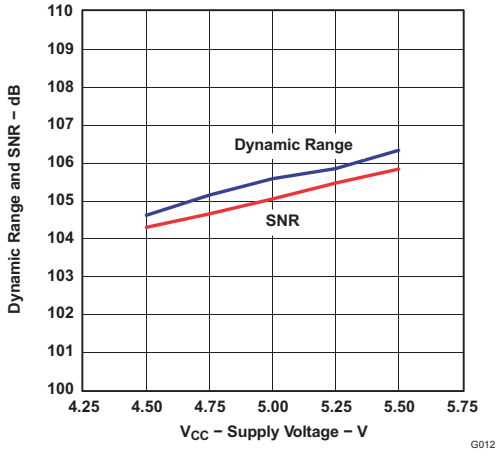


Figure 4. Dynamic Range and SNR vs Suppy Voltage

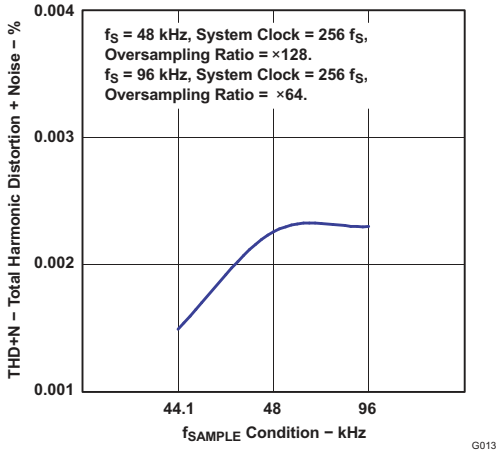


Figure 5. Total Harmonic Distortion + Noise vs f_{SAMPLE} Condition

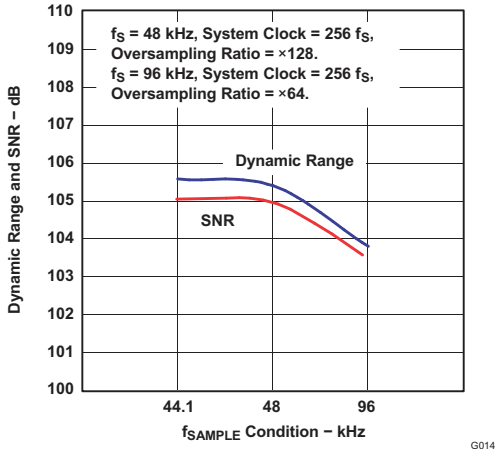


Figure 6. Dynamic Range and SNR vs f_{SAMPLE} Condition

6.6.1 Typical Characteristics: Internal Filter

6.6.1.1 Digital Filter: Decimation Filter Frequency Response

T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, Master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, and 24-bit data (unless otherwise noted).

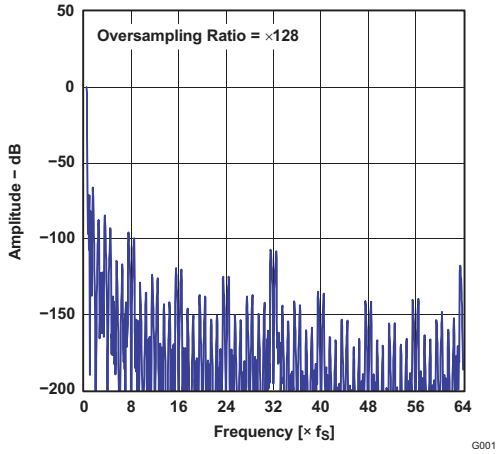


Figure 7. Amplitude vs Frequency Overall Characteristics

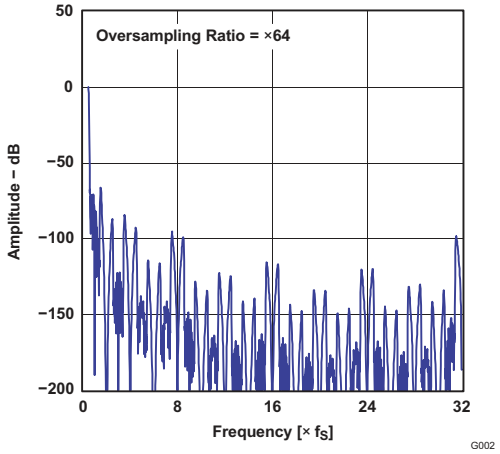


Figure 8. Amplitude vs Frequency Overall Characteristics

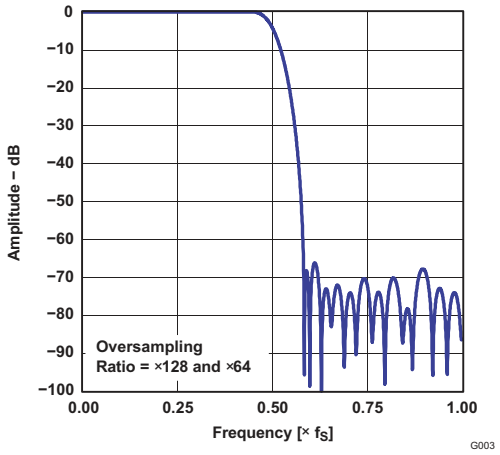


Figure 9. Amplitude vs Frequency Stop-Band Attenuation Characteristics

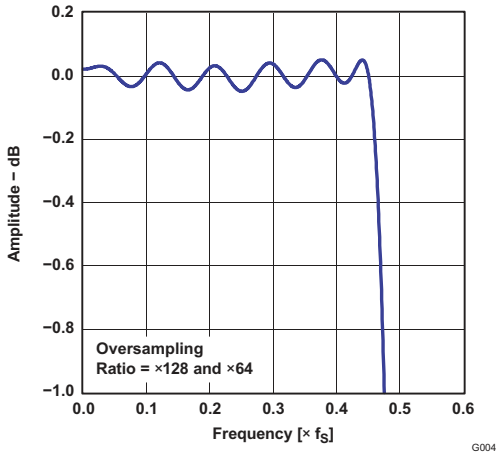


Figure 10. Amplitude vs Frequency Pass-Band Ripple Characteristics

Typical Characteristics: Internal Filter (continued)

6.6.1.2 HPF (High-Pass Filter) Frequency Response

T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, Master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, and 24-bit data (unless otherwise noted).

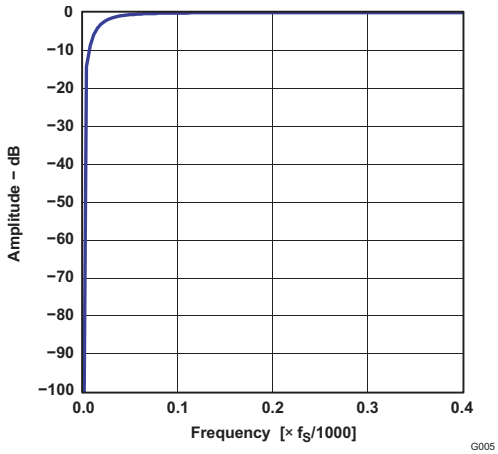


Figure 11. Amplitude vs Frequency HPF Stop-Band Characteristics

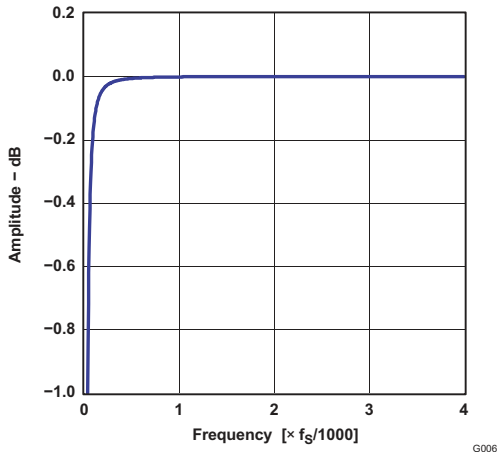


Figure 12. Amplitude vs Frequency HPF Pass-Band Characteristics

6.6.1.3 Analog Filter: Antialiasing Filter Frequence Response

T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, Master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, and 24-bit data (unless otherwise noted).

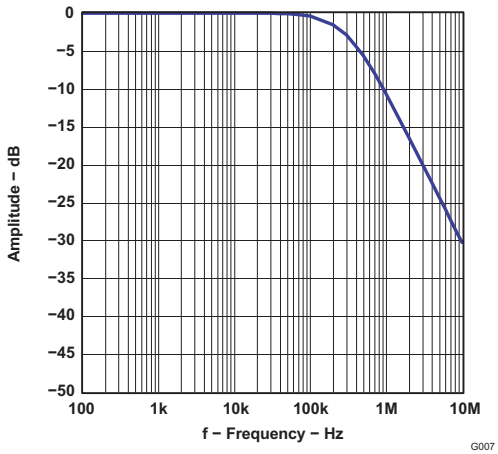


Figure 13. Amplitude vs Frequency Antialias Filter Stop-Band Characteristics

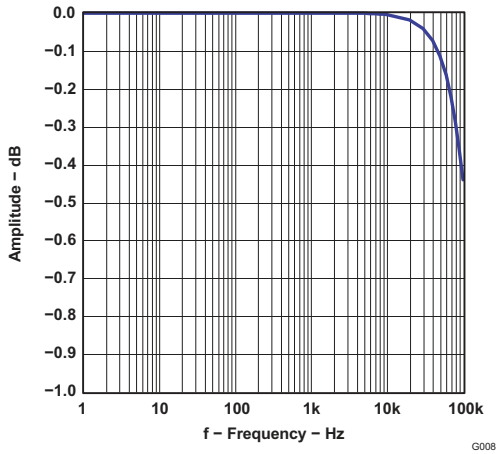


Figure 14. Amplitude vs Frequency Antialias Filter Pass-Band Characteristics

6.6.2 Typical Characteristics: Output Spectrum

T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, Master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, and 24-bit data (unless otherwise noted).

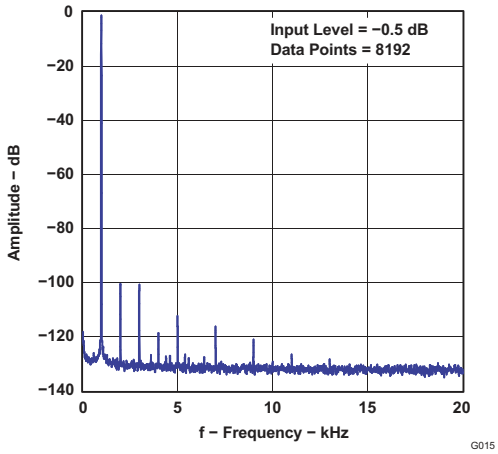


Figure 15. Amplitude vs Frequency

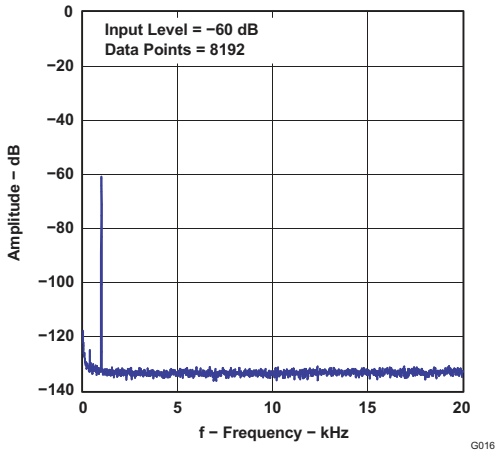


Figure 16. Amplitude vs Frequency

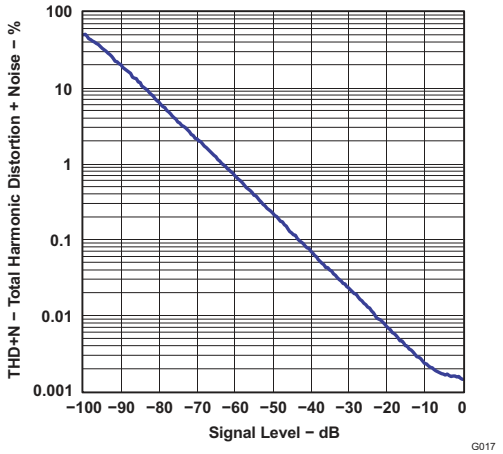


Figure 17. Total Harmonic Distortion + Noise vs Signal Level

6.6.3 Typical Characteristics: Supply Current

T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, Master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, and 24-bit data (unless otherwise noted).

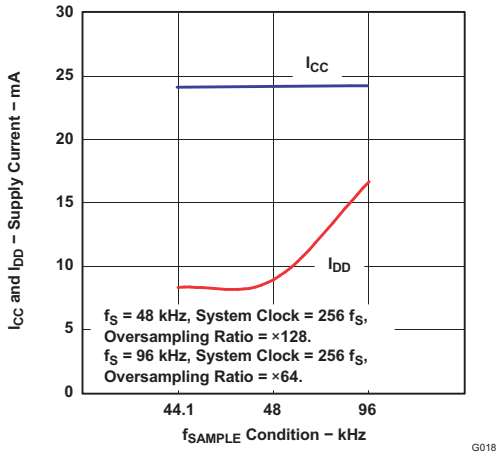


Figure 18. Supply Current vs f_{SAMPLE} Condition

7 Detailed Description

7.1 Overview

The PCM1802 device consists of a reference circuit, two channels of single-ended-to-differential converter, a fifth-order delta-sigma modulator with full differential architecture, a decimation filter with high-pass filter, and a serial interface circuit. Figure 19 illustrates the total architecture of the PCM1802, Figure 20 illustrates the architecture of single-ended-to-differential converter and antialiasing filter, and Figure 21 is the block diagram of the fifth-order delta-sigma modulator and transfer function. An on-chip high-precision reference with one external capacitor provides all reference voltages that are required by the PCM1802 device and defines the full-scale voltage range for both channels. On-chip single-ended-to-differential signal converters save the design, space, and extra parts cost for external signal converters. Full-differential architecture provides a wide dynamic range and excellent power-supply rejection performance. The input signal is sampled at a ×64 or ×128 oversampling rate, thus eliminating an external sample-hold amplifier. A fifth-order delta-sigma noise shaper, which consists of five integrators using the switched capacitor technique and a comparator, shapes the quantization noise generated by the comparator and 1-bit DAC outside of the audio signal band. The high-order delta-sigma modulation randomizes the modulator outputs and reduces the idle tone level. The 64-f_S or 128-f_S, 1-bit stream from the delta-sigma modulator is converted to a 1-f_S, 24-bit or 20-bit digital signal by removing high-frequency noise components with a decimation filter. The DC component of the signal is removed by the HPF, and the HPF output is converted to a time-multiplexed serial signal through the serial interface, which provides flexible serial formats.

7.2 Functional Block Diagrams

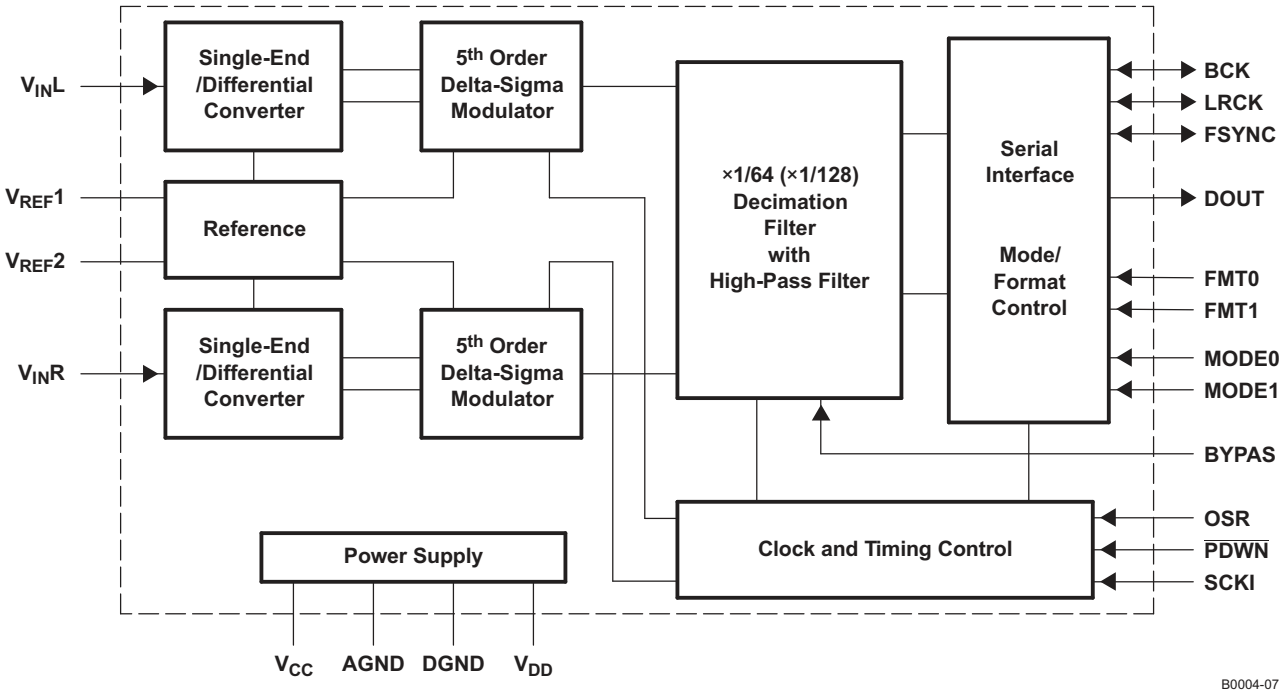


Figure 19. Block Diagram

Functional Block Diagrams (continued)

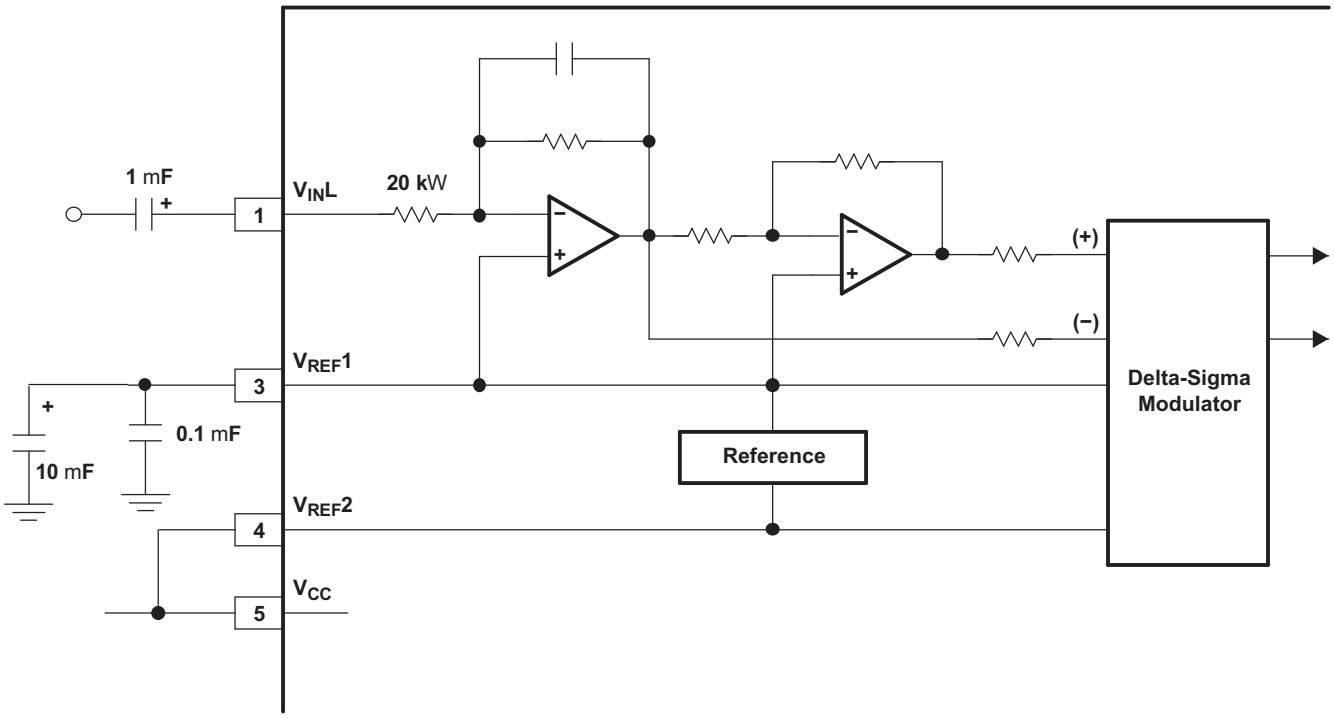


Figure 20. Analog Front End (Left Channel)

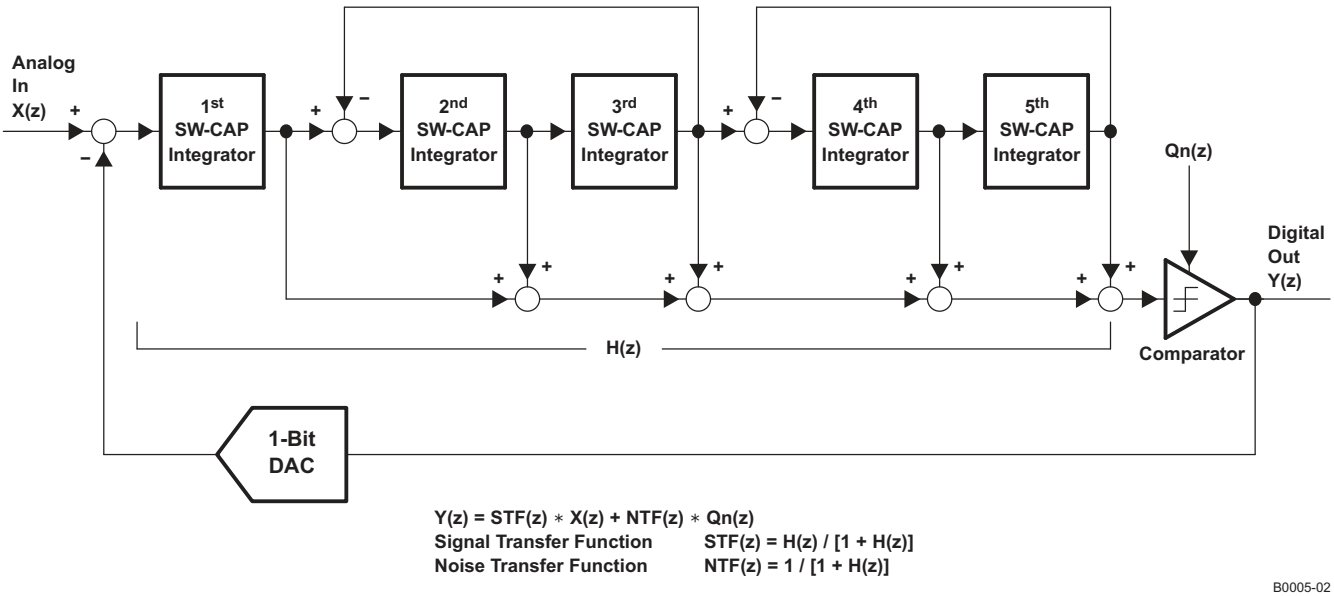


Figure 21. Block Diagram of Fifth-Order Delta-Sigma Modulator

7.3 Feature Description

7.3.1 Hardware Control

The FMT0, FMT1, OSR, BYPASS, MD0, and MD1 pins allow the device to be controlled by tying these pins to GPIO and GND or VDD from a host IC. These controls allow full configuration of the PCM1802.

7.3.2 Power-On Reset Sequence

The PCM1802 has an internal power-on reset circuit, and initialization (reset) is performed automatically when the power supply (V_{DD}) exceeds 2.2 V (typical). While V_{DD} < 2.2 V (typical), and for 1024 system-clock counts after V_{DD} > 2.2 V (typical), the PCM1802 stays in the reset state and the digital output is forced to zero. The digital output is valid after the reset state is released and the time of 4480 / f_S is passed. Figure 22 illustrates the internal power-on reset timing and the digital output for power-on reset.

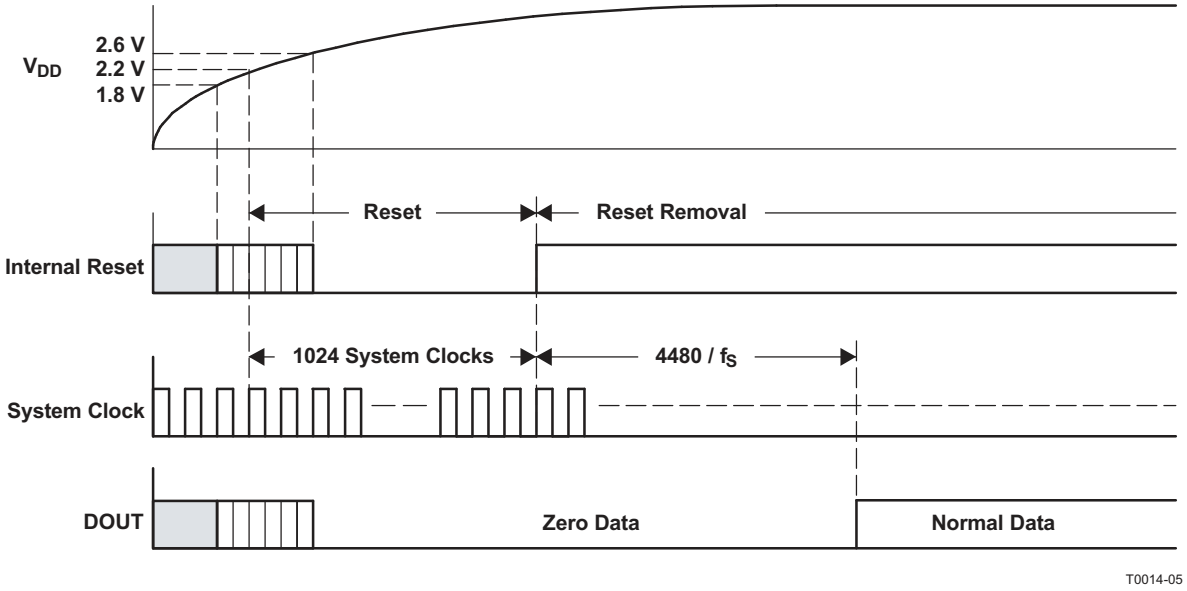


Figure 22. Internal Power-On Reset Timing

7.3.3 System Clock

The PCM1802 supports 256 f_S, 384 f_S, 512 f_S, and 768 f_S as the system clock, where f_S is the audio sampling frequency. The system clock must be supplied on SCKI.

The PCM1802 has a system clock detection circuit which automatically senses if the system clock is operating at 256 f_S, 384 f_S, 512 f_S, or 768 f_S in slave mode. In master mode, the system clock frequency must be selected by MODE0 and MODE1, and 768 f_S is not available. For system clock inputs of 384 f_S, 512 f_S, and 768 f_S, the system clock is divided to 256 f_S automatically, and the 256 f_S clock operates the delta-sigma modulator and the digital filter.

Feature Description (continued)

Table 1 lists the relationship of typical sampling frequencies and system clock frequencies, and Table 2 shows system clock timing.

Table 1. Sampling Frequency and System Clock Frequency

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)			
	256 f_S	384 f_S	512 f_S	768 f_S
32	8.192	12.288	16.384	24.576
44.1	11.2896	16.9344	22.5792	33.8688
48	12.288	18.432	24.576	36.864
64	16.384	24.576	32.768	49.152
88.2	22.5792	33.8688	45.1584	—
96	24.576	36.864	49.152	—

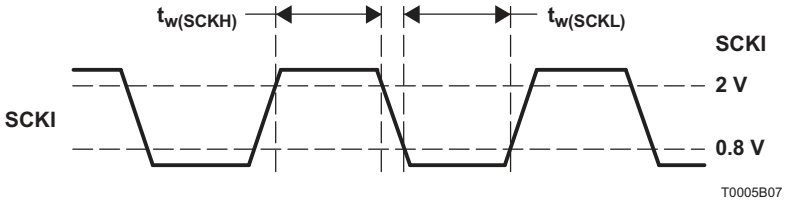


Table 2. System Clock Timing

PARAMETER		MIN	MAX	UNIT
$t_{w(SCKH)}$	System clock-pulse duration, high	7		ns
$t_{w(SCKL)}$	System clock-pulse duration, low	7		ns

7.4 Device Functional Modes

7.4.1 Power Down, HPF Bypass, Oversampling Control

$\overline{\text{PDWN}}$ controls the entire ADC operation. During power-down mode, both the supply current for the analog portion and the clock signal for the digital portion are shut down, and power dissipation is minimized. DOUT is also disabled and no system clock is accepted during power-down mode.

Table 3. Power-Down Control

$\overline{\text{PDWN}}$	MODE
LOW	Power-down mode
HIGH	Normal operation mode

The built-in function for DC component rejection can be bypassed using the BYPAS control. In bypass mode, the DC components of the analog input signal, such as the internal DC offset, are converted and included in the digital output data.

Table 4. HPF Bypass Control

BYPAS	HPF (HIGH-PASS FILTER) MODE
LOW	Normal (no DC component on DOUT) mode
HIGH	Bypass (DC component on DOUT) mode

OSR controls the oversampling ratio of the delta-sigma modulator, ×64 or ×128. The ×128 mode is available for f_S < 50 kHz, and must be used carefully as the duty cycle of the 384 f_S system clock affects performance.

Table 5. Oversampling Control

OSR	OVERSAMPLING RATIO
LOW	×64
HIGH	×128 (f_S < 50 kHz)

7.4.2 Serial Audio Data Interface

The PCM1802 interfaces with the audio system through BCK, LRCK, FSYNC, and DOUT.

7.4.2.1 Data Format

The PCM1802 supports four audio data formats in both master and slave modes, and they are selected by FMT1 and FMT0 as shown in Table 6. Figure 23 and Figure 25 illustrate the data formats in slave mode and master mode, respectively.

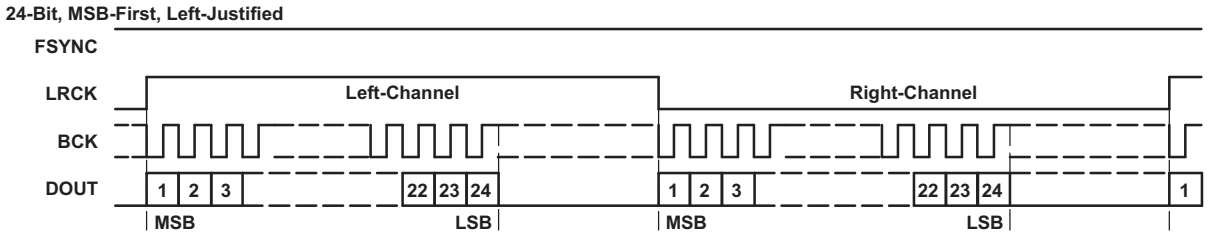
Table 6. Data Format

FORMAT	FMT1	FMT0	FORMAT
0	0	0	Left-justified, 24-bit
1	0	1	I^2S, 24-bit
2	1	0	Right-justified, 24-bit
3	1	1	Right-justified, 20-bit

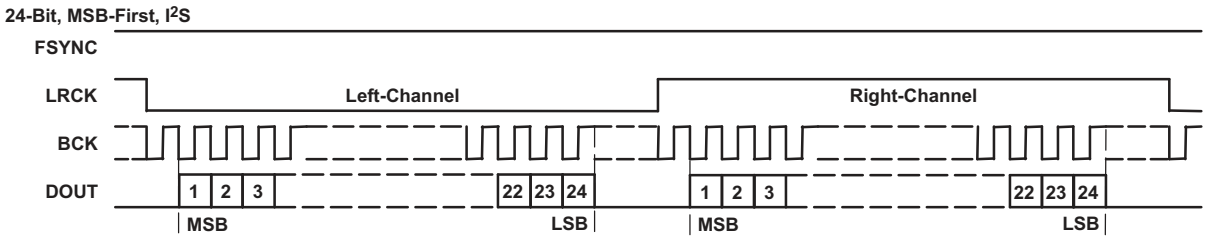
7.4.2.2 Interface Timing

Figure 24 and Figure 26 illustrate the interface timing in slave mode and master mode, respectively.

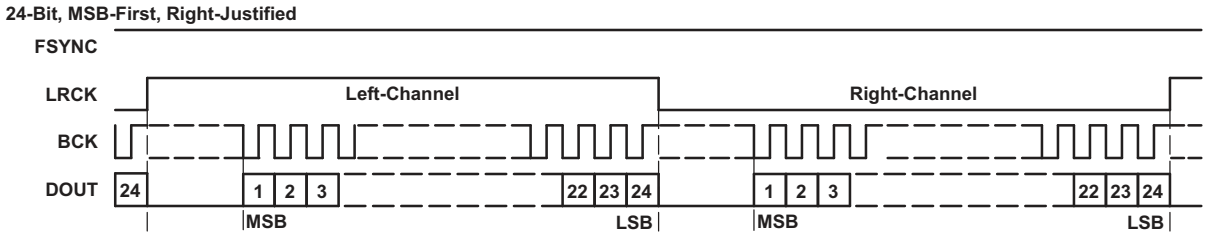
FORMAT 0: FMT[1:0] = 00



FORMAT 1: FMT[1:0] = 01



FORMAT 2: FMT[1:0] = 10



FORMAT 3: FMT[1:0] = 11

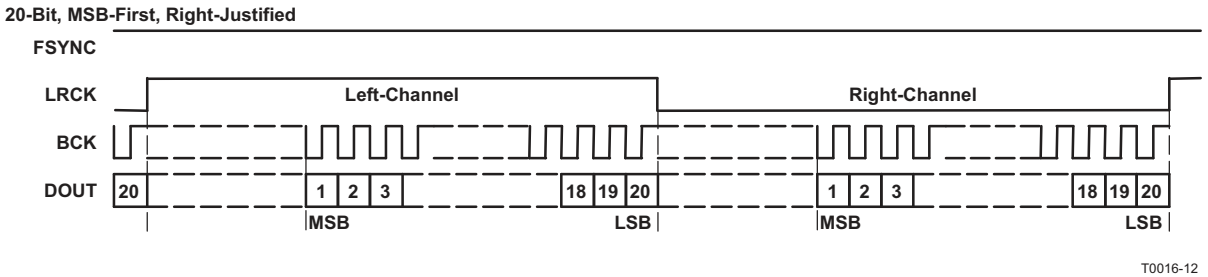
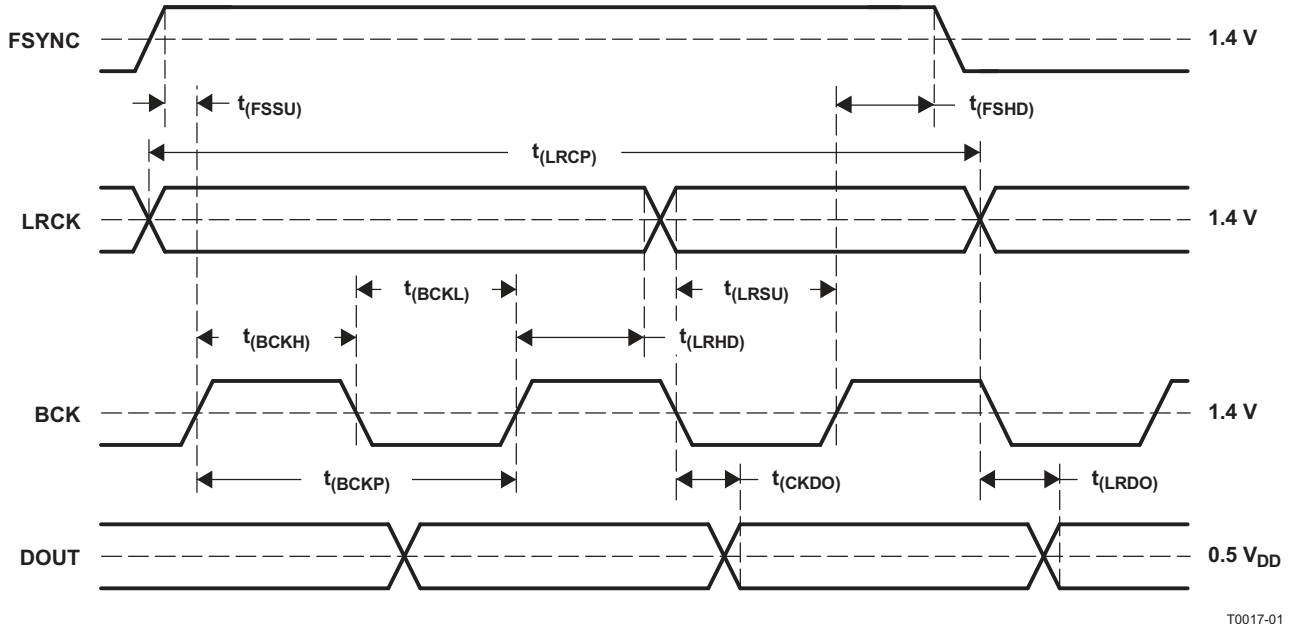


Figure 23. Audio Data Format (Slave Mode: FSYNC, LRCK, and BCK Work as Inputs)



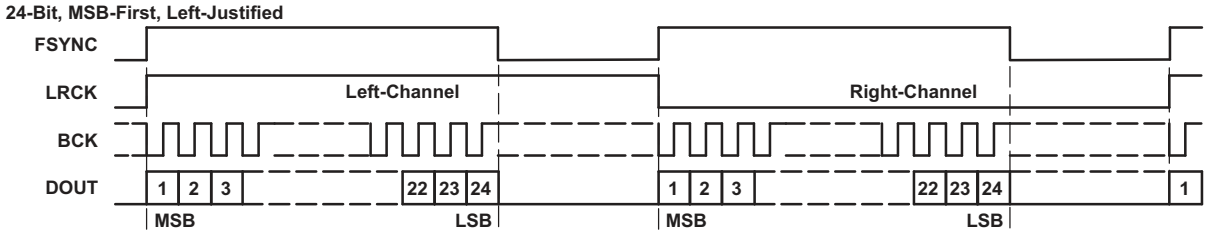
Timing measurement reference level is (V_{IH} + V_{IL}) / 2. Rise and fall times are measured from 10% to 90% of IN to OUT signal swing. Load capacitance of DOUT is 20 pF.

Figure 24. Audio Data Interface Timing (Slave Mode: FSYNC, LRCK, and BCK Work as Inputs)

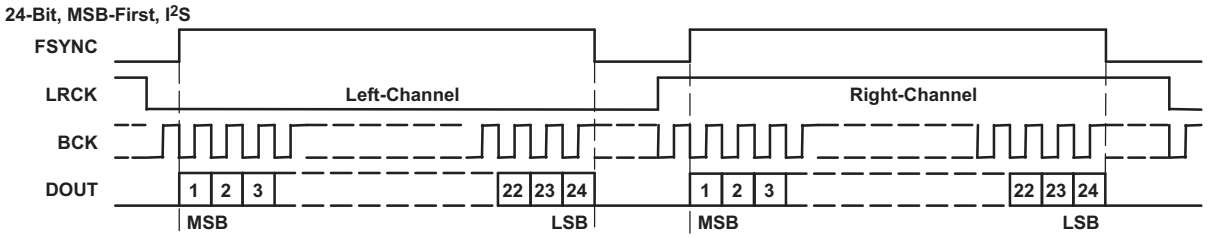
Table 7. Audio Data Interface Timing: Slave Mode

	PARAMETER	MIN	MAX	UNIT
$t_{(BCKP)}$	BCK period	150		ns
$t_{(BCKH)}$	BCK pulse duration, high	60		ns
$t_{(BCKL)}$	BCK pulse duration, low	60		ns
$t_{(LRSU)}$	LRCK setup time to BCK rising edge	40		ns
$t_{(LRHD)}$	LRCK hold time to BCK rising edge	20		ns
$t_{(LRCP)}$	LRCK period	10		µs
$t_{(FSSU)}$	FSYNC setup time to BCK rising edge	20		ns
$t_{(FSHD)}$	FSYNC hold time to BCK rising edge	20		ns
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10	20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10	20	ns
t_r	Rise time of all signals		10	ns
t_f	Fall time of all signals		10	ns

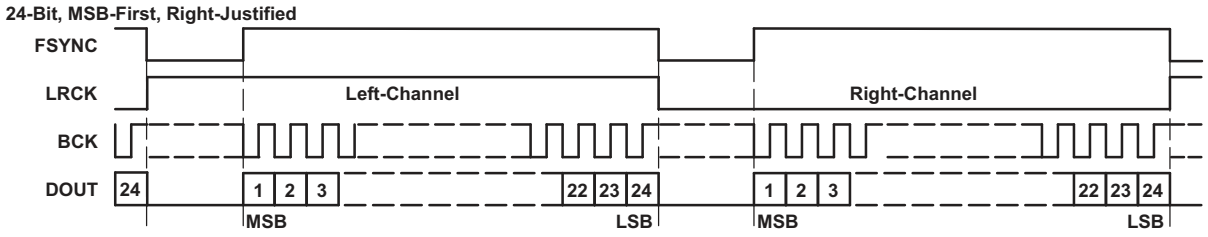
FORMAT 0: FMT[1:0] = 00



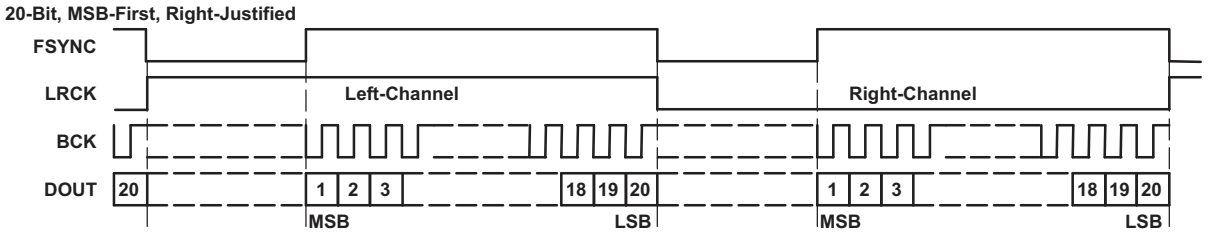
FORMAT 1: FMT[1:0] = 01



FORMAT 2: FMT[1:0] = 10

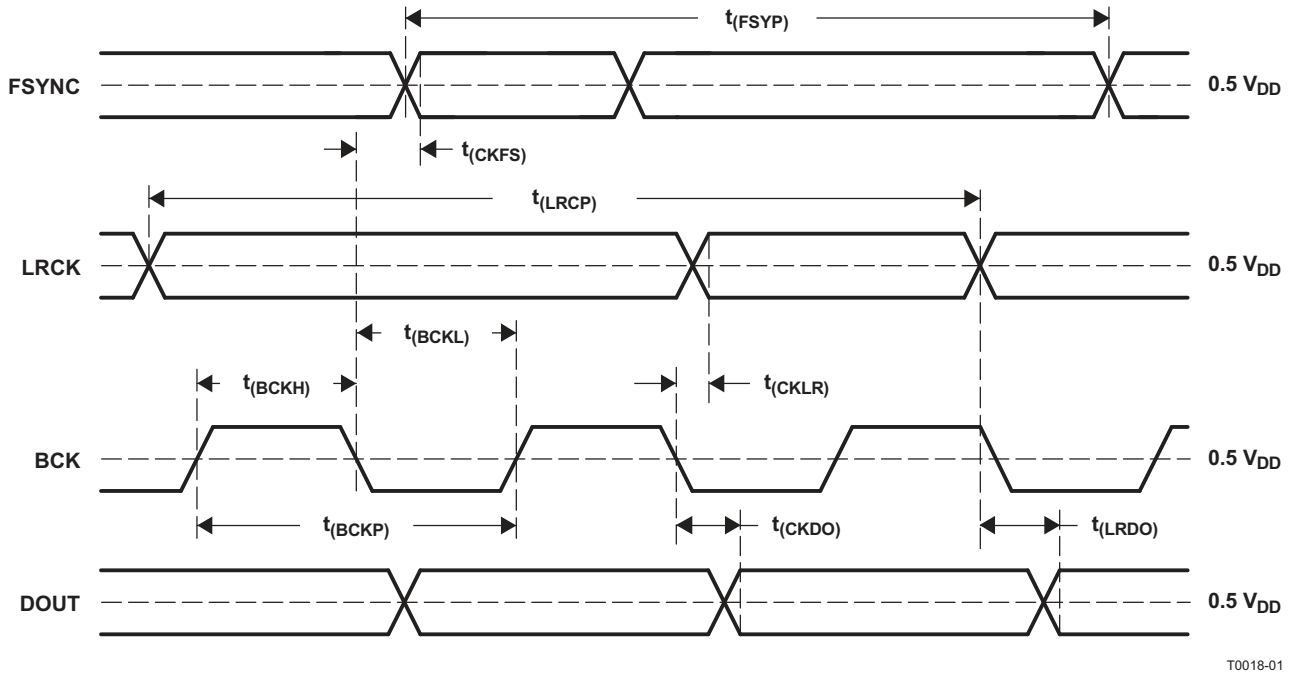


FORMAT 3: FMT[1:0] = 11



T0016-13

Figure 25. Audio Data Format (Master Mode: FSYNC, LRCK, and BCK Work as Outputs)



Timing measurement reference level is (V_{IH} + V_{IL}) / 2. Rise and fall times are measured from 10% to 90% of IN to OUT signal swing. Load capacitance of all signals is 20 pF.

Figure 26. Audio Data Interface Timing (Master Mode: FSYNC, LRCK, and BCK Work as Outputs)

Table 8. Audio Data Interface Timing: Master Mode

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	150	1 / (64 f_S)	1200	ns
$t_{(BCKH)}$	BCK pulse duration, high	75		600	ns
$t_{(BCKL)}$	BCK pulse duration, low	75		600	ns
$t_{(CKLR)}$	Delay time, BCK falling edge to LRCK valid	–10		20	ns
$t_{(LRCP)}$	LRCK period	10	1 / f_S	80	µs
$t_{(CKFS)}$	Delay time, BCK falling edge to FSYNC valid	–10		20	ns
$t_{(FSYP)}$	FSYNC period	5	1 / (2 f_S)	40	µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		20	ns
t_r	Rise time of all signals			10	ns
t_f	Fall time of all signals			10	ns

7.4.2.3 Synchronization With Digital Audio System

In slave mode, the PCM1802 operates under LRCK, synchronized with system clock SCKI. The PCM1802 does not require a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCKs for 64 f_S BCK (±5 BCKs for 48 f_S BCK) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within 1 / f_S and digital output is forced into BPZ code until resynchronization between LRCK and SCKI is completed.

In the case of changes less than ±5 BCKs for 64 BCK per frame (±4 BCKs for 48 BCK per frame), resynchronization does not occur.

Figure 27 illustrates the digital output response for loss of synchronization and resynchronization. During undefined data, some noise might be generated in the audio signal. The transition of normal to undefined data and undefined or zero data to normal creates a data discontinuity in the digital output, which generates some noise in the audio signal.

TI recommends setting $\overline{\text{PDWN}}$ low to achieve stable analog performance when the sampling rate, interface mode, data format, or oversampling control is changed.

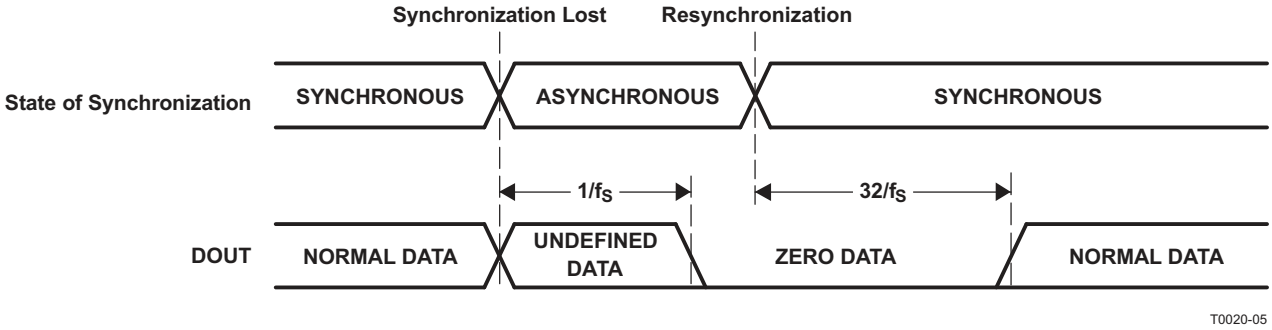


Figure 27. ADC Digital Output for Loss of Synchronization and Resynchronization

7.4.3 Master Mode

In master mode, BCK, LRCK, and FSYNC work as output pins, and these pins are controlled by timing which is generated in the clock circuit of the PCM1802. FSYNC is used to designate the valid data from the PCM1802. The rising edge of FSYNC indicates the starting point of the converted audio data and the falling edge of this signal indicates the ending point of the data. The frequency of this signal is fixed at 2 × LRCK. The duty cycle ratio depends on data bit length. The frequency of BCK is fixed at 64 × LRCK. The 768-f_S system clock is not available in master mode.

7.4.4 Slave Mode

In slave mode, BCK, LRCK, and FSYNC work as input pins. FSYNC enables the BCK signal, and the device can shift out the converted data while FSYNC is HIGH. The PCM1802 accepts the 64-f_S BCK or the 48-f_S BCK format. The delay of FSYNC from the LRCK transition must be within 16 BCKs for the 64-f_S BCK format and within 12 BCKs for the 48-f_S BCK format.

7.4.5 Interface Mode

The PCM1802 supports master mode and slave mode as interface modes, and they are selected by MODE1 and MODE0 as shown in Table 9.

In master mode, the PCM1802 provides the timing for serial audio data communications between the PCM1802 and the digital audio processor or external circuit. In slave mode, the PCM1802 receives the timing for data transfer from an external controller.

Table 9. Interface Mode

MODE1	MODE0	INTERFACE MODE
0	0	Slave mode (256 f_S, 384 f_S, 512 f_S, 768 f_S)
0	1	Master mode (512 f_S)
1	0	Master mode (384 f_S)
1	1	Master mode (256 f_S)

8 Application and Implementation

NOTE

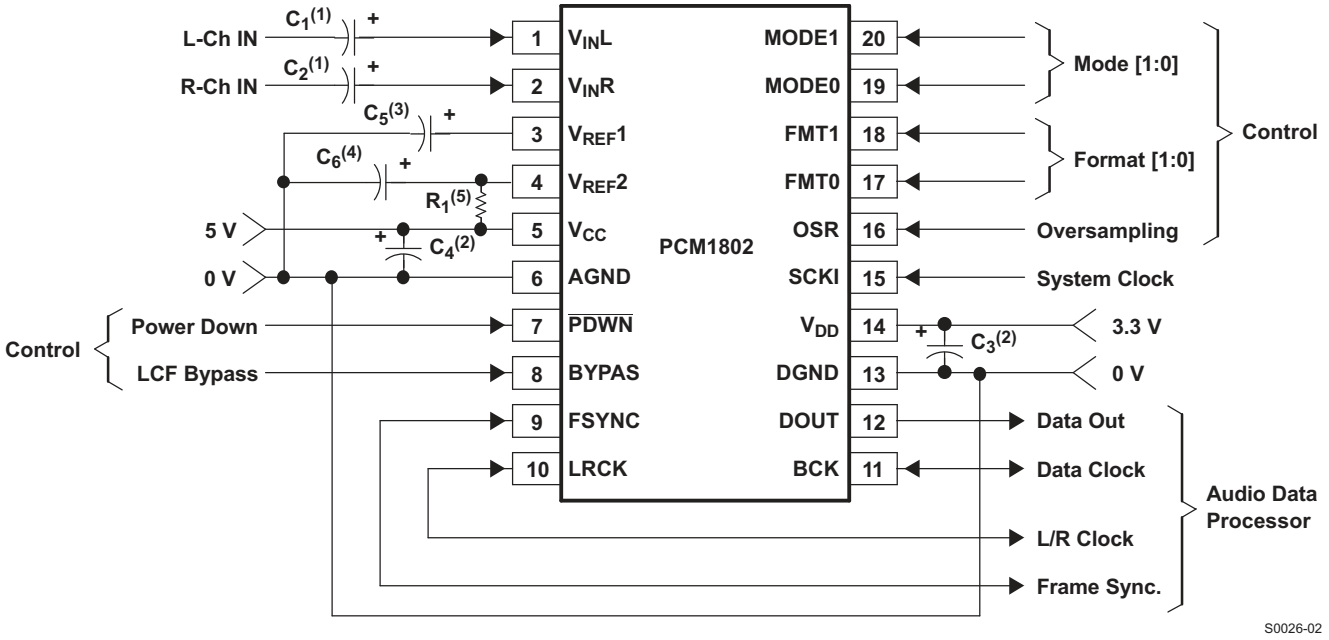
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PCM1802 device is suitable for wide variety of cost-sensitive consumer applications requiring good performance and operation with a 5-V analog supply and 3.3-V digital supply.

8.2 Typical Application

Figure 28 illustrates a typical circuit connection diagram in which the cutoff frequency of the input HPF is about 8 Hz.



(1) C_1, C_2: A 1-µF capacitor gives a 8-Hz (τ = 1 µF × 20 kΩ) cutoff frequency for input HPF in normal operation and requires a power-on settling time with a 20-ms time constant during the power-on initialization period.

(2) C_3, C_4: Bypass capacitors, 0.1-µF ceramic and 10-µF tantalum, depending on layout and power supply

(3) C_5: TI recommends 0.1-µF ceramic and 10-µF tantalum capacitors.

(4) C_6: TI recommends 0.1-µF ceramic and 10-µF tantalum capacitors when using a noisy analog power supply. These capacitor are not required for a clean analog supply.

(5) R_1: TI recommends a 1-kΩ resistor when using a noisy analog power supply. This resistor is shorted for a clean analog supply.

Figure 28. Typical Circuit Connection

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 10 as the input parameters.

Table 10. Design Parameters

PARAMETER	VALUE
Analog input voltage	0 $V_{P–P}$ to 3 $V_{P–P}$
Output	PCM audio data
System clock input frequency	2.048 MHz to 49.152 MHz
Output sampling frequency	8 kHz to 96 kHz
Power supply	3.3 V and 5 V

8.2.2 Detailed Design Procedure

8.2.2.1 Control Pins

The FMT, MODE, OSR, and BYPASS control pins are controlled by tying up to VDD, down to GND, or driven with GPIO from the DSP or audio processor.

8.2.2.2 DSP or Audio Processor

In this application a DSP or audio processor acts as the audio master, and the PCM1802 acts as the audio slave. This means the DSP or audio processor must be able to output audio clocks that the PCM1802 can use to process audio signals.

8.2.2.3 Input Filters

For the analog input circuit an AC-coupling capacitor must be placed in series with the input. This removes the DC component of the input signal. An RC filter can also be implemented to filter out of band noise to reduce aliasing. Equation 1 calculates the cutoff frequency of the optional RC filter for the input.

$$f_c = \frac{1}{2\pi RC} \quad (1)$$

8.2.3 Application Curve

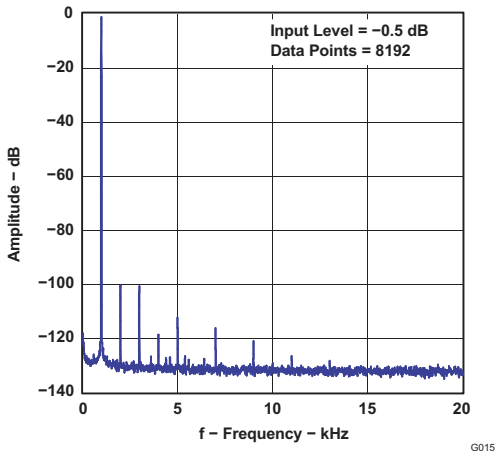


Figure 29. Amplitude vs Frequency

9 Power Supply Recommendations

The PCM1802 requires a 5-V nominal supply and a 3.3-V nominal supply. The 5-V supply is for the analog circuitry powered by the VCC pin. The 3.3-V supply is for the digital circuitry powered by the VDD pin. The decoupling capacitors for the power supplies must be placed close to the device pins.

10 Layout

10.1 Layout Guidelines

10.1.1 VCC and VDD Pins

The digital and analog power supply lines to the PCM1802 must be bypassed to the corresponding ground pins with 0.1-µF ceramic and 10-µF tantalum capacitors as close to the pins as possible to maximize the dynamic performance of the ADC.

10.1.2 AGND and DGND Pins

To maximize the dynamic performance of the PCM1802, the analog and digital grounds are not connected internally. These grounds must have low impedance to avoid digital noise feeding back into the analog ground. They must be connected directly to each other under the parts to reduce the potential noise problem.

10.1.3 VIN Pins

TI recommends a 1-µF capacitor for AC-coupling, which gives an 8-Hz cutoff frequency. A higher full-scale input voltage, if required, can be accommodated by adding only one series resistor to each VIN pin.

10.1.4 VREF1 Pin

TI recommends a ceramic capacitor of 0.1 µF and an electrolytic capacitor of 10 µF between VREF1 and AGND to ensure low source impedance for the ADC references. These capacitors must be placed as close as possible to the VREF1 pin to reduce dynamic errors on the ADC references.

10.1.5 VREF2 Pin

The differential voltage between VREF2 and AGND sets the analog input full-scale range. TI recommends a ceramic capacitor of 0.1 µF and an electrolytic capacitor of 10 µF between VREF2 and AGND with the insertion of a 1-kΩ resistor between VCC and VREF2 when using a noisy analog power supply. These capacitors and resistor are not required for a clean analog supply. These capacitors must be placed as close as possible to the VREF2 pin to reduce dynamic errors on the ADC references. Full-scale input level is affected by this 1-kΩ resistor, decreasing by 3%.

10.1.6 DOUT Pin

The DOUT pin has enough load drive capability, but TI recommends placing a buffer near the PCM1802 and minimizing load capacitance if the DOUT line is long, to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

10.1.7 System Clock

The quality of the system clock can influence dynamic performance, as the PCM1802 operates based on the system clock. In slave mode, it may be necessary to consider the system-clock duty cycle, jitter, and the time difference between the system clock transition and the BCK or LRCK transition.

10.2 Layout Example

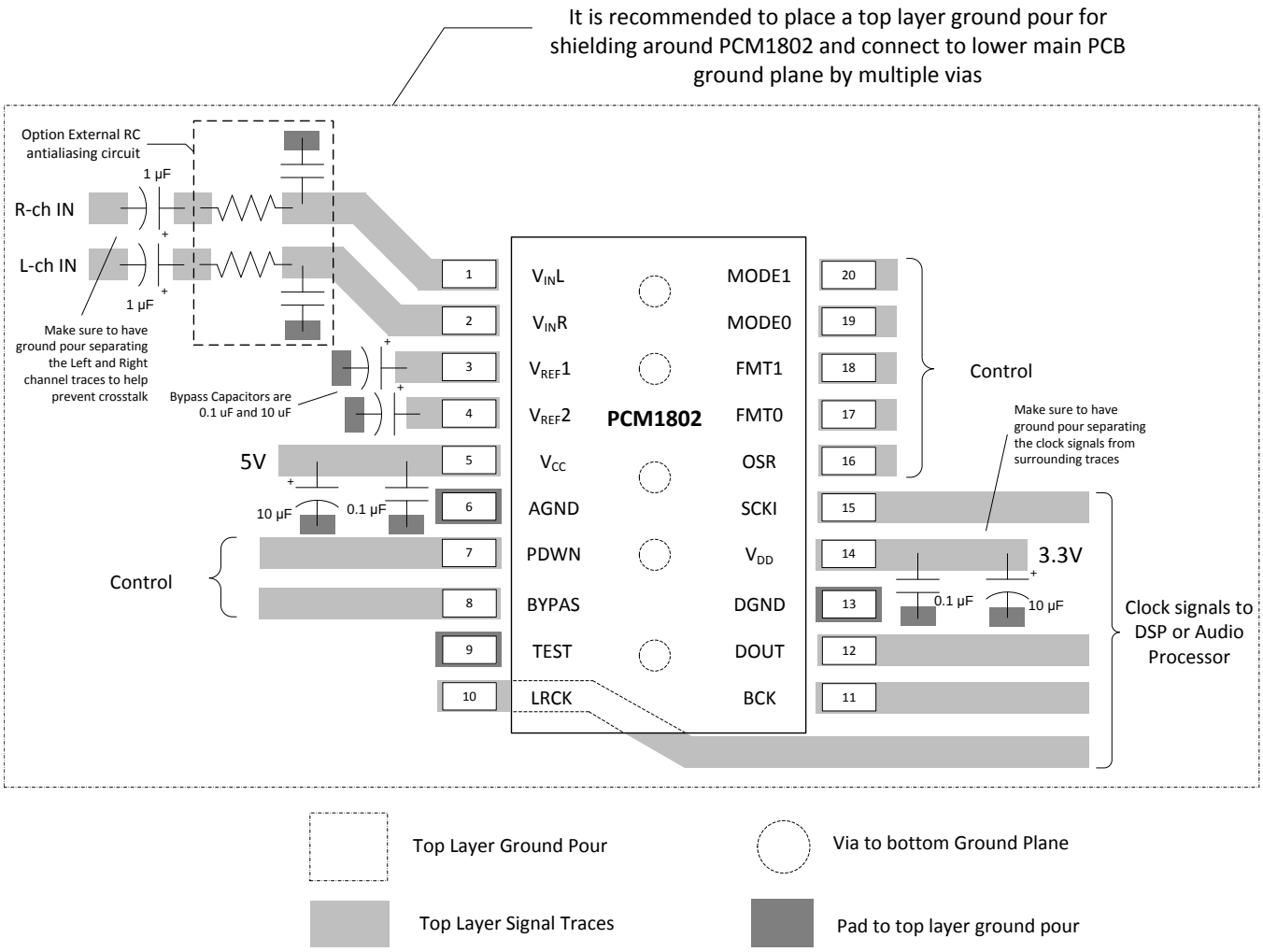


Figure 30. Layout Recommendation

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
System Two, Audio Precision are trademarks of Audio Precision.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1802DB	ACTIVE	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1802	Samples
PCM1802DBG4	ACTIVE	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1802	Samples
PCM1802DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1802	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

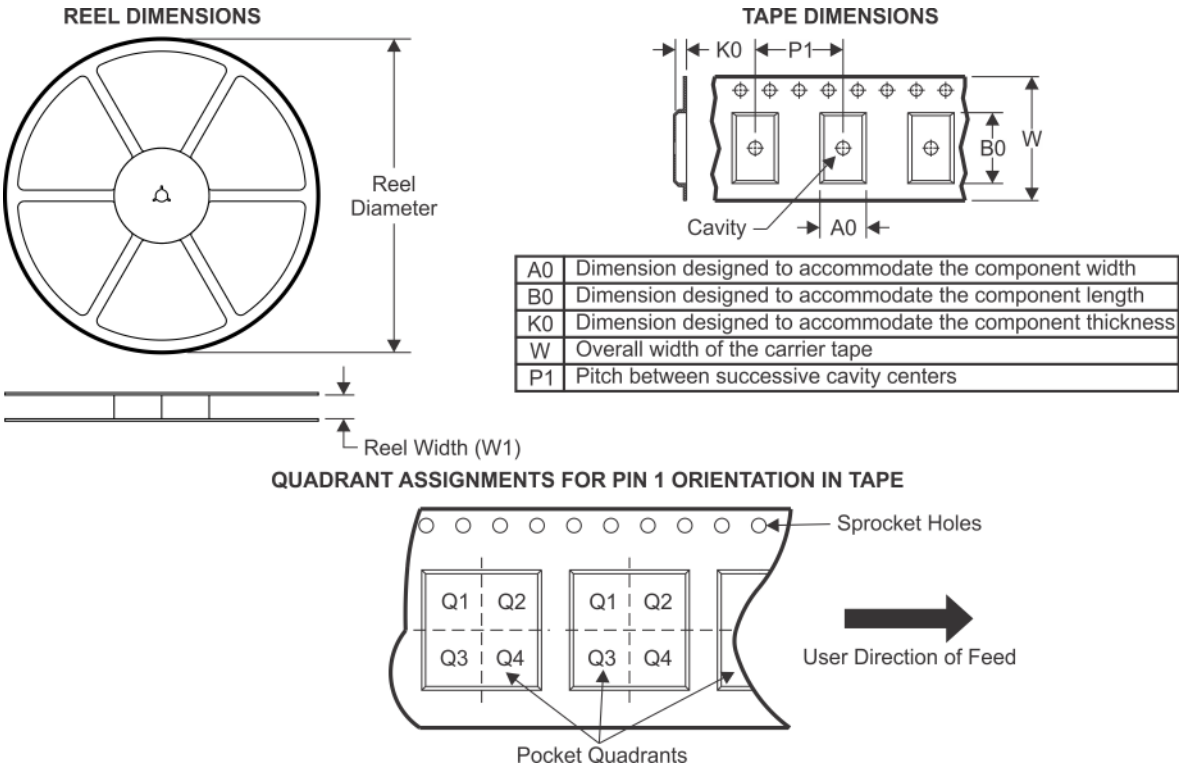
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

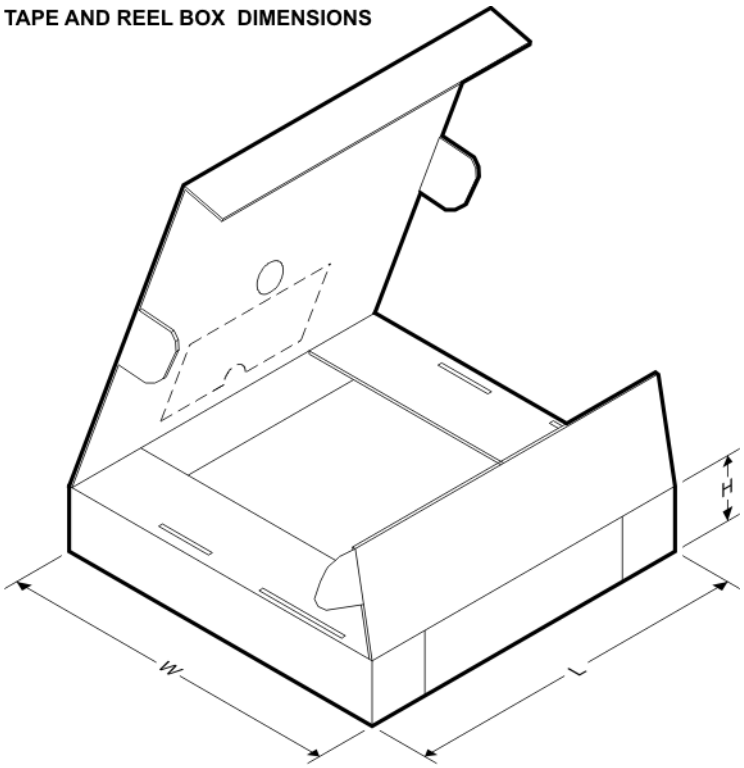


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1802DBR	SSOP	DB	20	2000	330.0	17.4	8.5	7.6	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

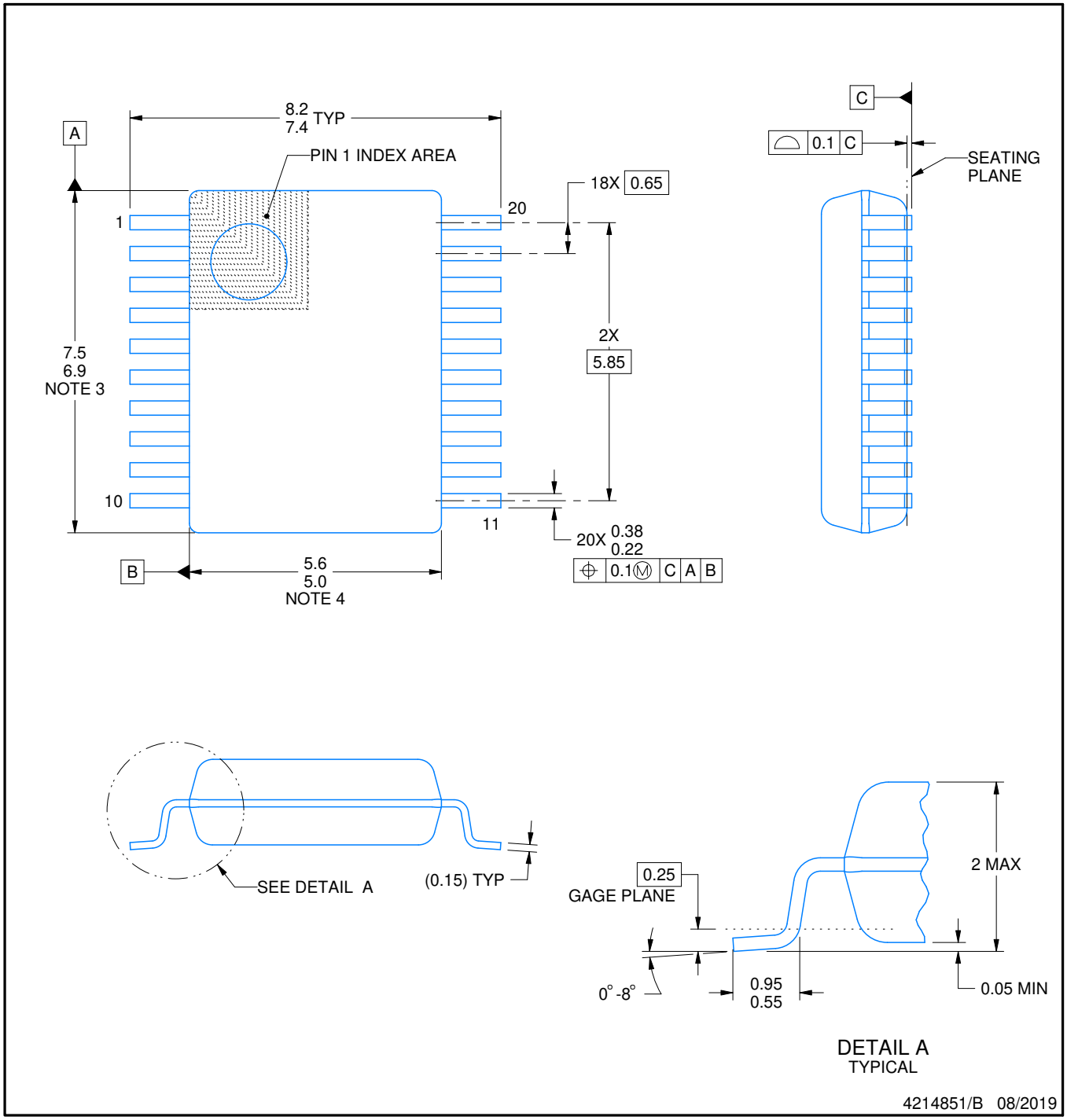
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1802DBR	SSOP	DB	20	2000	336.6	336.6	28.6

PACKAGE OUTLINE

DB0020A

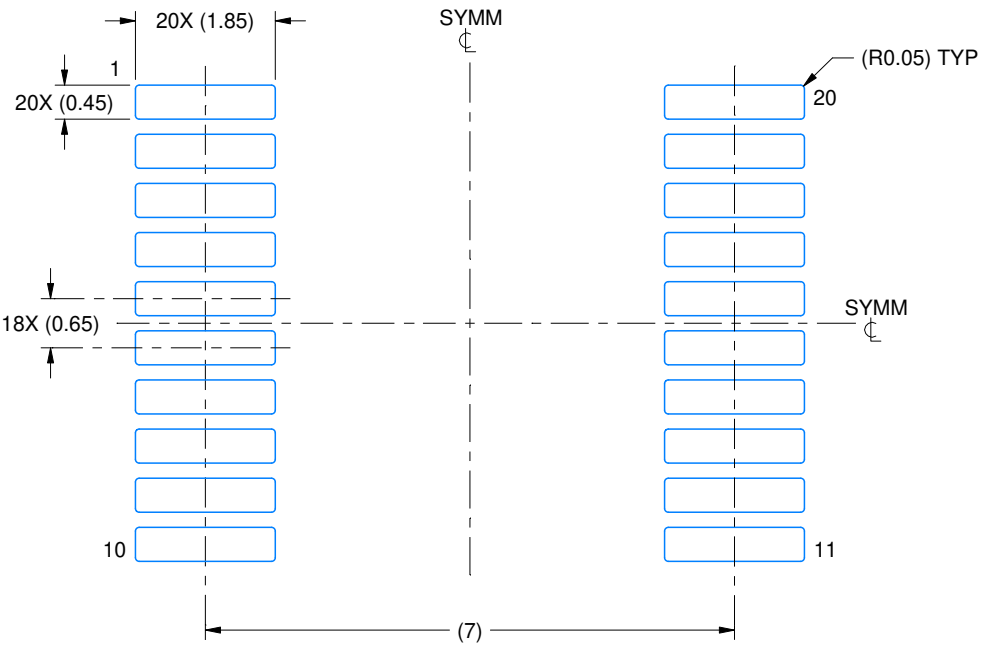
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

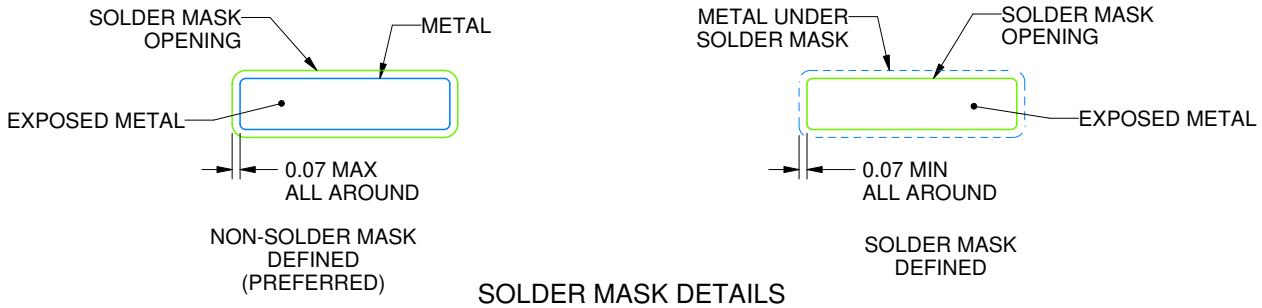


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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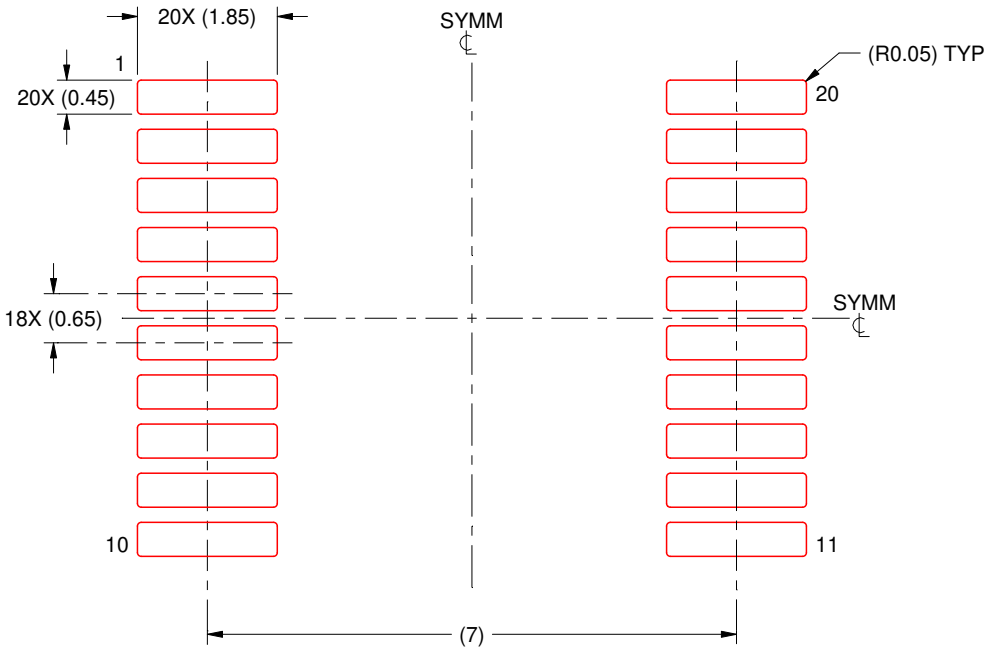
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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