

ORDERING INFORMATION

| Part Number | Package | Top Marking | Free Air Temperature (T _A) |
|-------------|---------|-------------|--|
| MP24943DS* | SOIC8 | MP24943 | -40°C to +85°C |
| MP24943DN** | SOIC8E | MP24943 | -40°C to +85°C |

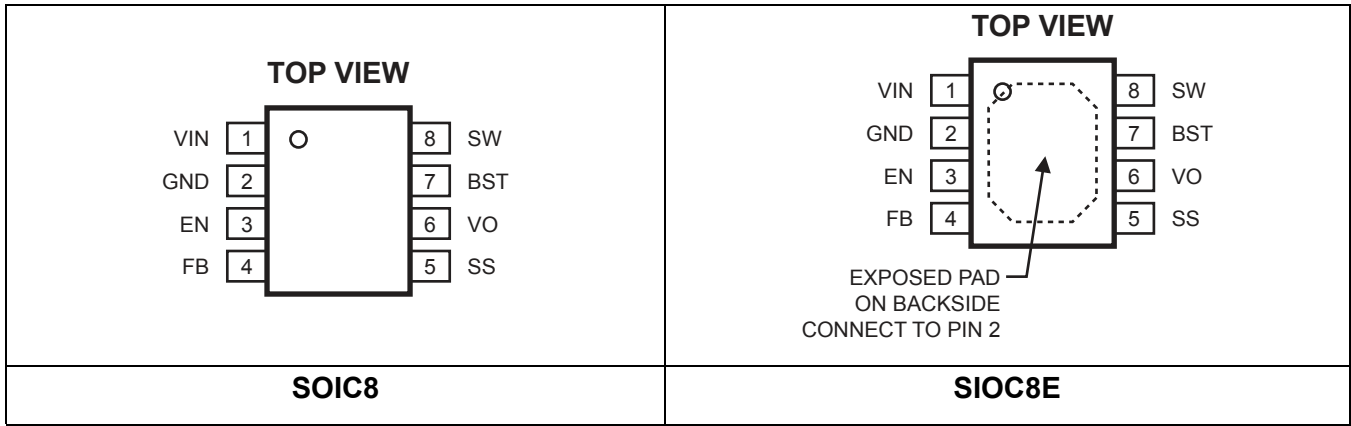
* For Tape & Reel, add suffix -Z (eg. MP24943DS-Z);

For RoHS, compliant packaging, add suffix -LF (eg. MP24943DS-LF-Z).

** For Tape & Reel, add suffix -Z (eg. MP24943DN-Z);

For RoHS, compliant packaging, add suffix -LF (eg. MP24943DN-LF-Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

| | |
|---|-----------------------------------|
| Input Voltage V _{IN} | 60V |
| V _{SW} | -0.3V to (V _{IN} + 0.3V) |
| V _{BST} | V _{SW} + 6.5V |
| All Other Pins..... | -0.3V to +6.5V |
| Junction Temperature..... | 150°C |
| Lead Temperature..... | 260°C |
| Storage Temperature..... | -65°C to +150°C |
| Continuous Power Dissipation (T _A = 25°C) ⁽²⁾ | |
| SOIC8..... | 1.38W |
| SOIC8E..... | 2.5W |

Recommended Operating Conditions ⁽³⁾

| | |
|---|-------------|
| Input Voltage V _{IN} | 4.5V to 55V |
| Output Voltage V _{OUT} | 0.8V to 45V |
| Maximum Junction Temp. (T _J)..... | 125°C |

Thermal Resistance ⁽⁴⁾

| | θ _{JA} | θ _{JC} |
|-------------|-----------------|-----------------|
| SOIC8..... | 90..... | 45... °C/W |
| SOIC8E..... | 50..... | 10... °C/W |

Notes:

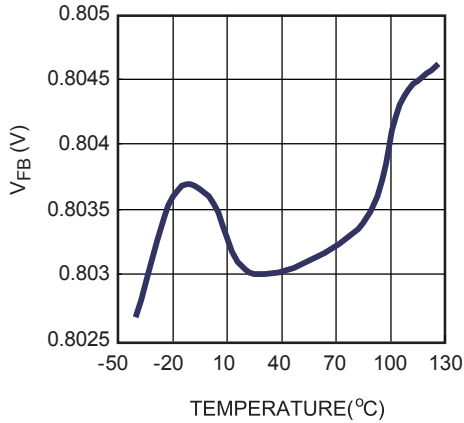
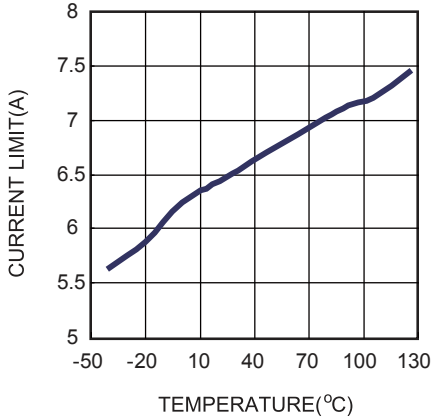
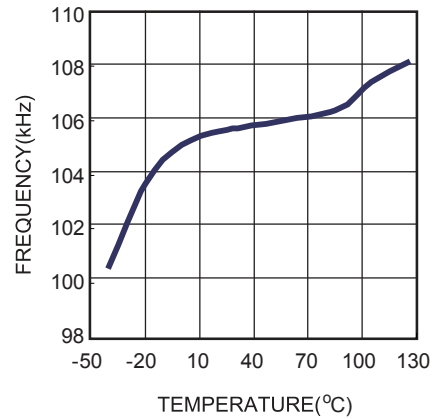
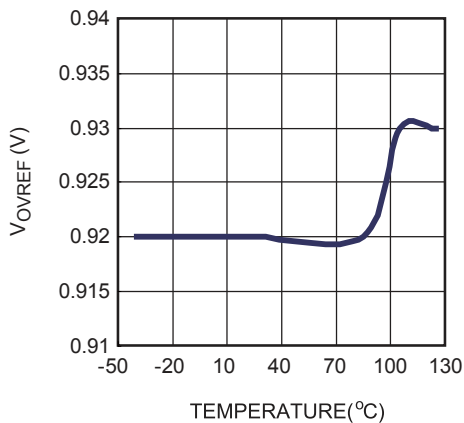
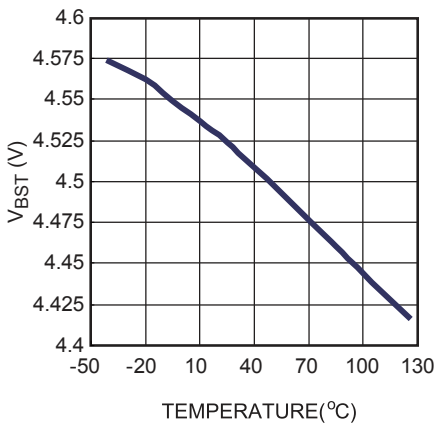
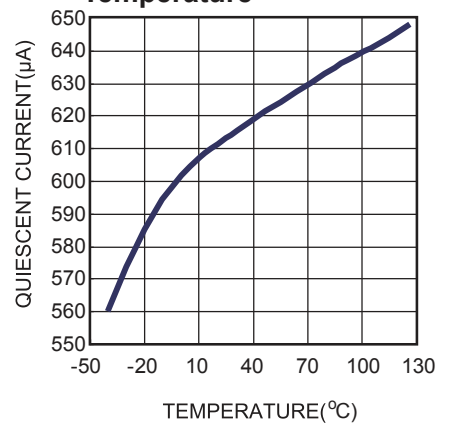
- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS
 $V_{IN} = 12V$, $T_A = 25^{\circ}C$, unless otherwise noted.

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|--|--------------------|-------------------------------|------|-------|------|-------------|
| Feedback Voltage | V_{FB} | $4.5V \leq V_{IN} \leq 55V$ | 0.78 | 0.80 | 0.82 | V |
| Feedback Bias Current | $I_{BIAS(FB)}$ | $V_{FB} = 0.8V$ | -100 | 10 | 100 | nA |
| Output Over-Voltage Reference | V_{OVREF} | | 0.88 | 0.92 | 0.96 | V |
| Switch-On Resistance | $R_{DS(ON)}$ | | | 0.125 | 0.15 | Ω |
| Switch Leakage | | $V_{EN} = 0V$, $V_{SW} = 0V$ | | 0.1 | 1 | μA |
| Current Limit | | Duty Cycle=10% | 5.5 | 6.5 | 8 | A |
| Oscillator Frequency | f_{SW} | $V_{FB} = 0.6V$ | 70 | 100 | 140 | kHz |
| Bootstrap Voltage | $V_{BST} - V_{SW}$ | | | 4.3 | 5.5 | V |
| Minimum-On Time | t_{ON} | | 50 | 100 | 250 | ns |
| SW-rising edge | t_{rise} | | | 50 | 100 | ns |
| SW-falling edge | t_{fall} | | | 50 | 100 | ns |
| EN-Input Low Voltage | | | | | 0.4 | V |
| EN-Input High Voltage | | | 1.8 | | | V |
| EN-Input Bias Current | | $V_{EN}=0-6V$ | -10 | -2 | 10 | μA |
| Under-Voltage Lockout Threshold Rising | | | 3.0 | 3.3 | 3.6 | V |
| Under-Voltage Lockout Threshold Hysteresis | | | 200 | | | mV |
| Supply Current (Shutdown) | | $V_{EN}=0V$ | | 4 | 10 | μA |
| Supply Current (Quiescent) | | $V_{EN} = 2V$, $V_{FB} = 1V$ | | 650 | 800 | μA |
| Thermal Shutdown | | | | 150 | | $^{\circ}C$ |

PIN FUNCTIONS

| Package Pin # | Name | Description |
|---------------|------------------|---|
| 1 | VIN | Supply Voltage. Unregulated input can range from 4.5V to 55V. Input capacitor (C_{IN}) required to decouple input. Provides drain for internal power device and power supply. |
| 2 | GND, Exposed Pad | Ground. Voltage reference for the regulated output voltage. Layout requires special attention: this node must be placed outside of the D1-to- C_{IN} ground path to prevent current spikes from inducing voltage noise. Connect exposed pad to GND plane for optimal thermal performance. |
| 3 | EN | Enable Input. Pull this pin below the specified threshold to shut the chip down. Pull it above the specified threshold enables the chip. |
| 4 | FB | Feedback. Use an external resistor divider from V_{OUT} to GND tapped to the FB pin to set the output voltage. |
| 5 | SS | Soft-Start. Connect to an external capacitor for Soft-Start. |
| 6 | VO | Output Over-Voltage Protection. Connect VO to the tap of an external resistor divider from V_{OUT} to GND. The OVP reference is 0.9V. |
| 7 | BST | Bootstrap. Requires a capacitor to drive the power switch's gate above the supply voltage. Connect this capacitor between SW and BST pins to form a floating supply across the power switch driver. An on-chip regulator charges up the bootstrap capacitor. If the on-chip regulator is not strong enough, one optional diode can be connected from V_{IN} or V_{OUT} to charge the external boot-strap capacitor. |
| 8 | SW | Switch Output. Output supply. |

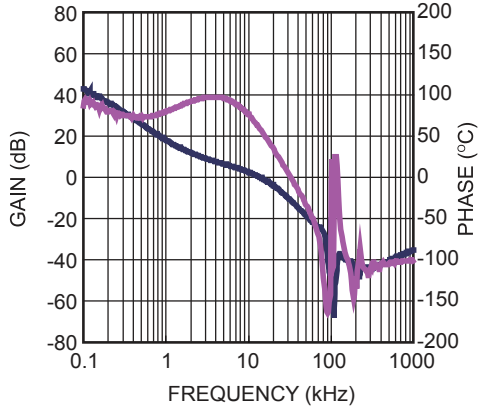
TYPICAL CHARACTERISTICS
 $V_{IN}=12V$
 V_{FB} vs. Temperature

Current Limit vs. Temperature

Frequency vs. Temperature

 V_{OVREF} vs. Temperature

 V_{BST} vs. Temperature

Quiescent Current vs. Temperature


TYPICAL PERFORMANCE CHARACTERISTICS

C1=220μF, C2=2.2μF, C3=100μF, C4=22μF, L=33μH, T_A=25°C, unless otherwise noted.

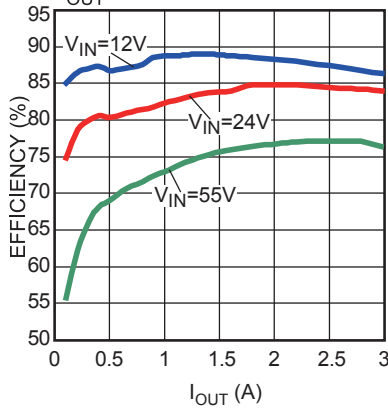
Loop Gain with Phase Margin

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, Resistor Load

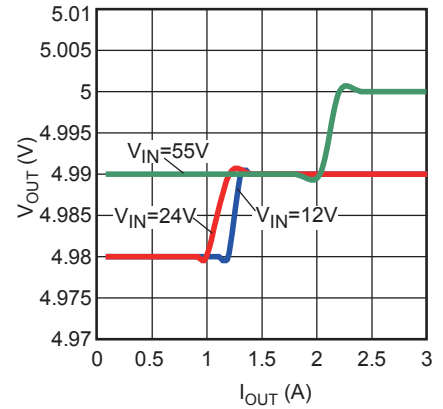


Efficiency vs. Output Current

V_{OUT}=5V

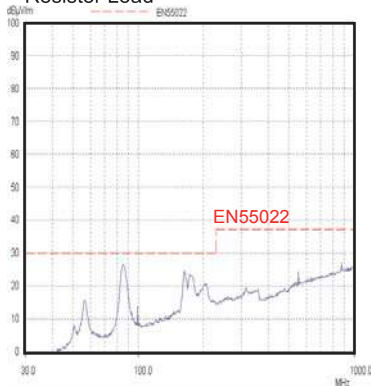


Load Regulation



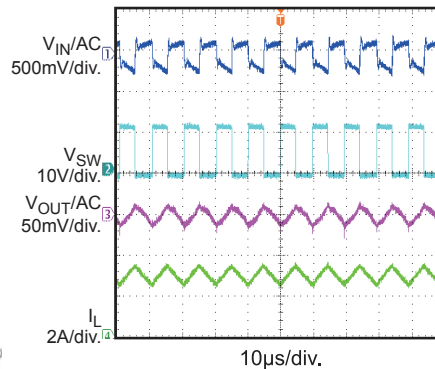
EMI Radiation

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, Resistor Load



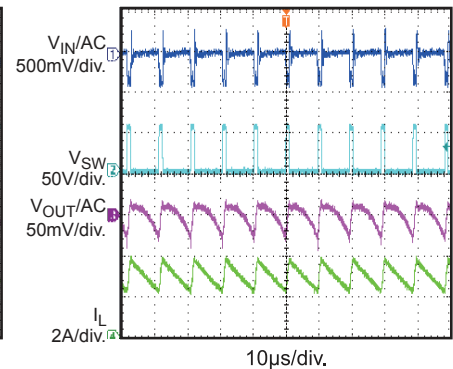
Steady State

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, E-Load



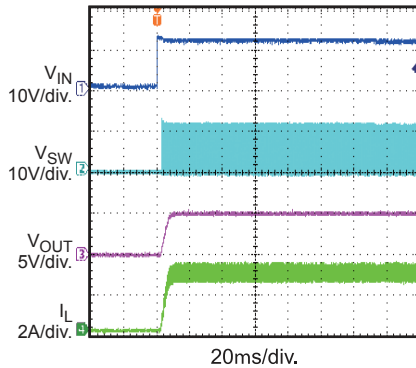
Steady State

V_{IN} = 55V, V_{OUT} = 5V, I_{OUT} = 3A, E-Load



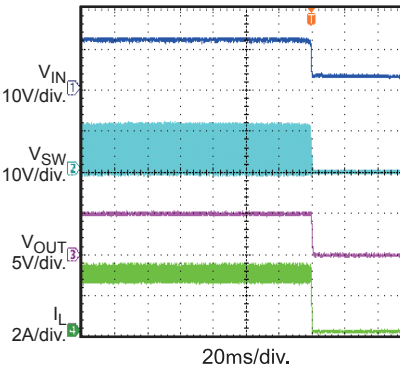
Power Ramp Up

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, Resistor Load



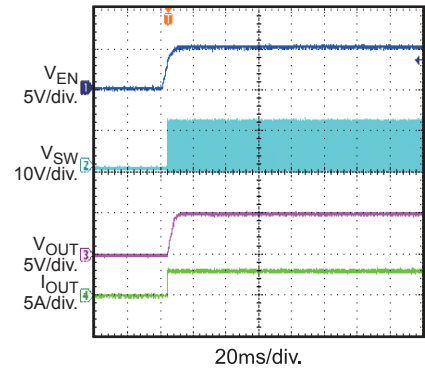
Power Ramp Down

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, Resistor Load



Enable Start Up

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, Resistor Load

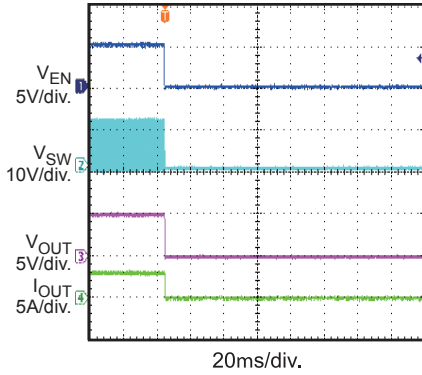


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

C1=220µF, C2=2.2µF, C3=100µF, C4=22µF, L=33µH, T_A=25°C, unless otherwise noted.

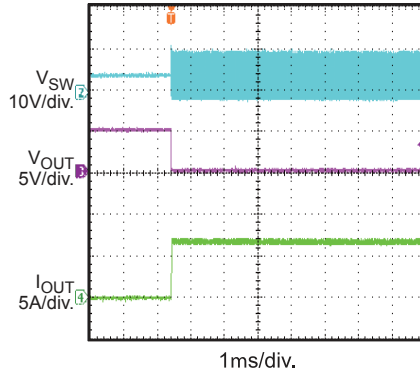
Enable Shutdown

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A,
Resistor Load



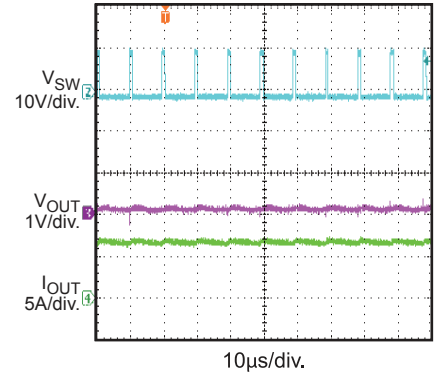
Short Circuit Enter

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A



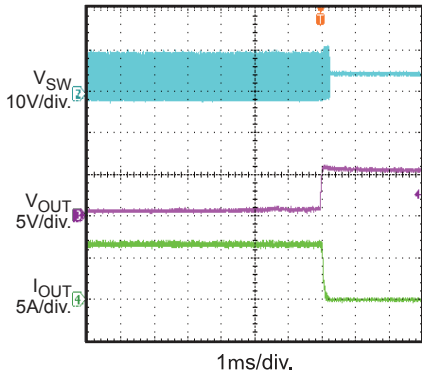
Short Circuit Steady

V_{IN} = 12V, V_{OUT} = 5V



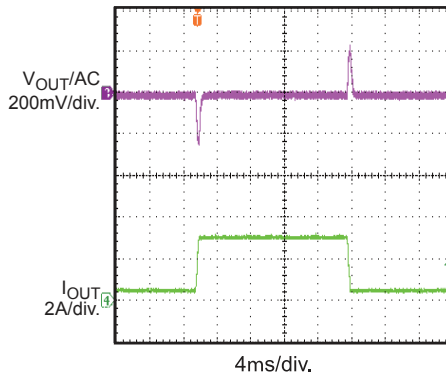
Short Circuit Recovery

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A



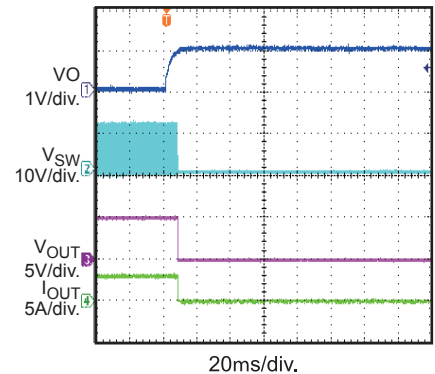
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A,
Slew Rate=6.4mA/µs



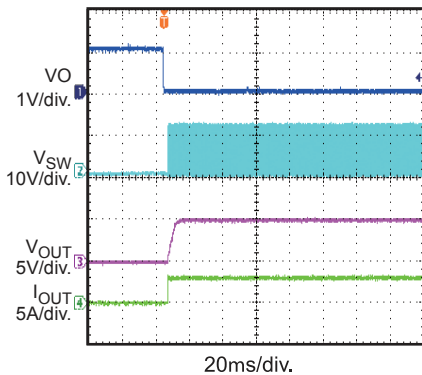
OVP Enter

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A,
E-Load



OVP Recovery

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A,
E-Load



OPERATION

Main Control Loop

The MP24943 is a current-mode buck regulator where the error amplifier (EA) output voltage is proportional to the peak inductor current.

At the beginning of the cycle, SW is off, the EA output voltage is higher than the current sense amplifier (CSA) output, and output of the current limit comparator is low. The rising edge of the 100kHz CLK signal sets the RS flip-flop: this turns on the internal switch, which then connects SW and the inductor to the input supply.

The CSA detects the current flow through the internal switch. If the sum of the CSA output and the slope compensation output exceeds the EA output voltage, the RS flip-flop resets, and the MP24943 reverts to its initial SW off state—otherwise, the falling edge of the CLK resets the flip-flop.

The EA amplifies the voltage difference between V_{FB} and the 0.8V reference. When V_{FB} is less than the 0.8V reference, the EA output is proportional to the inductor current. An external Schottky diode (D1) carries the inductor current when SW is off.

Enable Control

The MP24943 has an enable-control pin (EN): driving EN above 1.8V turns on MP24943, while driving EN below 0.4V turns it off. Connect EN to V_{IN} for automatic start-up.

Output Over-Voltage Protection

The MP24943 has output over-voltage protection (OVP), where V_{OUT} connects to VO through an external resistor divider, and a 0.9V reference on the negative input of the OVP comparator. If the voltage on VO pin is greater than 0.9V, the high-side switch turns off after a short delay, and the soft-start capacitor discharges. If the voltage is less than 0.9V, the part restarts automatically.

FUNCTIONAL BLOCK DIAGRAM

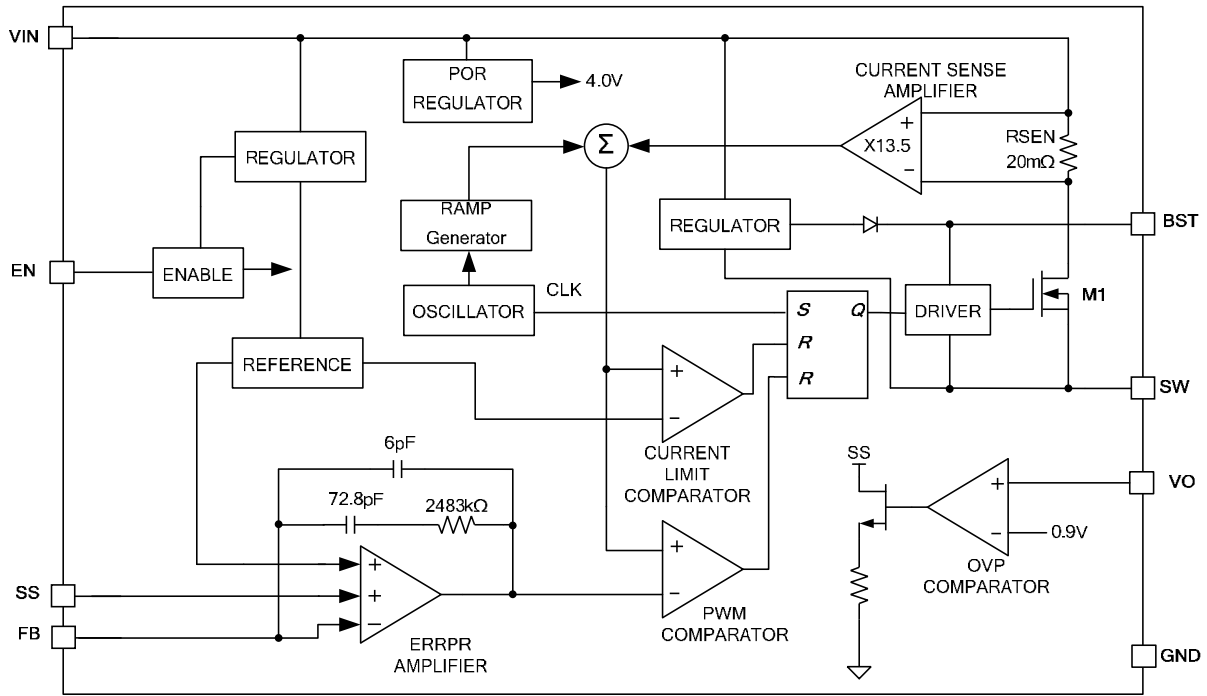


Figure 1—Functional Block Diagram

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider—R1 and R2—sets V_{OUT} (see the Typical Application Circuit on the front page). R1 also sets the feedback loop bandwidth with the internal compensation capacitors (see Figure 1). Choose R1 to be around 300k Ω for optimal transient response. Choose R2 as determined by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

| V_{OUT} (V) | R1 (k Ω) | R2 (k Ω) |
|---------------|------------------|------------------|
| 1.8 | 301 (1%) | 240 (1%) |
| 2.5 | 301 (1%) | 140 (1%) |
| 3.3 | 301 (1%) | 95.3 (1%) |
| 5 | 301 (1%) | 57.6 (1%) |

Setting the Output OVP Threshold

An external resistor divider—R5 and R6 (see the typical application circuit on the front page)—connected to VO sets the output OVP threshold. Choose R5 to be 301k Ω for reduced power dissipation. Then R6 is given by:

$$R6 = \frac{R5}{\frac{V_{OVP}}{V_{OVREF}} - 1} \text{ (k}\Omega\text{)}$$

Where, V_{OVREF} is the OVP reference, 0.9V, and V_{OVP} is over voltage protection threshold.

Selecting the Inductor

Include an inductor with a value between 22 μ H and 47 μ H and a DC current rating that is at least 25% percent higher than the maximum load current for most applications. For maximum efficiency, the inductor DC resistance should be less than 200m Ω . For most designs, the inductance value can be estimated from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current ripple to be approximately 30% of the maximum load current, 3A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions of <100mA, larger inductance values improve efficiency.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and also the switching noise from the device. Choose a capacitor with a switching-frequency impedance of less than the input source impedance to prevent any high-frequency switching current from flowing to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. Use a 4.7 μ F capacitor for most applications.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures regulator loop stability. Select an output capacitor with a low switching-frequency impedance, preferably ceramic capacitors with X5R or X7R dielectrics.

PC Board Layout

The high frequency path—GND, IN, and SW—should be placed very close to the device with short, direct, and wide traces. Place the input capacitor as close as possible to the IN and GND pins. Place the external feedback resistors next to the FB pin. Keep the SW node short and away from the feedback network.

External Bootstrap Diode

Add an external bootstrap diode when the system has a fixed 5V input or when the power supply generates a 5V output. This helps improve the efficiency of the regulator. The bootstrap diode can be a low-cost one such as IN4148 or BAT54.

This diode is also recommended for high-duty-cycle operation (when $\frac{V_{OUT}}{V_{IN}} > 65\%$) and high output voltage ($V_{OUT} > 12V$) applications.

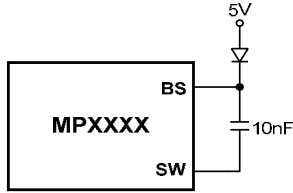


Figure 2—External Bootstrap Diode

Example Design

Below is an example design that follows the application guidelines for the specifications:

| | |
|-----------|----------|
| V_{IN} | 8 to 55V |
| V_{OUT} | 5V |
| F_{SW} | 100kHz |
| V_{OVP} | 6V |

Figure 3 shows the detailed application schematic. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.

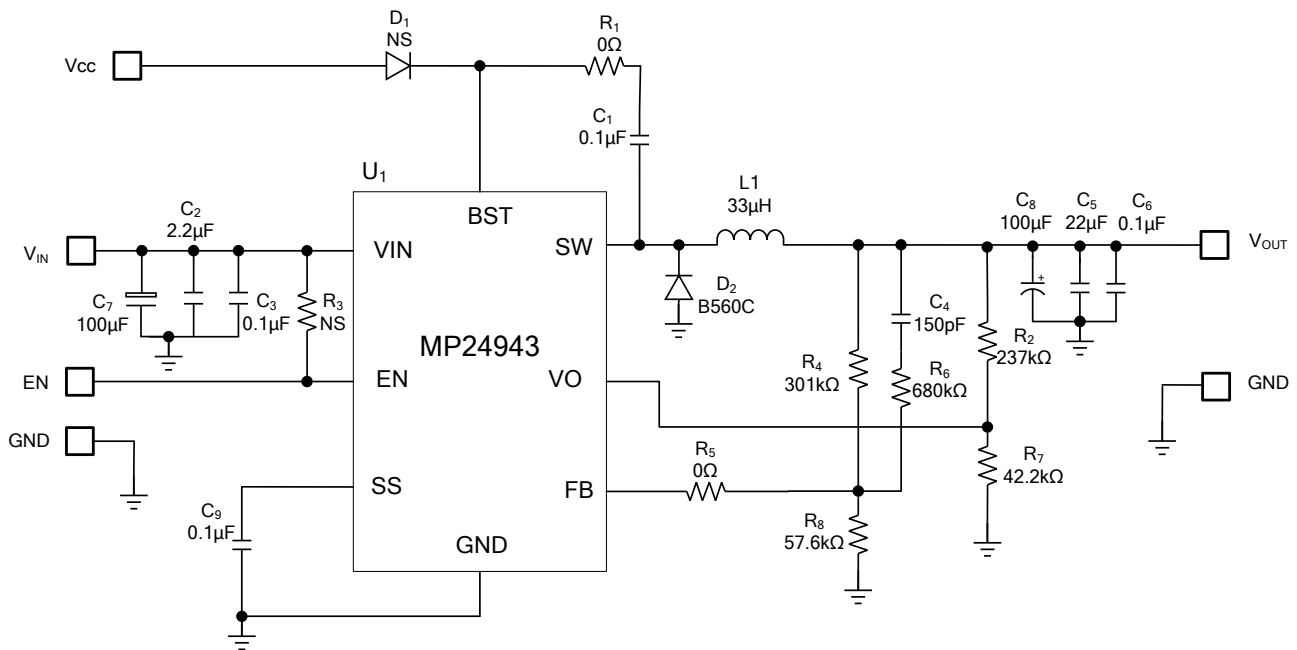
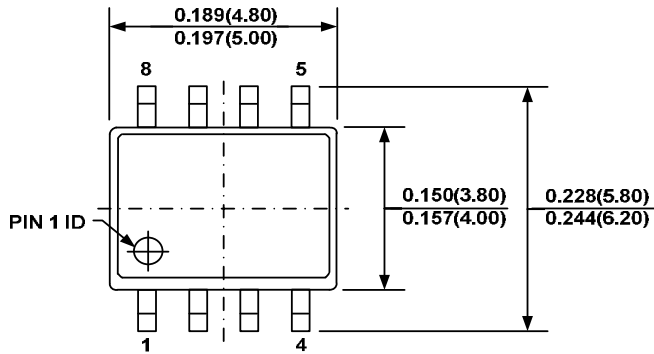
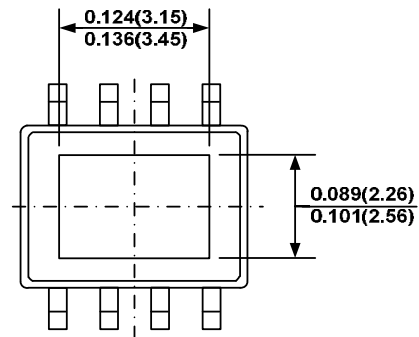
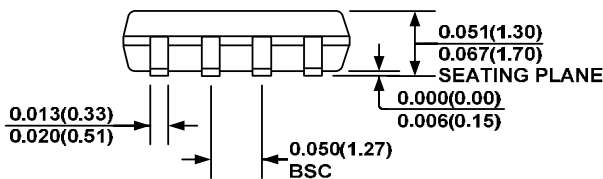
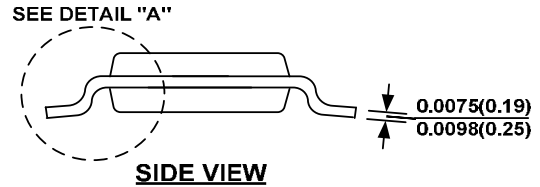
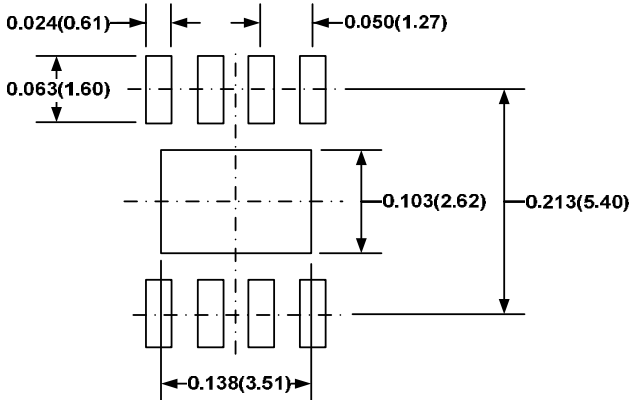
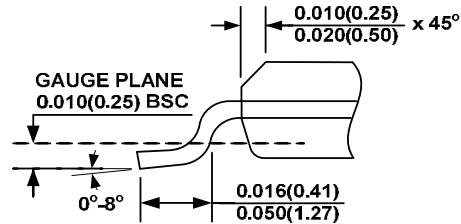
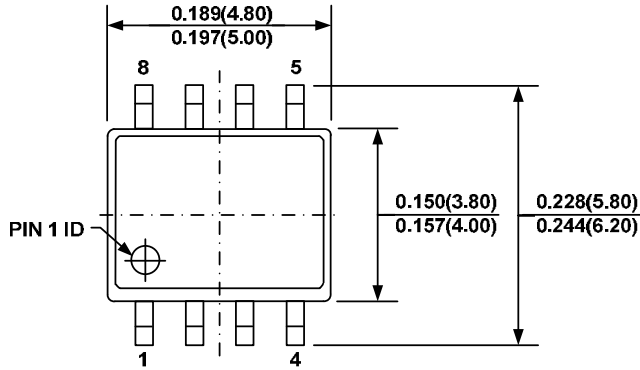
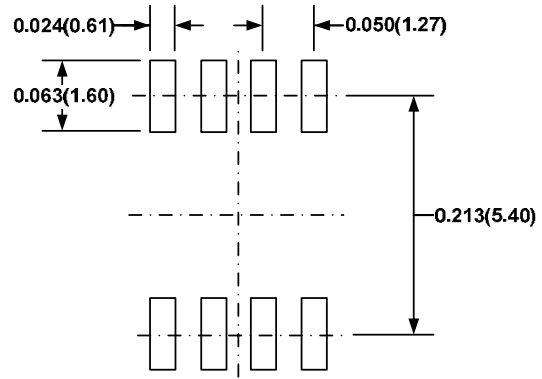
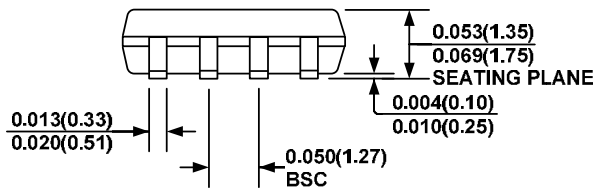
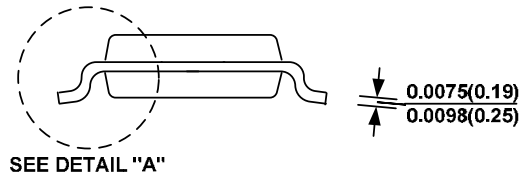
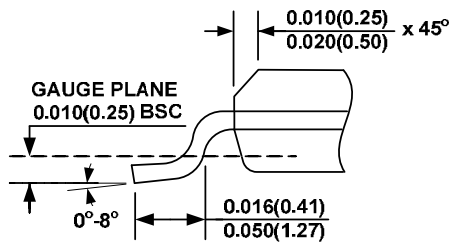


Figure 3—Detailed Application Schematic

PACKAGE INFORMATION
SOIC8E (EXPOSED PAD)

TOP VIEW

BOTTOM VIEW

FRONT VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN

DETAIL "A"
NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION
SOIC8

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

DETAIL "A"
NOTE:

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- 6) DRAWING IS NOT TO SCALE.

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