CY88151A

Spread Spectrum Clock Generator

CY88151A is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. It corresponds to both of the center spread which modulates frequency in modulation off as Middle Centered and down spread which modulates so as not to exceed frequency in modulation off.

Features

	CY88151A-100 (Multiply-by-1)	CY88151A-200 (Multiply-by-2)
Input frequency/ Output frequency	16.6 MHz to 33.4 MHz/ 16.6 MHz to 33.4 MHz	16.6 MHz to 33.4 MHz/ 33.2 MHz to 66.8 MHz
Modulation clock cycle-cycle jitter	Less than100 ps	Less than 100 ps

- Modulation rate : ± 0.5%, ± 1.5% (Center spread), − 1.0%, − 3.0% (Down spread)
- Equipped with oscillation circuit : Range of oscillation 16.6 MHz to 33.4 MHz
- Modulation clock output Duty : 40% to 60%
- Low current consumption by CMOS process : 5 mA (24 MHz : Typ-sample, no load)
- Power supply voltage : 3.3 V ± 0.3 V
- Operating temperature : − 40 °C to + 85 °C
- Package : SOP 8-pin

Contents

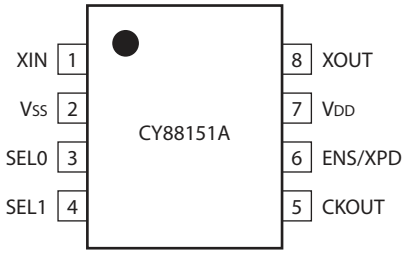
1. Product Lineup

CY88151A has five kinds of multiplication type.

Product	Input Frequency Range	Multiplier Ratio	Output Frequency Range
CY88151A-100	16.6 MHz to 33.4 MHz	Multiply-by-1	16.6 MHz to 33.4 MHz
CY88151A-200		Multiply-by-2	33.2 MHz to 66.8 MHz

2. Pin Assignment

TOP VIEW



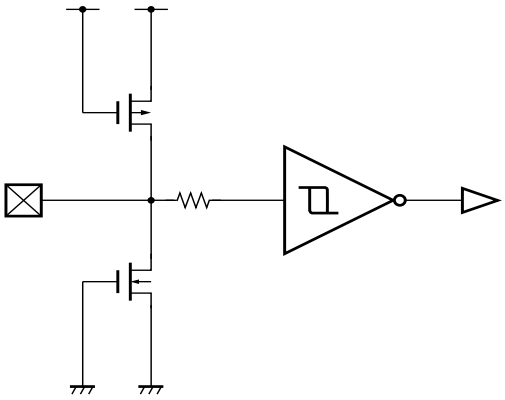
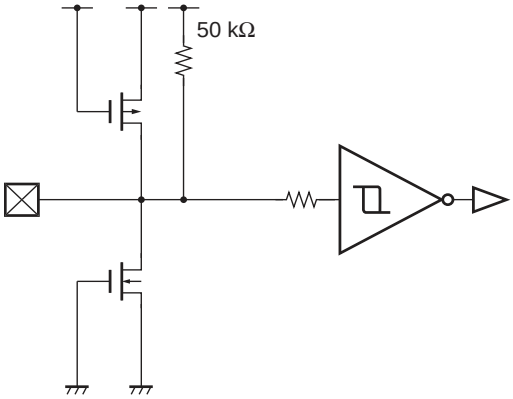
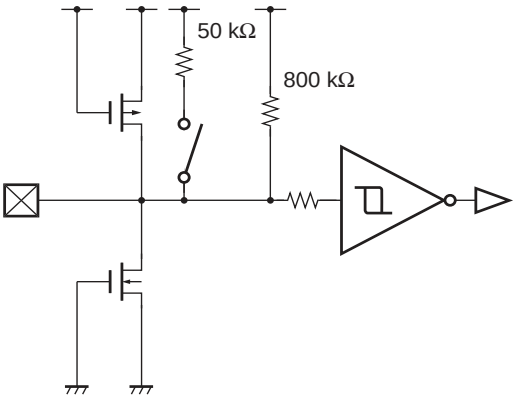
SOB008

3. Pin Description

Pin Name	I/O	Pin No.	Description
XIN	I	1	Resonator connection pin/clock input pin
V_{SS}	—	2	GND pin
SEL0	I	3	Modulation rate setting pin
SEL1	I	4	Modulation rate setting pin
CKOUT	O	5	Modulated clock output pin
ENS/XPD	I	6	Modulation enable setting pin (with pull-up resistance)/ Power down pin (with pull-up resistor)*
V_{DD}	—	7	Power supply voltage pin
XOUT	O	8	Resonator connection pin

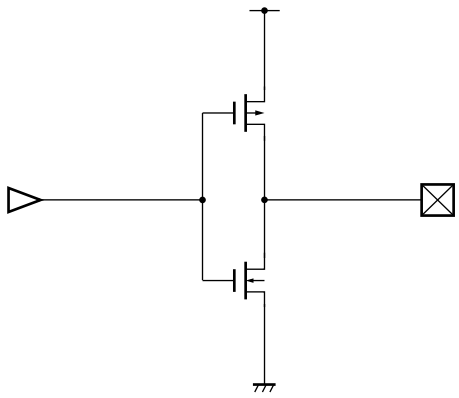
* : XPD = 800 kΩ pull-up resistor at “L”

4. I/O Circuit Type

Pin	Circuit Type	Remarks
SEL0, SEL1		CMOS hysteresis input
ENS		■ With 50 kΩ pull-up resistors ■ CMOS hysteresis input
XPD		■ With 50 kΩ + 800 kΩ pull-up resistors Note : If “L” is input to XPD, 50 kΩ pull-up resistor is disconnected. ■ CMOS hysteresis input

(Continued)

(Continued)

Pin	Circuit Type	Remarks
CKOUT		■ CMOS output ■ I_{OL} = 4 mA

Note : For XIN and XOUT pins, refer to “Oscillation Circuit”.

5. Handling Devices

5.1 Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than V_{DD} or a voltage lower than V_{SS} is applied to an input or output pin or (b) a voltage higher than the rating is applied between V_{DD} pin and V_{SS} pin. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

5.2 Handling Unused Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

Unused output pin should be opened.

5.3 The Attention when the External Clock is Used

Input the clock to XIN pin, and XOUT pin should be opened when you use the external clock.
Please pay attention so that an overshoot and an undershoot do not occur to an input clock of XIN pin.

5.4 Power Supply Pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

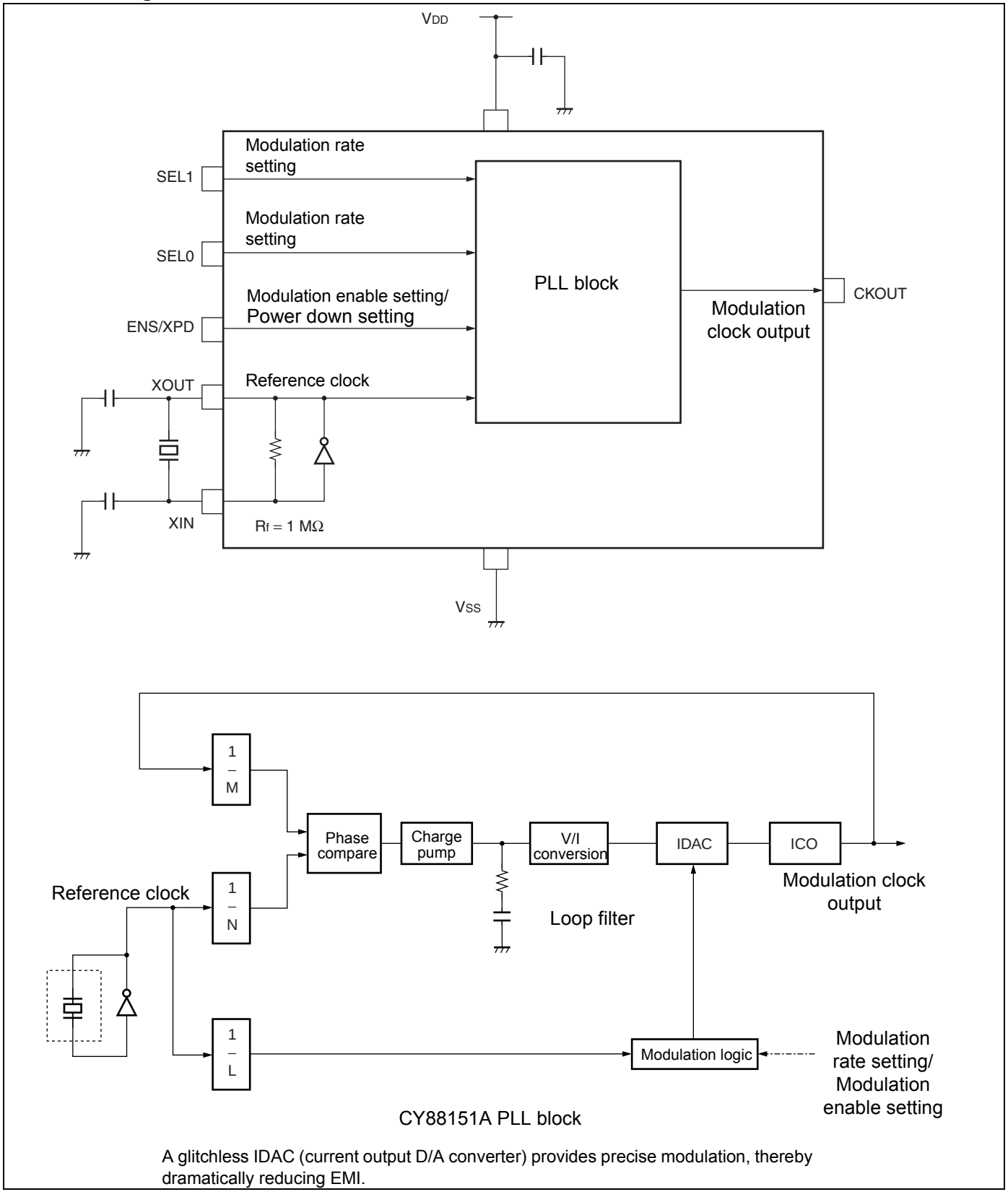
We recommend connecting electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between V_{SS} pin and V_{DD} pin near the device, as a bypass capacitor.

5.5 Oscillation Circuit

Noise near the XIN and XOUT pins may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN or XOUT pin and the resonator do not intersect other wiring.

Design the printed circuit board that surrounds the XIN and XOUT pins with ground.

6. Block Diagram



CY88151A PLL block

A glitchless IDAC (current output D/A converter) provides precise modulation, thereby dramatically reducing EMI.

7. Pin Setting

When changing the pin setting, the stabilization wait time for the modulation clock is required. The stabilization wait time for the modulation clock take the maximum value of “Electrical Characteristics AC Characteristics Lock-up time”.

ENS Modulation Enable Setting (CY88151A-100/200)

ENS	Modulation
L	No modulation
H	Modulation

Note : Spectrum does not spread when “L” is set to ENS. The clock with low jitter can be obtained. Because of ENS has Pull-up resistance, spectrum spread when “H” is set to it or open the terminal.

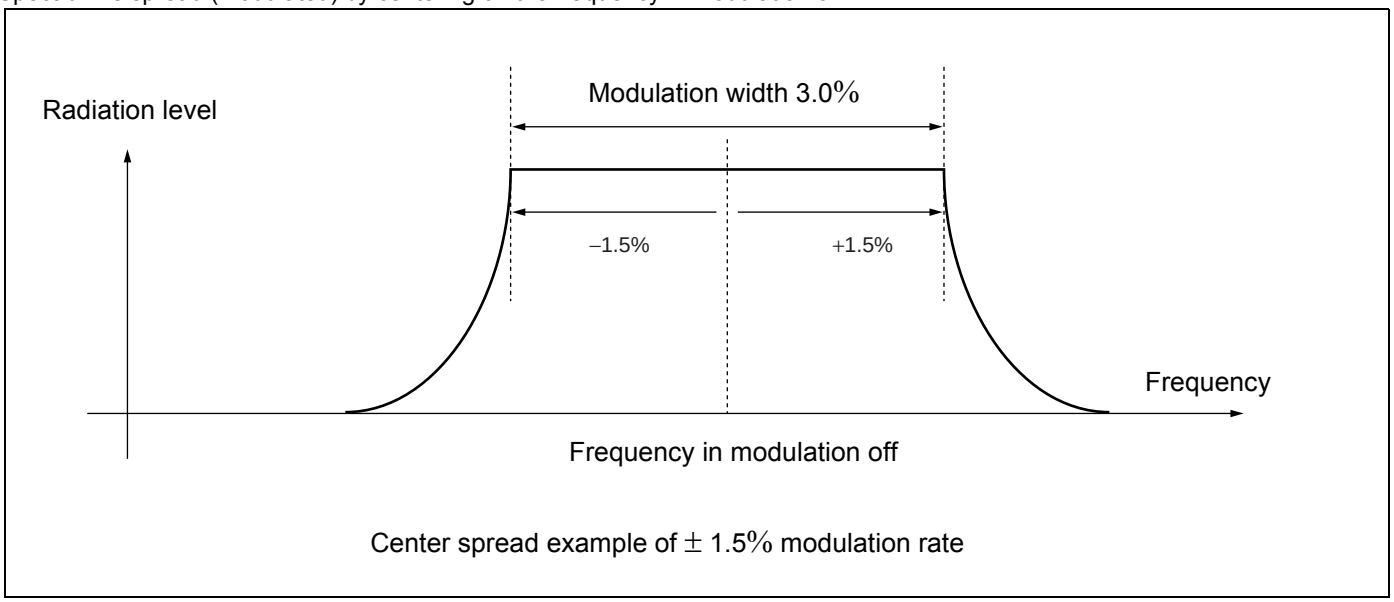
SEL0, SEL1 Modulation Rate Setting

SEL1	SEL0	Modulation Rate	Modulation Type
L	L	± 1.5%	Center spread
L	H	± 0.5%	Center spread
H	L	– 1.0%	Down spread
H	H	– 3.0%	Down spread

Note : The modulation rate can be changed at the level of the terminal.

■ Center Spread

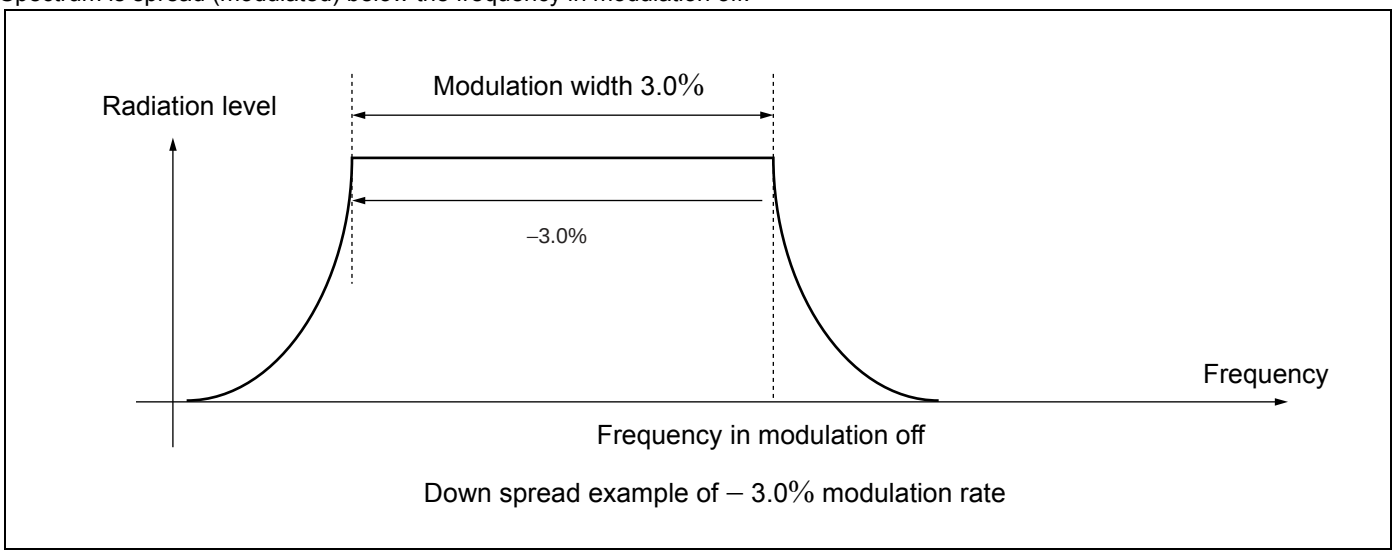
Spectrum is spread (modulated) by centering on the frequency in modulation off.



Center spread example of ± 1.5% modulation rate

■ Down Spread

Spectrum is spread (modulated) below the frequency in modulation off.



Down spread example of – 3.0% modulation rate

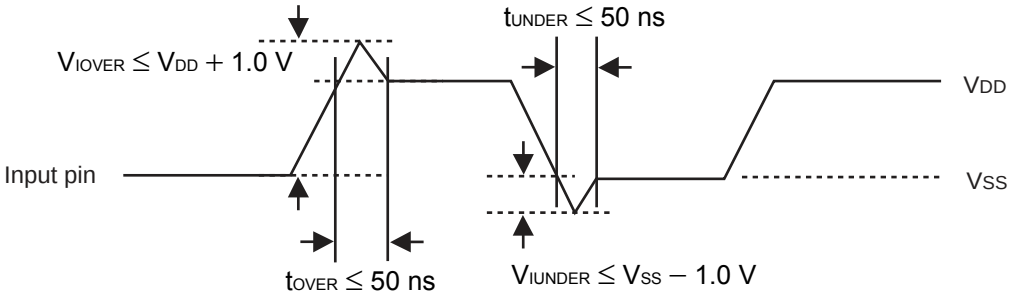
8. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 4.0	V
Input voltage*	V_I	V_{SS} − 0.5	V_{DD} + 0.5	V
Output voltage*	V_O	V_{SS} − 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	− 55	+ 125	°C
Operation junction temperature	T_J	− 40	+ 125	°C
Output current	I_O	− 14	+ 14	mA
Overshoot	V_{IOVER}	—	V_{DD} + 1.0 ($t_{OVER} \leq$ 50 ns)	V
Undershoot	V_{IUNDER}	V_{SS}−1.0 ($t_{UNDER} \leq$ 50 ns)	—	V

* : The parameter is based on V_{SS} = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



9. Recommended Operating Conditions

(V_{SS} = 0.0 V)

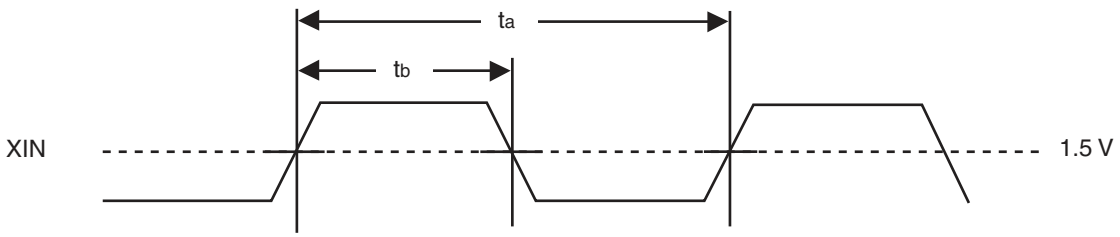
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	V_{DD}	—	3.0	3.3	3.6	V
"H" level input voltage	V_{IH}	XIN, SEL0, SEL1, ENS	—	V_{DD} × 0.8	—	V_{DD} + 0.3	V
"L" level input voltage	V_{IL}		—	V_{SS}	—	V_{DD} × 0.2	V
Input clock duty cycle	t_{DCI}	XIN	16.6 MHz to 33.4 MHz	40	50	60	%
Operating temperature	Ta	—	—	− 40	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b/t_a$)



10. Electrical Characteristics

■ DC Characteristics

(Ta = – 40 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	V_{DD}	No load capacitance at output 24 MHz CY88151A-100	—	5.0	7.0	mA
Output voltage	V_{OH}	CKOUT	"H" level output, I_{OH} = – 4 mA	V_{DD} – 0.5	—	V_{DD}	V
	V_{OL}		"L" level output, I_{OL} = 4 mA	V_{SS}	—	0.4	V
Output impedance	Z_O	CKOUT	16.6 MHz to 66.8 MHz	—	45	—	Ω
Input capacitance	C_{IN}	XIN, SEL0, SEL1, ENS	Ta = + 25 °C, V_{DD} = V_I = 0.0 V, f = 1 MHz	—	—	16	pF
Load capacitance	C_L	CKOUT	16.6 MHz to 66.8 MHz	—	—	15	pF
Input pull-up resistance	R_{PUE}	ENS	V_{IL} = 0.0 V	25	50	200	kΩ
	R_{PUP}	XPD	V_{IL} = 0.0 V	500	800	1200	

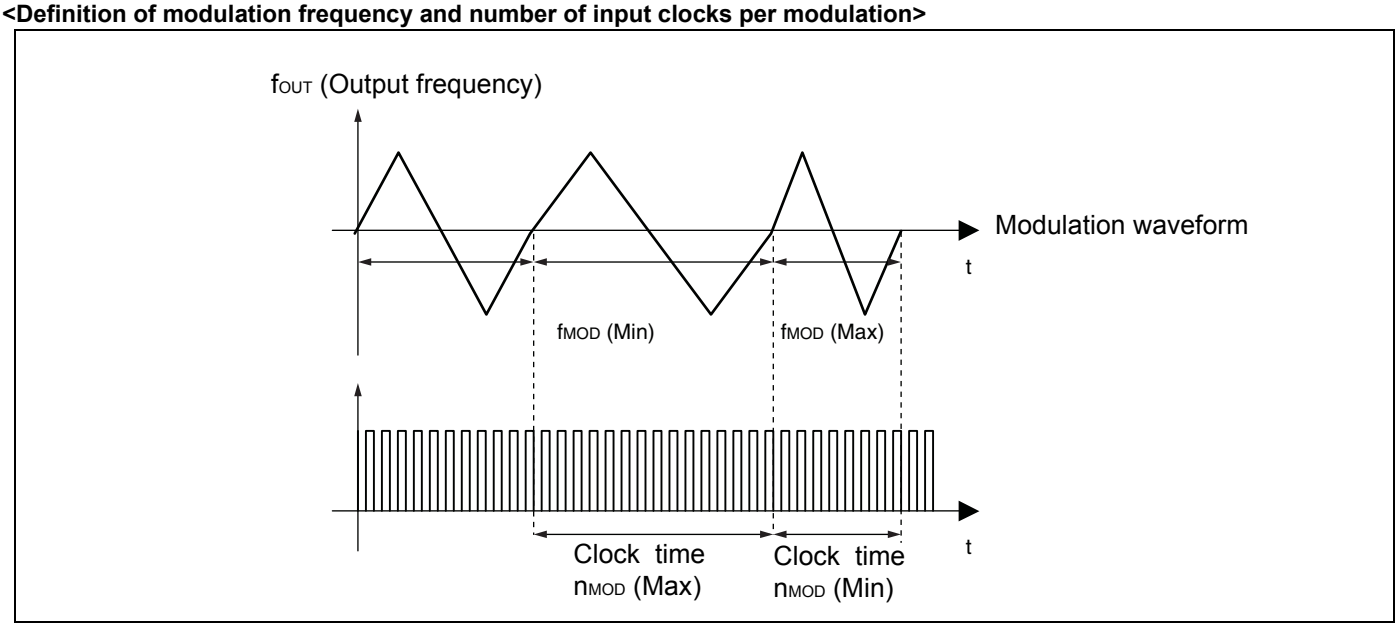
■ AC Characteristics

(Ta = − 40 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Oscillation frequency	f_x	XIN, XOUT	Fundamental oscillation	8.3	—	33.4	MHz
Input frequency	f_{in}	XIN	External clock input (multiply-by-1, 2)	16.6	—	33.4	MHz
Output frequency	f_{OUT}	CKOUT	CY88151A-100 (Multiply by 1)	16.6	—	33.4	MHz
			CY88151A-200 (Multiply by 2)	33.2	—	66.8	
Output slew rate	SR	CKOUT	0.4 V to 2.4 V Load capacitance 15 pF	0.4	—	4.0	V/ns
Output clock duty cycle	t_{DCC}	CKOUT	1.5 V	40	—	60	%
Modulation period (Number of input clocks per modulation)	f_{MOD} (n_{MOD})	CKOUT	CY88151A-100, CY88151A-200	fin/2200 (2200)	fin/1900 (1900)	fin/1600 (1600)	kHz (clks)
Lock-up time	t_{LK}	CKOUT	16.6 MHz to 66.8 MHz	—	2	5	ms
Cycle-cycle jitter	t_{JC}	CKOUT	CY88151A-100 CY88151A-200 No load capacitance, Ta = + 25 °C, V_{DD} = 3.3 V	—	—	100	ps-rms

Note : The modulation clock stabilization wait time is required after the power is turned on, the IC recovers from power saving, or after FREQ (frequency range) or ENS (modulation ON/OFF) setting is changed. For the modulation clock stabilization wait time, assign the maximum value for lock-up time.

<Definition of modulation frequency and number of input clocks per modulation>

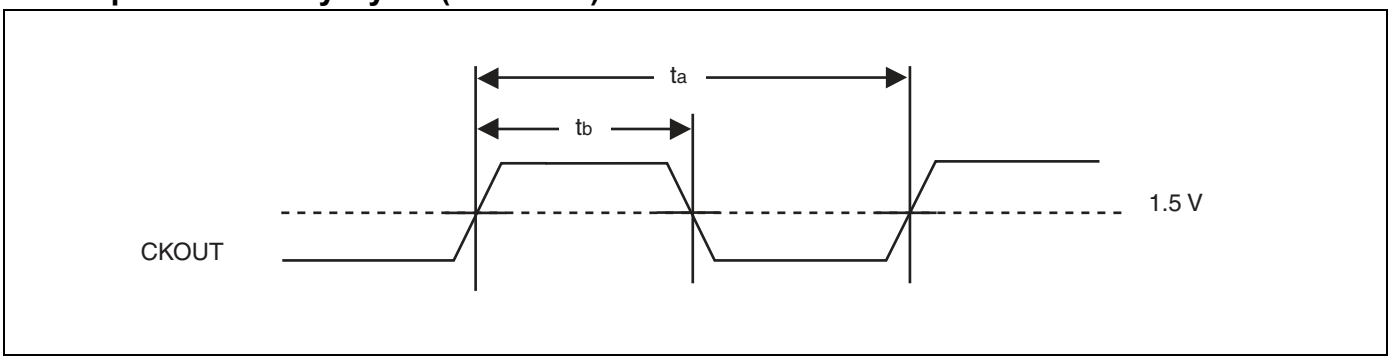


CY88151A contains the modulation period to realize the efficient EMI reduction.

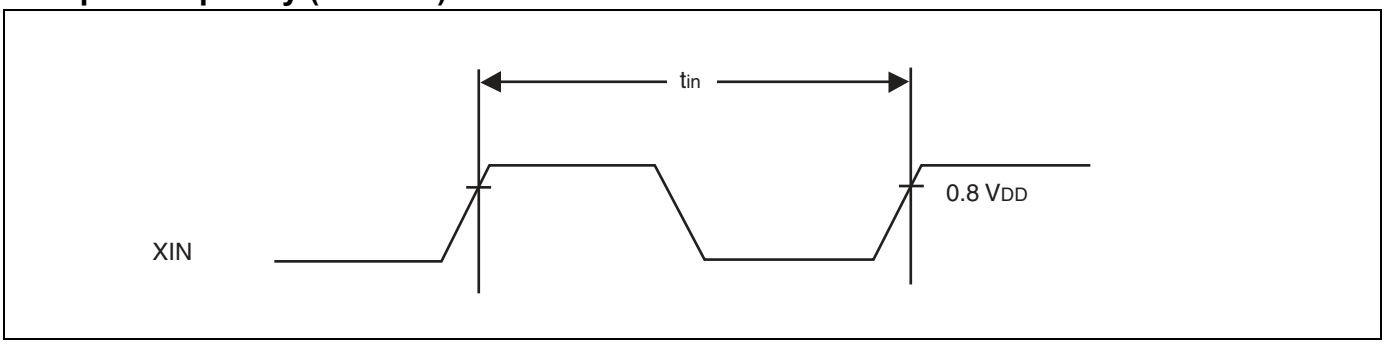
The modulation period f_{MOD} depends on the input frequency and changes between f_{MOD} (Min) and f_{MOD} (Max) .

Furthermore, the average value of f_{MOD} equals the typical value of the electrical characteristics.

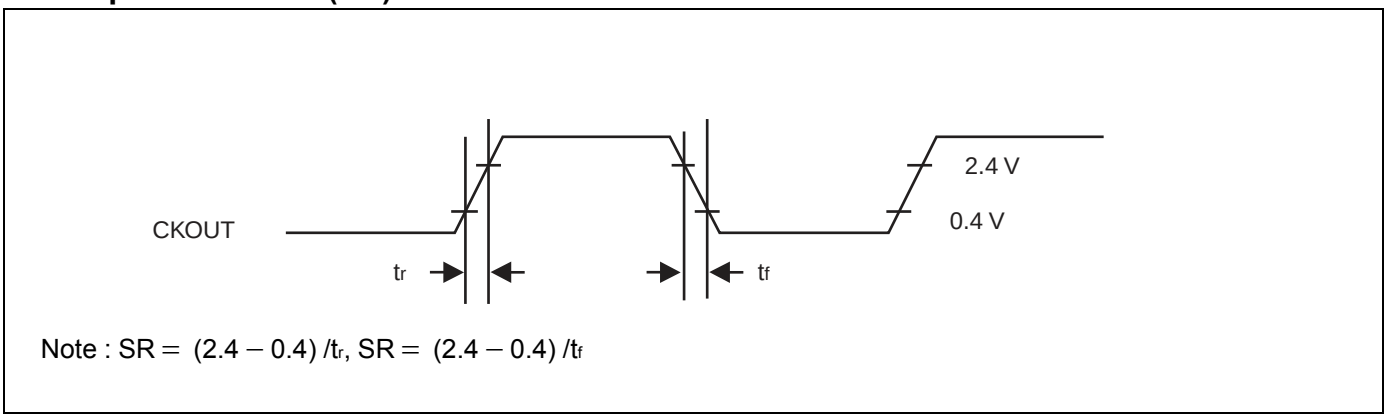
11. Output Clock Duty Cycle ($t_{DCC} = t_b/t_a$)



12. Input Frequency ($f_{in} = 1/t_{in}$)

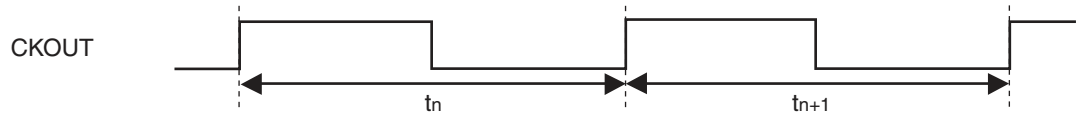


13. Output Slew Rate (SR)



Note : SR = (2.4 − 0.4) /t_r, SR = (2.4 − 0.4) /t_f

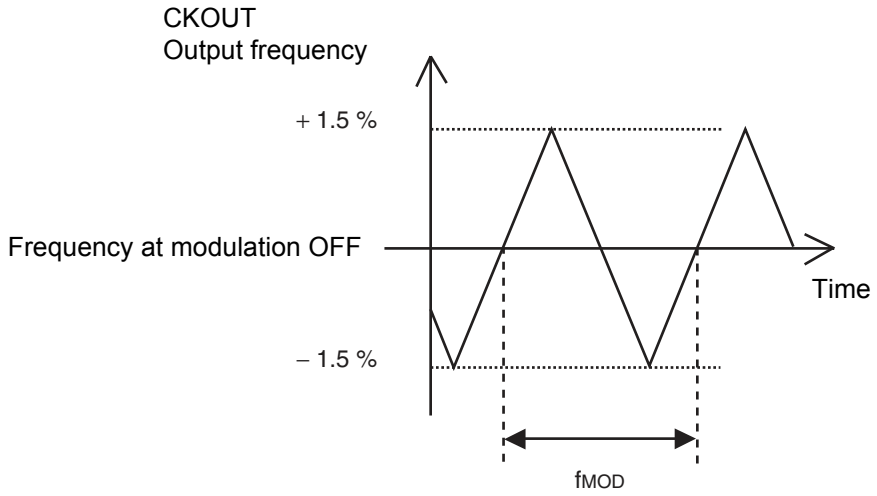
14. Cycle-cycle Jitter ($t_{JC} = | t_n - t_{n+1} |$)



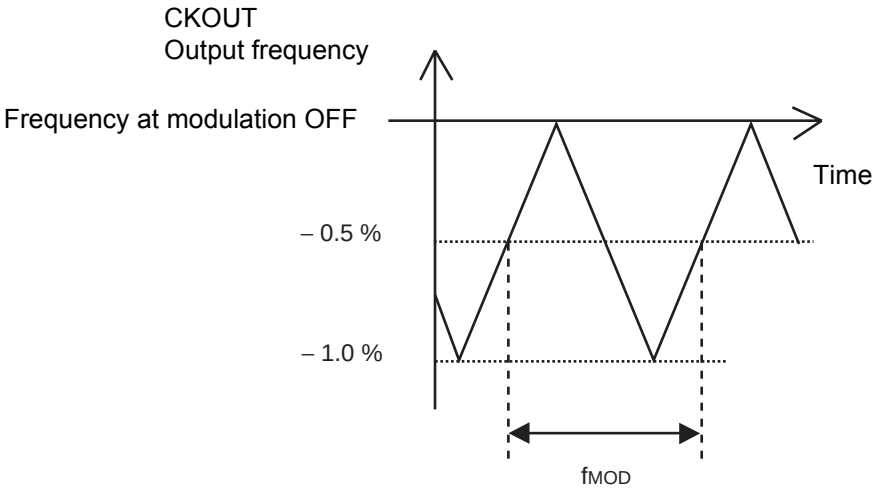
Note : Cycle-cycle jitter is defined the difference between a certain cycle and immediately after (or, immediately before) .

15. Modulation Waveform

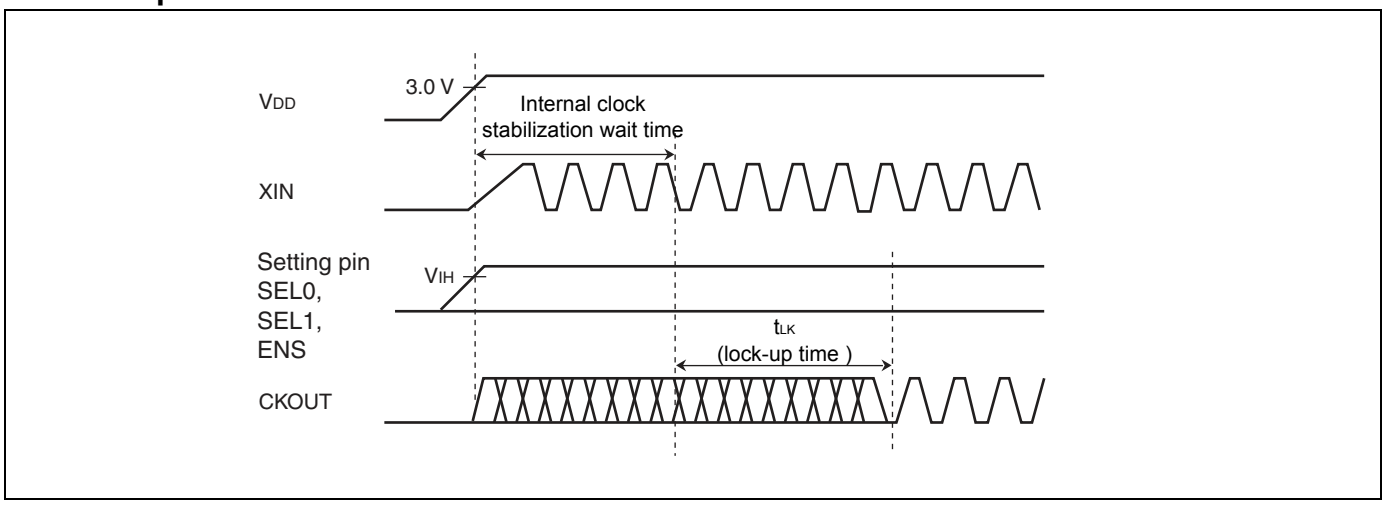
■ ±1.5% modulation rate, Example of center spread



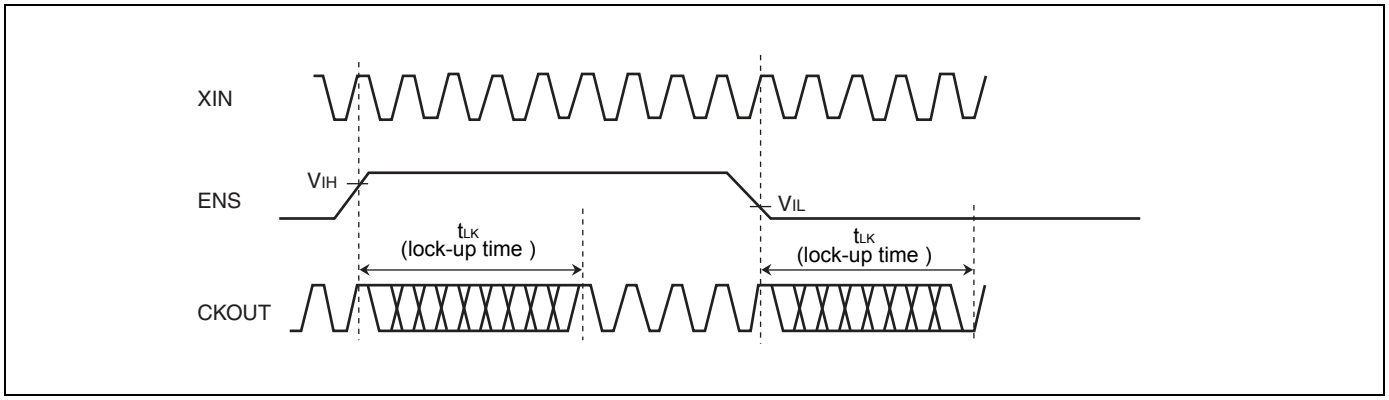
■ −1.0% modulation rate, Example of down spread



16. Lock-up Time

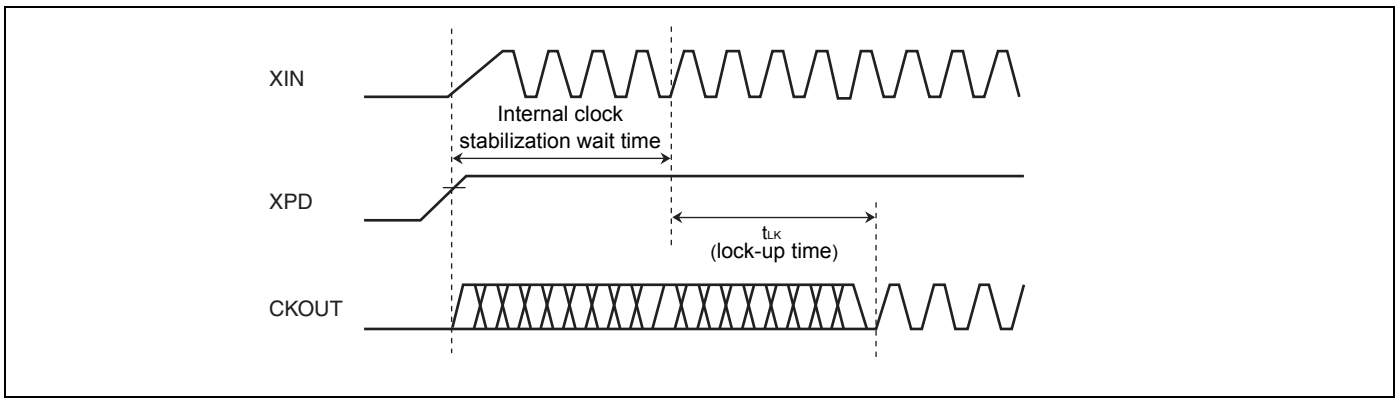


If the setting pin is fixed at the “H” or “L” level, the maximum time after the power is turned on until the set clock signal is output from CKOUT pin is (the stabilization wait time of input clock to XIN pin) ＋ (the lock-up time “t_{LK}”). For the input clock stabilization time, check the characteristics of the resonator or oscillator used.



For modulation enable control using the ENS pin during normal operation, the set clock signal is output from CKOUT pin at most the lock-up time (t_{LK}) after the level at the ENS pin is determined.

Note : When the pin setting is changed, the CKOUT pin output clock stabilization time is required. Until the output clock signal becomes stable, the output frequency, output clock duty cycle, modulation period, and cycle-cycle jitter cannot be guaranteed. It is therefore advisable to perform processing such as cancelling a reset of the device at the succeeding stage after the lock-up time.



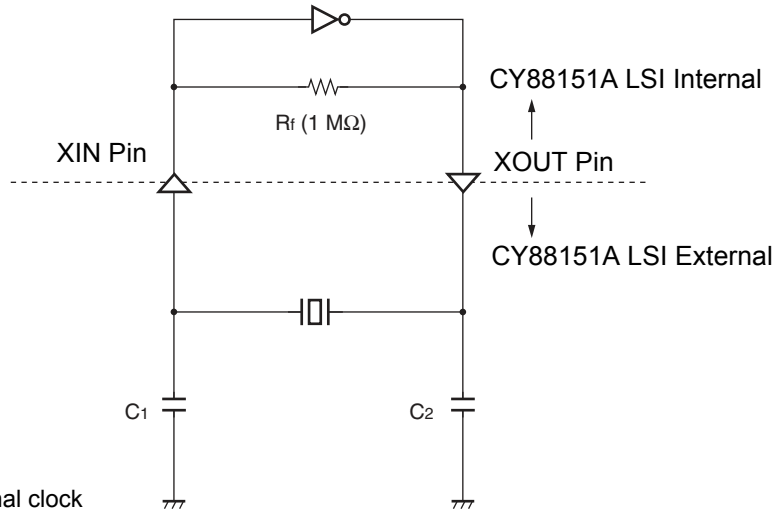
When the power down is controlled by XPD pin, the desired clock is obtained after the pin is set to H level until the maximum lock-up time t_{LK} is elapsed.

17. Oscillation Circuit

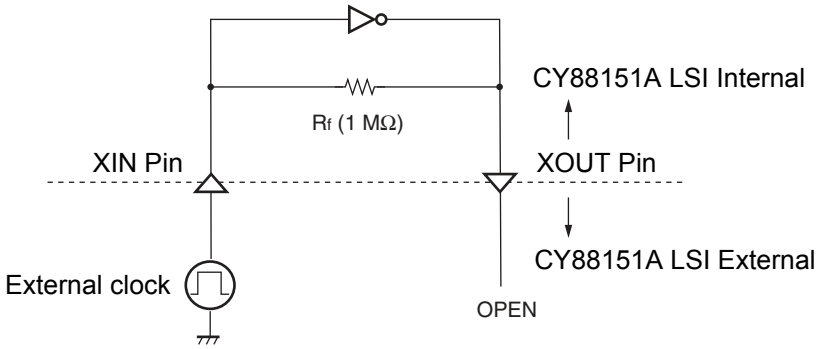
The figure below shows the connection example about general resonator. The oscillation circuit has the built-in resistance (Rf). The value of capacity (C_1 and C_2) is required adjusting to the most suitable value of individual resonator.
The most suitable value is different by individual resonator. Please refer to the resonator manufacturer which you use for the most suitable value.

Input the clock to XIN pin, and do not connect anything with XOUT pin if you use the external clock (you do not use the resonator).

■ When using the resonator

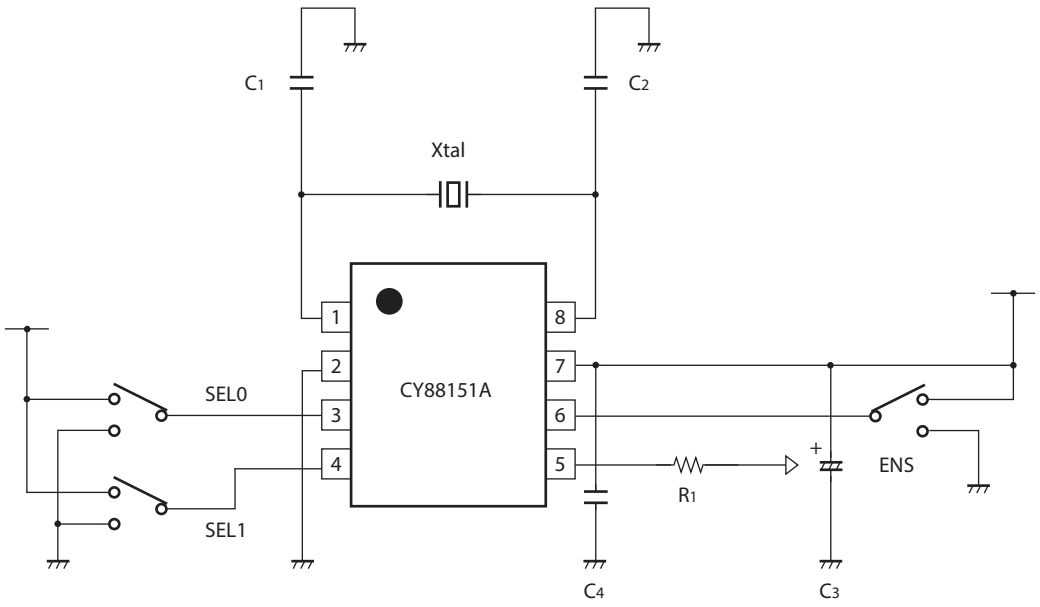


■ When using an external clock



Note : Note that a jitter characteristic of an input clock may cause an affect a cycle-cycle jitter characteristic.

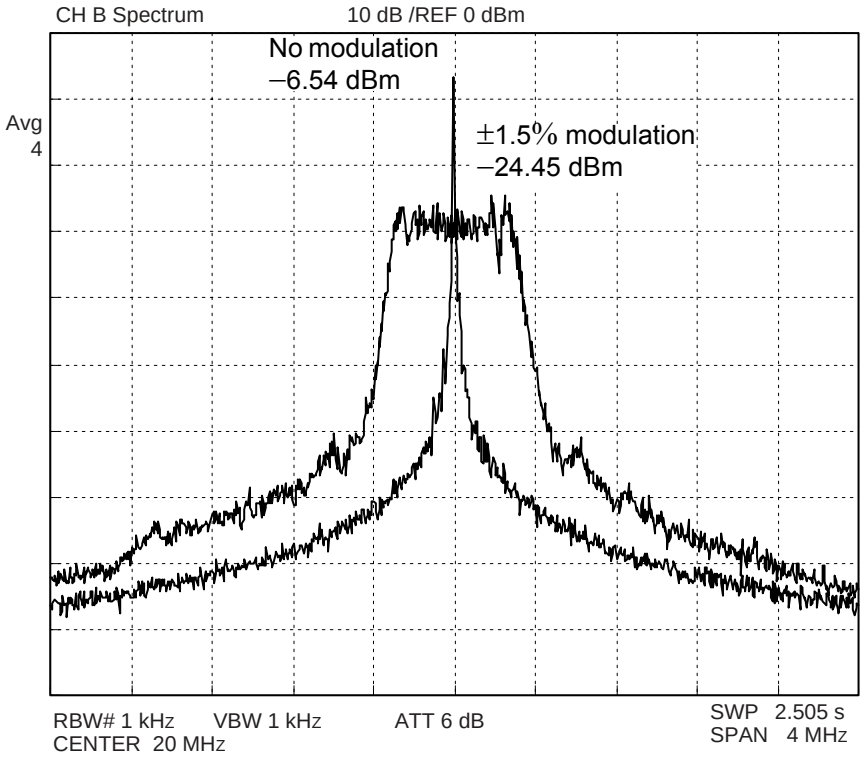
18. Interconnection Circuit Example



C_1, C_2	: Oscillation stabilization capacitance (refer to “Oscillation Circuit”.)
C_3	: Capacitor of 10 μF or higher
C_4	: Capacitor about 0.01 μF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device.)
R_1	: Impedance matching resistor for board pattern

19. Spectrum Example Characteristics

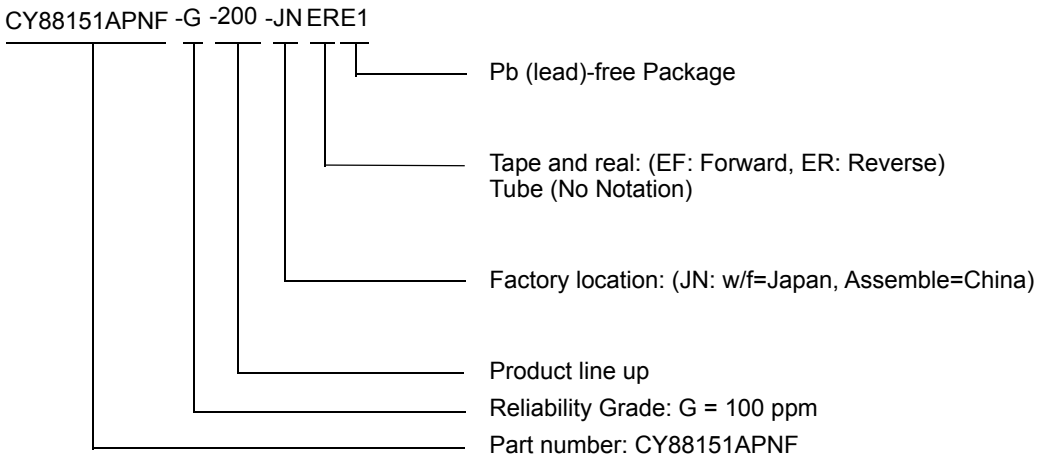
The condition of the examples of the characteristic is shown as follows : Input frequency = 20 MHz (Output frequency = 20 MHz : Using CY88151A-100 (Multiply-by-1)), Power - supply voltage = 3.3 V, None load capacity,
Modulation rate = ± 1.5% (center spread).
Spectrum analyzer HP4396B is connected with CKOUT. The result of the measurement with RBW = 1 kHz
(ATT use for − 6dB).



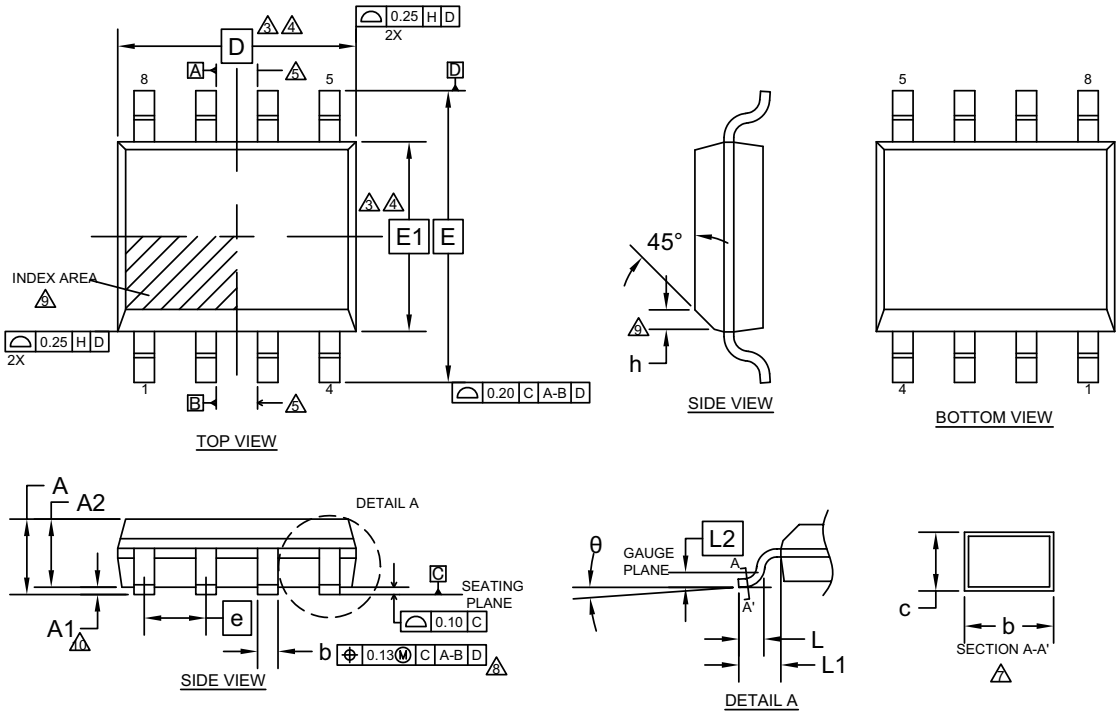
20. Ordering Information

Part Number	Input Frequency Range	Multiplier Ratio	Output Frequency Range	Package	Remarks
CY88151APNF-G-100-JNE1	16.6 MHz to 33.4 MHz	Multiply-by-1	16.6 MHz to 33.4 MHz	8-pin plastic SOP (SOB008)	
CY88151APNF-G-200-JNE1		Multiply-by-2	33.2 MHz to 66.8 MHz		
CY88151APNF-G-100-JNEFE1	16.6 MHz to 33.4 MHz	Multiply-by-1	16.6 MHz to 33.4 MHz		Emboss taping (EF type)
CY88151APNF-G-200-JNEFE1		Multiply-by-2	33.2 MHz to 66.8 MHz		
CY88151APNF-G-100-JNERE1	16.6 MHz to 33.4 MHz	Multiply-by-1	16.6 MHz to 33.4 MHz		Emboss taping (ER type)
CY88151APNF-G-200-JNERE1		Multiply-by-2	33.2 MHz to 66.8 MHz		

Ordering Code Definitions



21. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.75
A1	0.05	——	0.25
A2	1.30	1.40	1.50
D	5.05 BSC.		
E	6.00 BSC.		
E1	3.90 BSC		
θ	0°	——	8°
c	0.15	——	0.25
b	0.36	0.44	0.52
L	0.45	0.60	0.75
L 1	1.05 REF		
L 2	0.25 BSC		
e	1.27 BSC.		
h	0.40 BSC.		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	TAOA	06/29/2009	Initial Release
*A	5569547	TAOA	12/30/2016	Updated to Cypress Template
*B	5993569	TAOA	12/18/2017	Deleated EOL part number: MB88151A-101/201/400/401/500/501/800/801 Updated Package Dimensions: Updated to Cypress format. Changed the package name from FPT-8P-M02 to SOB008.
*C	6277189	ATTS	08/13/2018	Updated part number: MB88151A to CY88151A Added Ordering Code Definitions

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