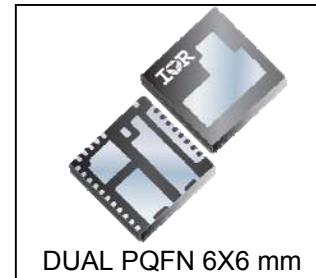
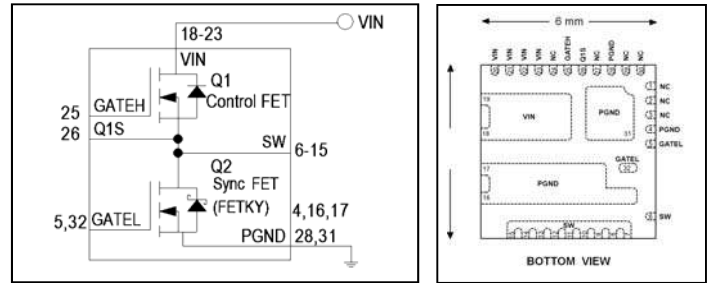


	Q1	Q2	
V_{DSS}	25	25	V
$R_{DS(on) \max}$ (@ $V_{GS} = 4.5V$)	4.10	1.35	m Ω
Q_g (typical)	13	35	nC
I_D (@ $T_C = 25^\circ C$)	60 $\text{\textcircled{7}}$	60 $\text{\textcircled{7}}$	A



Applications

- Control and Synchronous MOSFETs for synchronous buck converters

Features

Control and synchronous MOSFETs in one package
Low thermal resistance path to the PCB
Low thermal resistance path to the top
Low charge control MOSFET (13nC typical)
Low $R_{DS(on)}$ synchronous MOSFET (<1.35m Ω)
Intrinsic schottky diode with low forward voltage on Q2
RoHS compliant, halogen-free
MSL2, industrial qualification

Benefits

Increased power density
Increased power density
Increased power density
Lower switching losses
Lower conduction losses
Lower switching losses
Environmentally friendlier
Increased reliability

results in
=>

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFHE4250DPbF	Dual PQFN 6mm x 6mm	Tape and Reel	4000	IRFHE4250DTRPbF

Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
V_{GS}	Gate-to-Source Voltage	± 16		V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	86 $\text{\textcircled{7}}$	303 $\text{\textcircled{7}}$	A
$I_D @ T_C = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	69 $\text{\textcircled{7}}$	243 $\text{\textcircled{7}}$	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current (Source Bonding Technology Limited)	60 $\text{\textcircled{7}}$	60 $\text{\textcircled{7}}$	A
I_{DM}	Pulsed Drain Current	180	525 $\text{\textcircled{8}}$	
$P_D @ T_C = 25^\circ C$	Power Dissipation	156	156	W
$P_D @ T_C = 70^\circ C$	Power Dissipation	100	100	
	Linear Derating Factor	1.3	1.3	W/ $^\circ C$
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		$^\circ C$

Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case $\text{\textcircled{4}}$	3.7	0.91	$^\circ C/W$
$R_{\theta JC}$ (Top)	Junction-to-Case $\text{\textcircled{4}}$	0.91	2.1	
$R_{\theta JA}$	Junction-to-Ambient $\text{\textcircled{5}}$	24	24	
$R_{\theta JA} (<10s)$	Junction-to-Ambient $\text{\textcircled{5}}$	17	17	

Notes $\text{\textcircled{1}}$ through $\text{\textcircled{8}}$ are on page 12

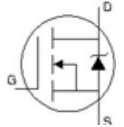
Static @ T_J = 25°C (unless otherwise specified)

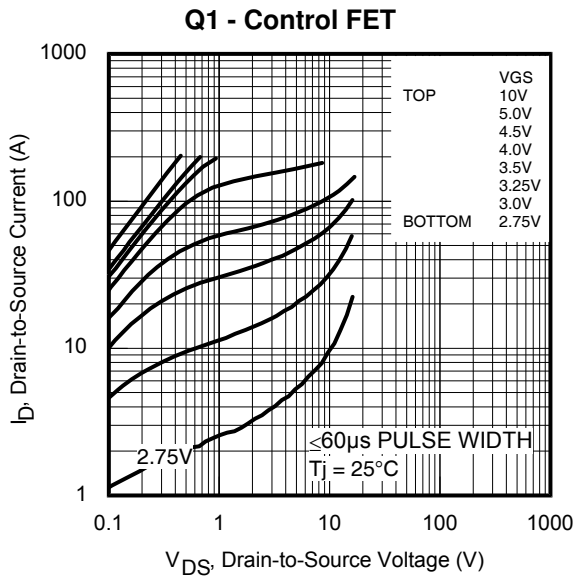
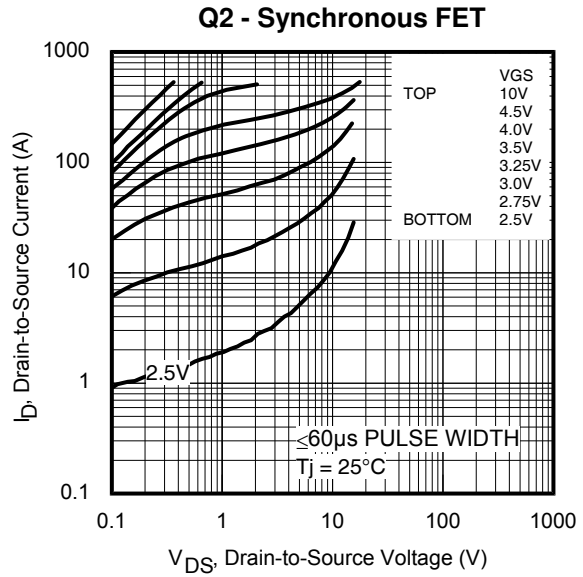
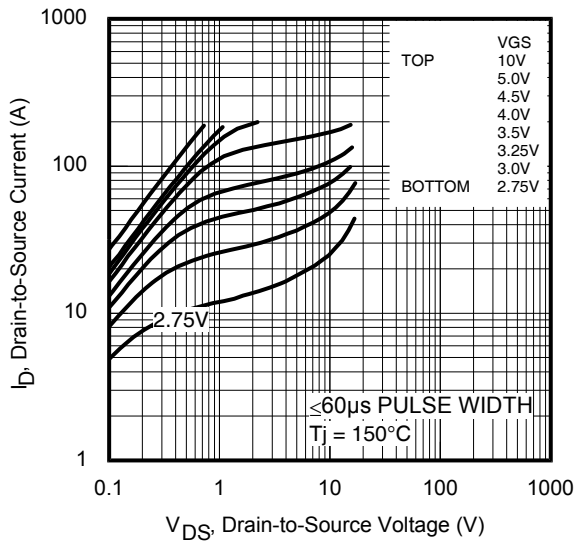
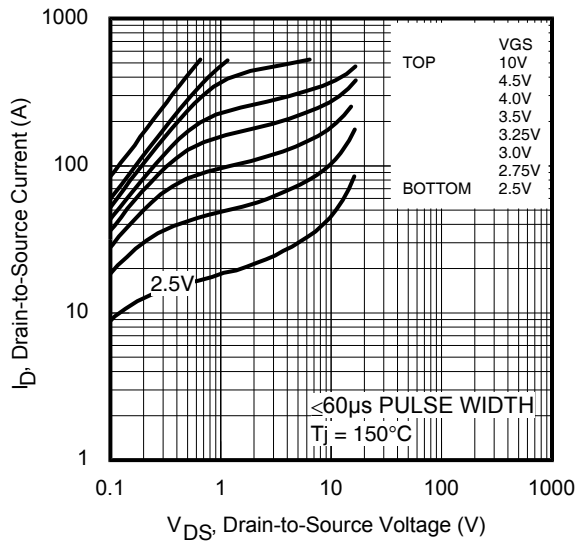
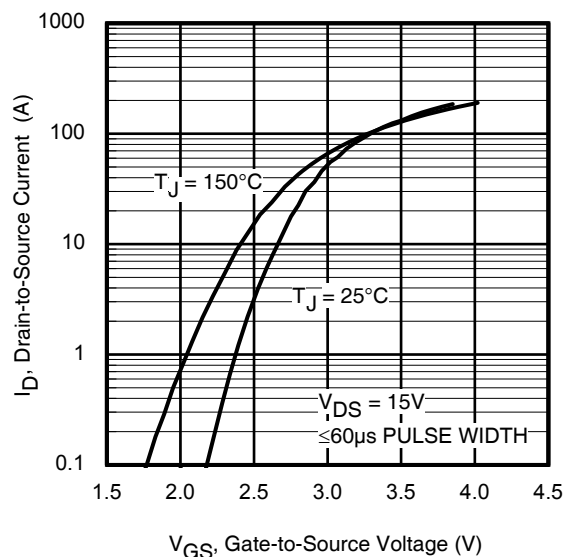
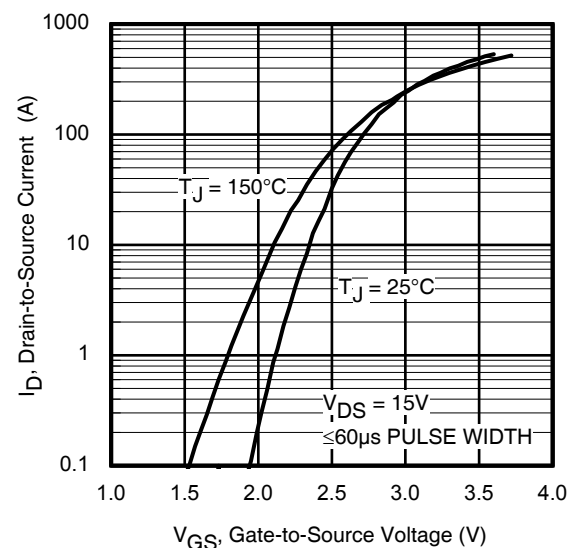
	Parameter		Min.	Typ.	Max.	Units	Conditions		
BV _{DSS}	Drain-to-Source Breakdown Voltage	Q1	25	—	—	V	V _{GS} = 0V, I _D = 250μA		
		Q2	25	—	—		V _{GS} = 0V, I _D = 1.0mA		
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	Q1	—	23	—	mV/°C	Reference to 25°C, I _D = 1.0mA		
		Q2	—	21	—		Reference to 25°C, I _D = 10mA		
R _{DS(on)}	Static Drain-to-Source On-Resistance	Q1	—	2.20	2.75	mΩ	V _{GS} = 10V, I _D = 27A ③		
		Q2	—	0.70	0.90		V _{GS} = 10V, I _D = 27A ③		
		Q1	—	3.20	4.10		V _{GS} = 4.5V, I _D = 27A ③		
		Q2	—	1.00	1.35		V _{GS} = 4.5V, I _D = 27A ③		
V _{GS(th)}	Gate Threshold Voltage	Q1	1.1	1.6	2.1	V	Q1: V _{DS} = V _{GS} , I _D = 35μA		
		Q2	1.1	1.6	2.1		Q2: V _{DS} = V _{GS} , I _D = 100μA		
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	Q1	—	-5.8	—	mV/°C	Q1: V _{DS} = V _{GS} , I _D = 35μA		
		Q2	—	-7.8	—		Q2: V _{DS} = V _{GS} , I _D = 1.0mA		
I _{DSS}	Drain-to-Source Leakage Current	Q1	—	—	1.0	μA	V _{DS} = 20V, V _{GS} = 0V		
		Q2	—	—	500		V _{DS} = 20V, V _{GS} = 0V		
I _{GSS}	Gate-to-Source Forward Leakage	Q1/Q2	—	—	100	nA	V _{GS} = 16V		
	Gate-to-Source Reverse Leakage	Q1/Q2	—	—	-100		V _{GS} = -16V		
g _{fs}	Forward Transconductance	Q1	73	—	—	S	V _{DS} = 10V, I _D = 14A		
		Q2	121	—	—		V _{DS} = 10V, I _D = 23A		
Q _g	Total Gate Charge	Q1	—	13	20	nC	Q1 V _{DS} = 13V V _{GS} = 4.5V, I _D = 13A Q2 V _{DS} = 13V V _{GS} = 4.5V, I _D = 23A		
		Q2	—	35	53				
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	Q1	—	3.6	—				
		Q2	—	8.6	—				
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	Q1	—	1.3	—				
		Q2	—	3.8	—				
Q _{gd}	Gate-to-Drain Charge	Q1	—	5.2	—				
		Q2	—	13	—				
Q _{godr}	Gate Charge Overdrive	Q1	—	2.9	—				
		Q2	—	9.6	—				
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	Q1	—	6.5	—				
		Q2	—	16.8	—				
Q _{oss}	Output Charge	Q1	—	14	—	nC	V _{DS} = 16V, V _{GS} = 0V		
		Q2	—	41	—				
R _G	Gate Resistance	Q1	—	0.5	—	Ω			
		Q2	—	0.4	—				
t _{d(on)}	Turn-On Delay Time	Q1	—	11	—	ns	Q1 V _{DS} = 13V V _{GS} = 4.5V I _D = 14A, R _G = 1.8Ω Q2 V _{DS} = 13V V _{GS} = 4.5V I _D = 23A, R _G = 1.8Ω		
		Q2	—	17	—				
t _r	Rise Time	Q1	—	33	—				
		Q2	—	54	—				
t _{d(off)}	Turn-Off Delay Time	Q1	—	14	—				
		Q2	—	24	—				
t _f	Fall Time	Q1	—	12	—				
		Q2	—	16	—				
C _{iss}	Input Capacitance	Q1	—	1735	—			pF	V _{GS} = 0V V _{DS} = 13V f = 1.0MHz
		Q2	—	4765	—				
C _{oss}	Output Capacitance	Q1	—	493	—				
		Q2	—	1577	—				
C _{rss}	Reverse Transfer Capacitance	Q1	—	137	—				
		Q2	—	370	—				

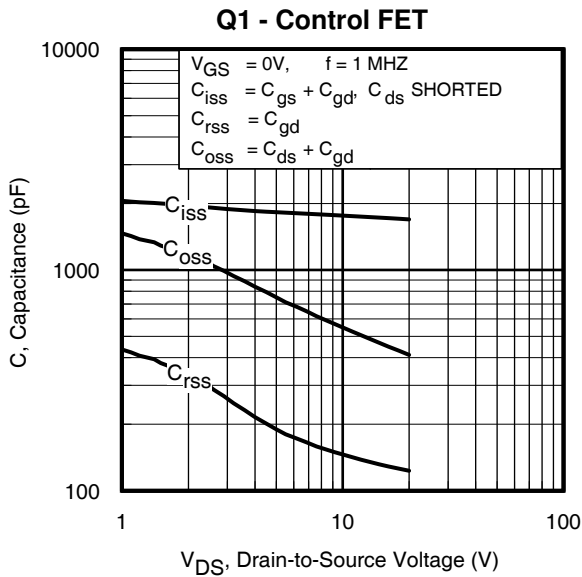
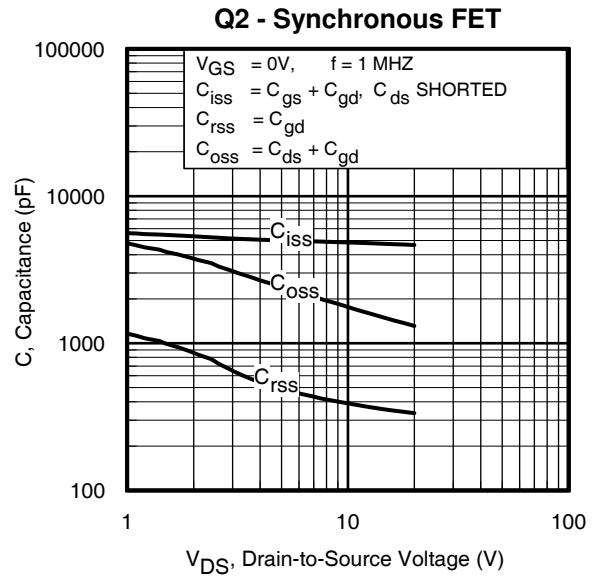
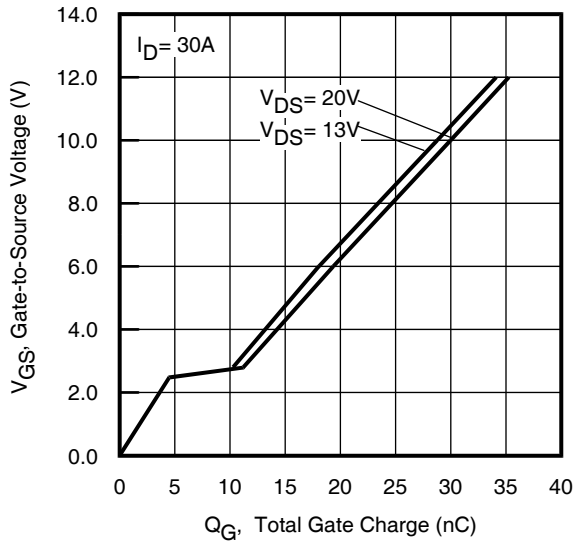
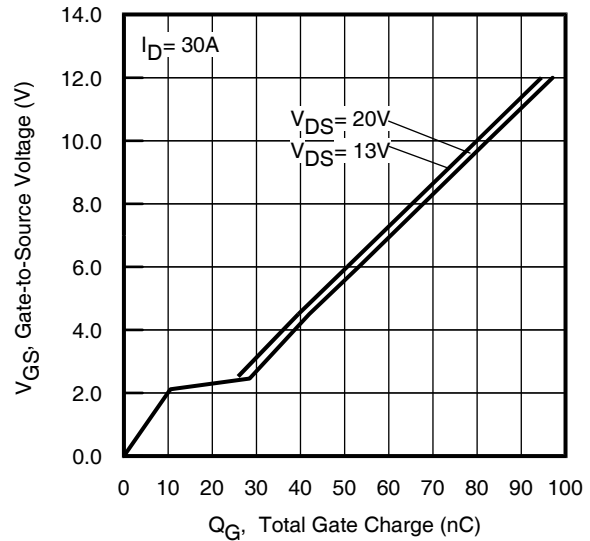
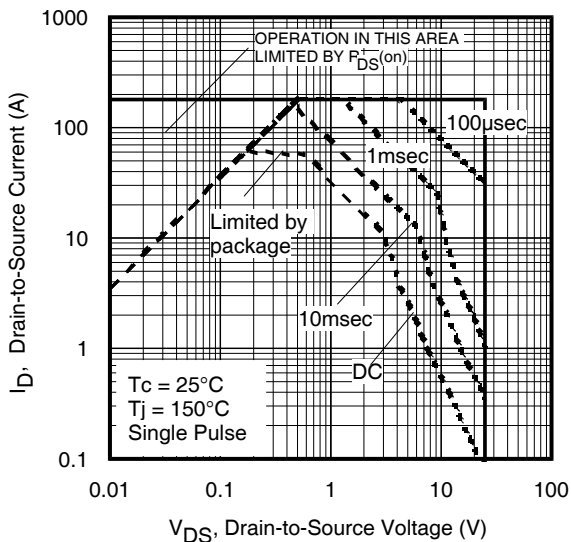
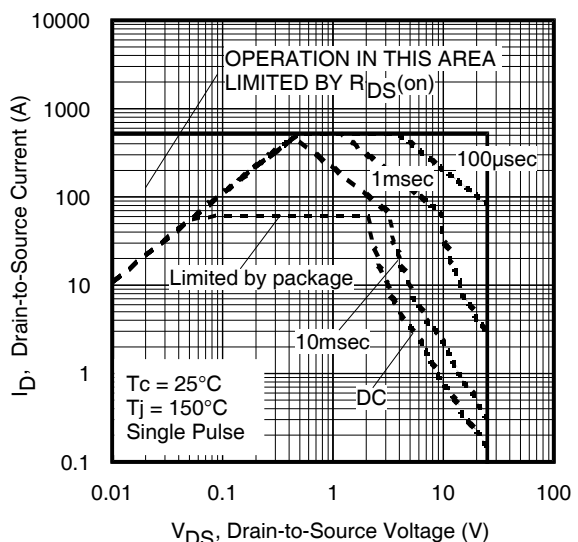
Avalanche Characteristics

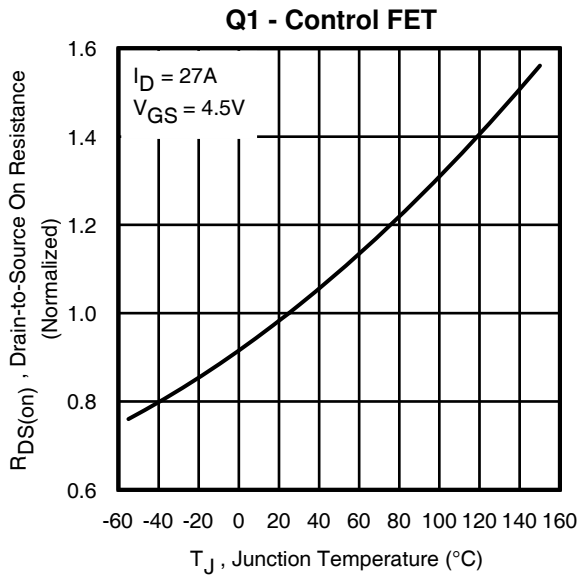
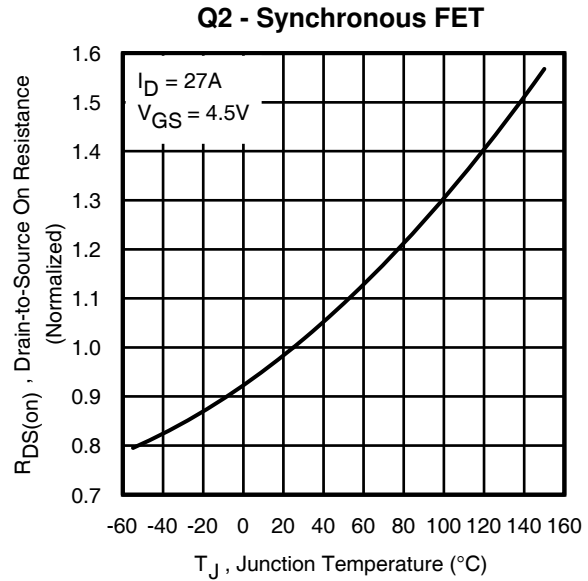
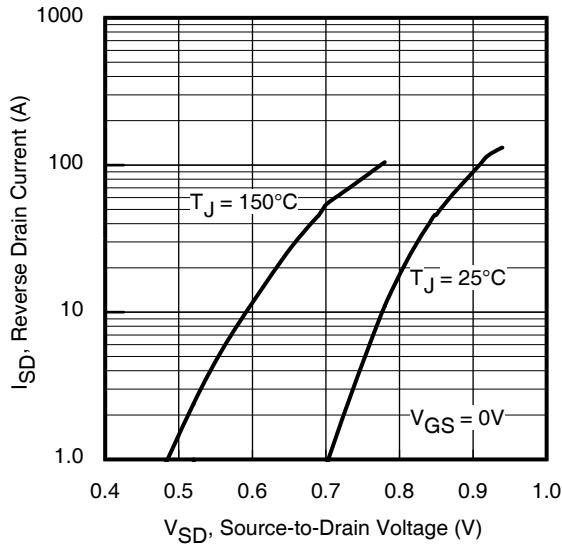
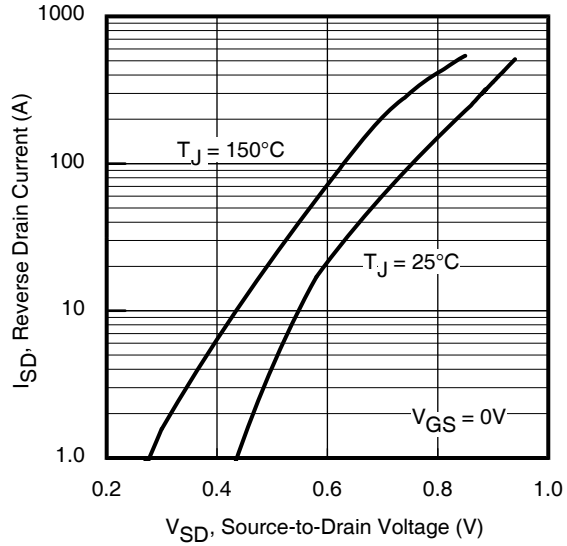
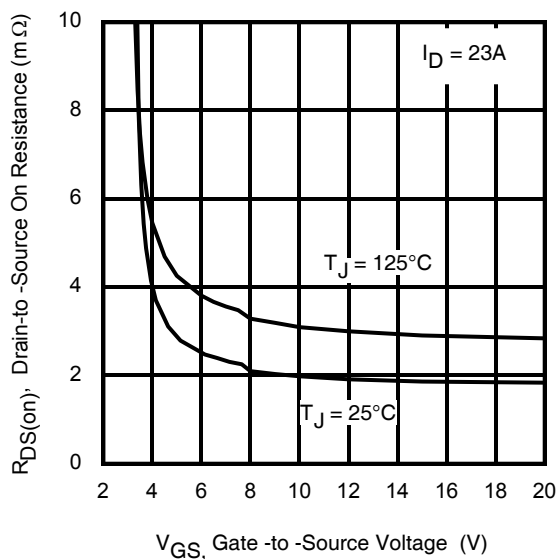
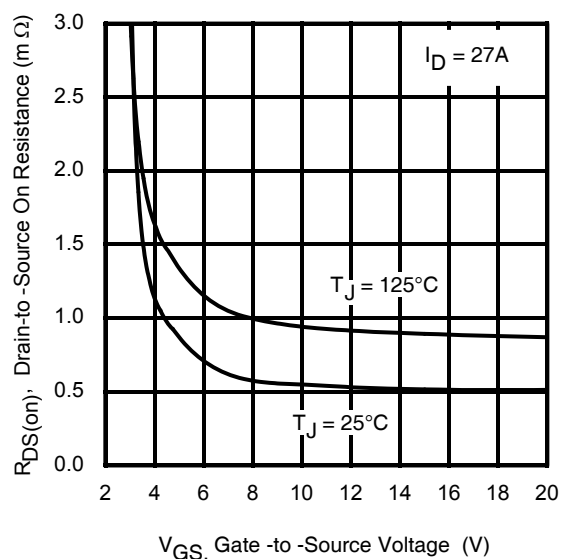
	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	71②	481②	mJ
I_{AR}	Avalanche Current ①	—	32	63	A

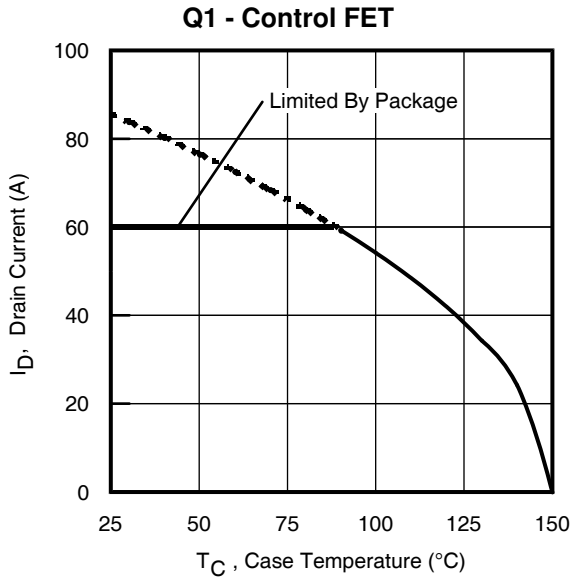
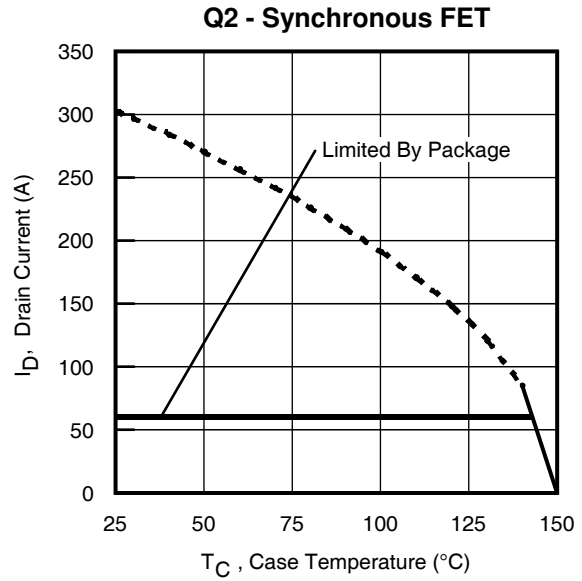
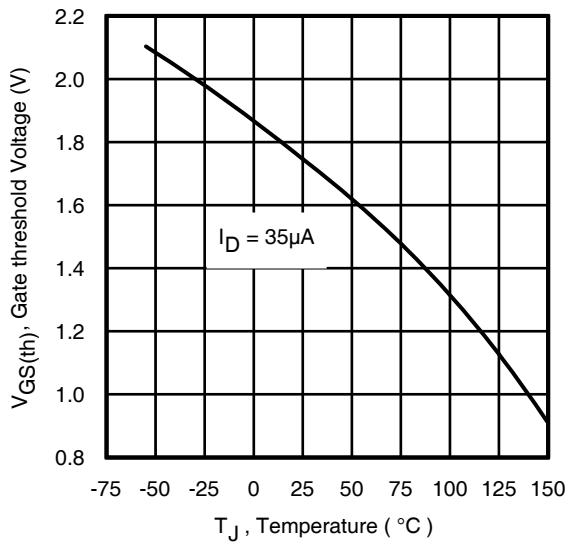
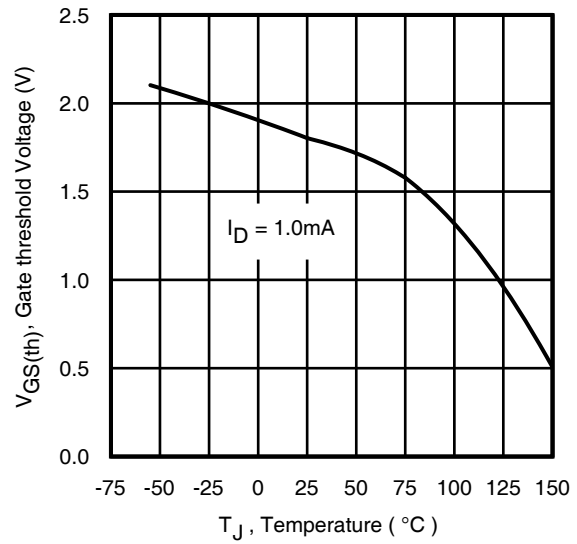
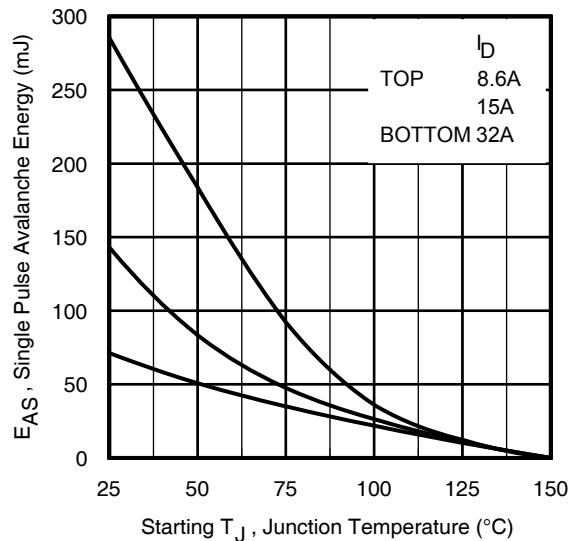
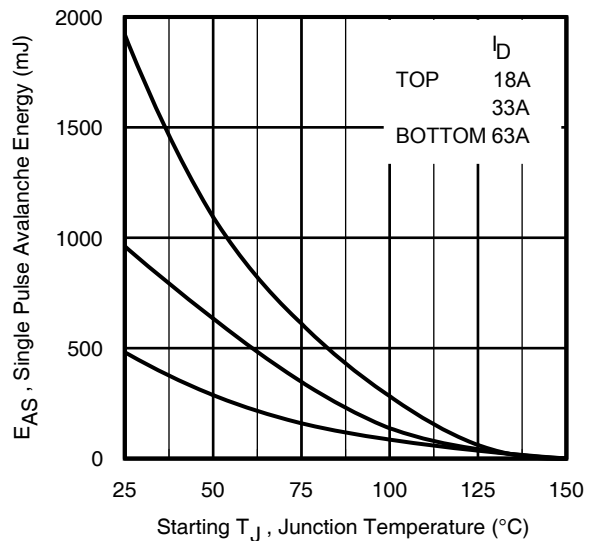
Diode Characteristics

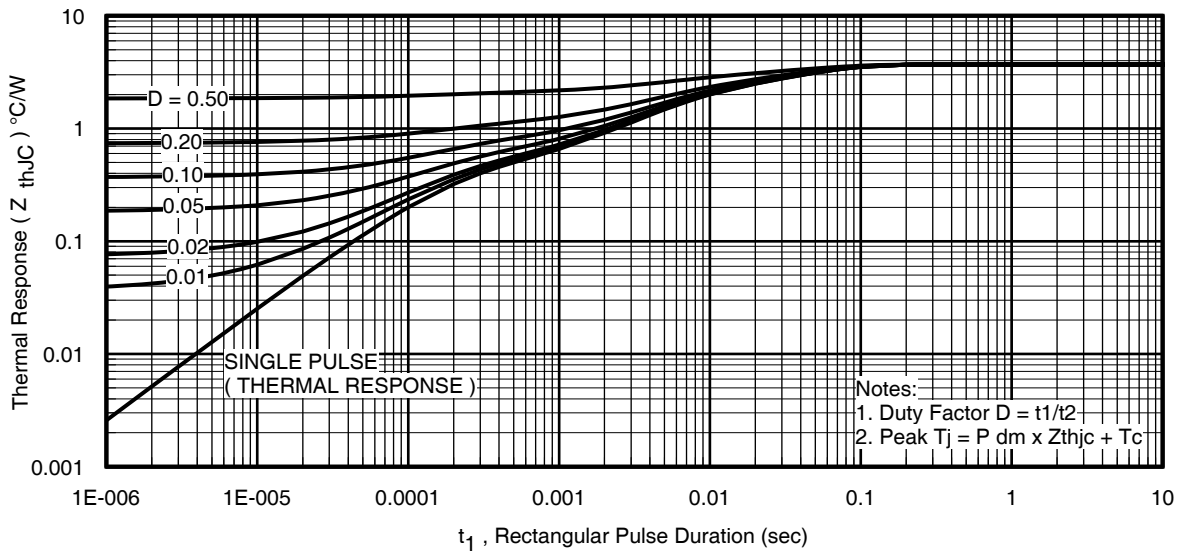
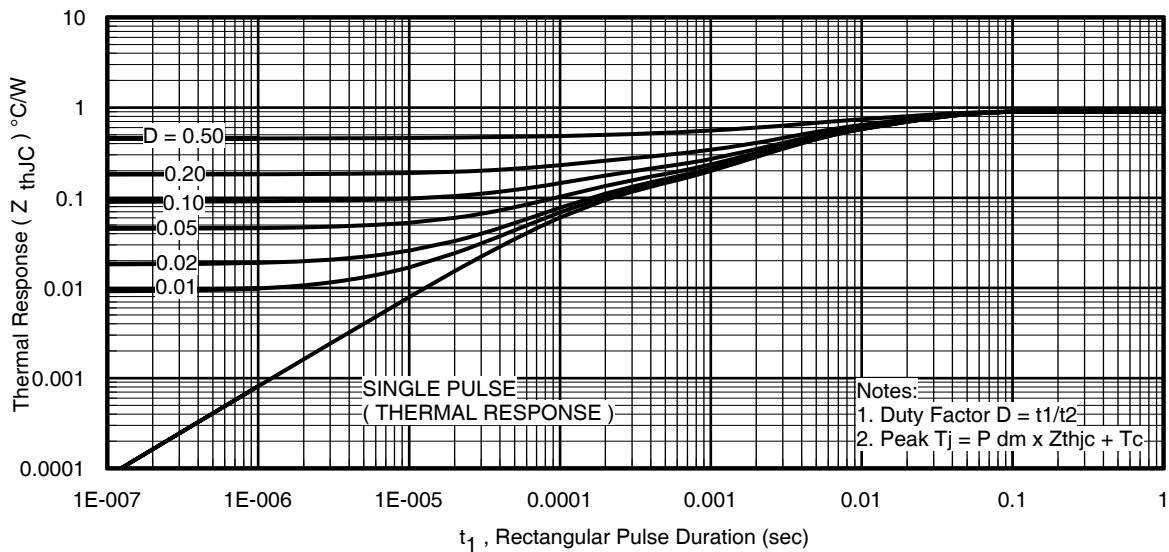
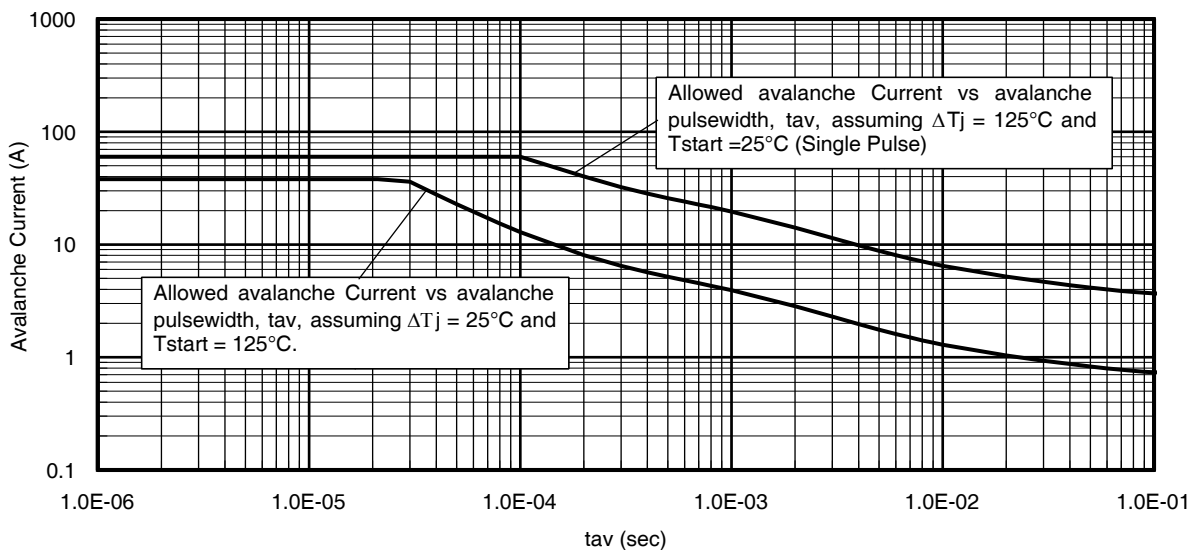
	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	Q1	—	—	60⑦	A	MOSFET symbol showing the integral reverse p-n junction diode. 
		Q2	—	—	60⑦		
I_{SM}	Pulsed Source Current (Body Diode)	Q1	—	—	180	A	
		Q2	—	—	525⑧		
V_{SD}	Diode Forward Voltage	Q1	—	0.77	0.88	V	$T_J = 25^\circ\text{C}$, $I_S = 14\text{A}$, $V_{GS} = 0\text{V}$ ③
		Q2	—	0.60	0.75		$T_J = 25^\circ\text{C}$, $I_S = 27\text{A}$, $V_{GS} = 0\text{V}$ ③
t_{rr}	Reverse Recovery Time	Q1	—	19	29	ns	$Q1$ $T_J = 25^\circ\text{C}$, $I_F = 30\text{A}$ $V_{DD} = 13\text{V}$, $di/dt = 200\text{A}/\mu\text{s}$ ③
		Q2	—	34	51		
Q_{rr}	Reverse Recovery Charge	Q1	—	16	24	nC	$Q2$ $T_J = 25^\circ\text{C}$, $I_F = 30\text{A}$ $V_{DD} = 13\text{V}$, $di/dt = 200\text{A}/\mu\text{s}$ ③
		Q2	—	54	81		


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Output Characteristics

Fig 4. Typical Output Characteristics

Fig 5. Typical Transfer Characteristics

Fig 6. Typical Transfer Characteristics


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

Fig 11. Maximum Safe Operating Area

Fig 12. Maximum Safe Operating Area


Fig 13. Normalized On-Resistance vs. Temperature

Fig 14. Normalized On-Resistance vs. Temperature

Fig 15. Typical Source-Drain Diode Forward Voltage

Fig 16. Typical Source-Drain Diode Forward Voltage

Fig 17. Typical On-Resistance vs. Gate Voltage

Fig 18. Typical On-Resistance vs. Gate Voltage


Fig 19. Maximum Drain Current vs. Case Temperature

Fig 20. Maximum Drain Current vs. Case Temperature

Fig 21. Threshold Voltage vs. Temperature

Fig 22. Threshold Voltage vs. Temperature

Fig 23. Maximum Avalanche Energy vs. Drain Current

Fig 24. Maximum Avalanche Energy vs. Drain Current


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q1)

Fig 26. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q2)

Fig 27. Single Avalanche Event: Pulse Current vs. Pulse Width (Q1)

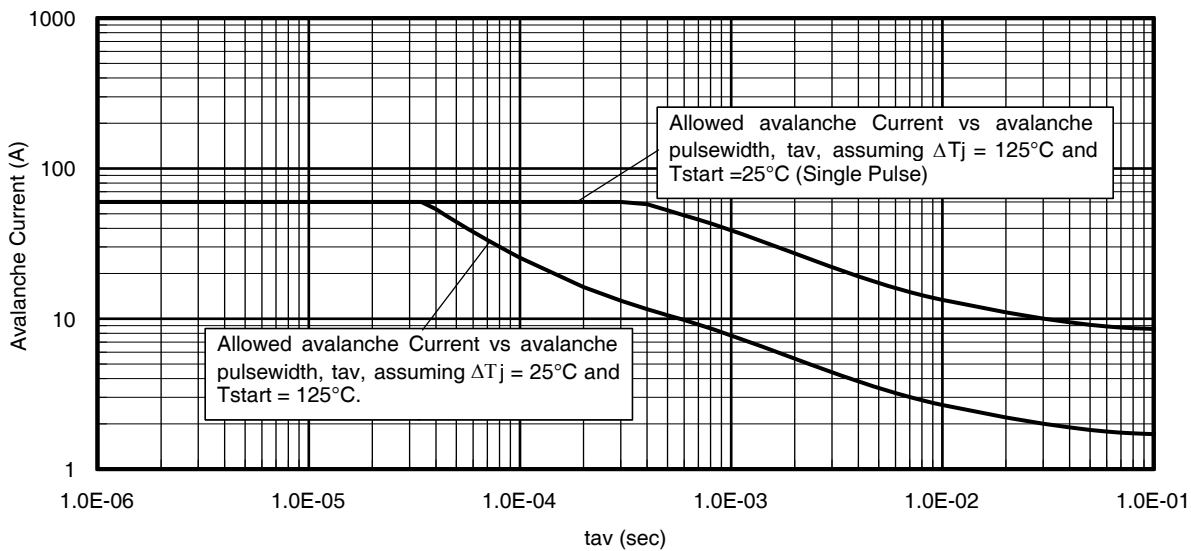
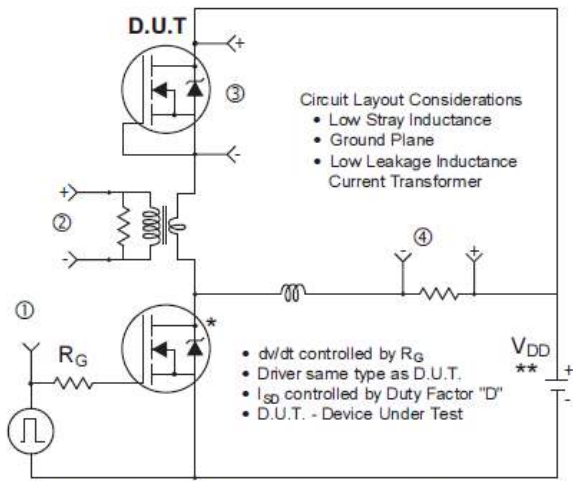
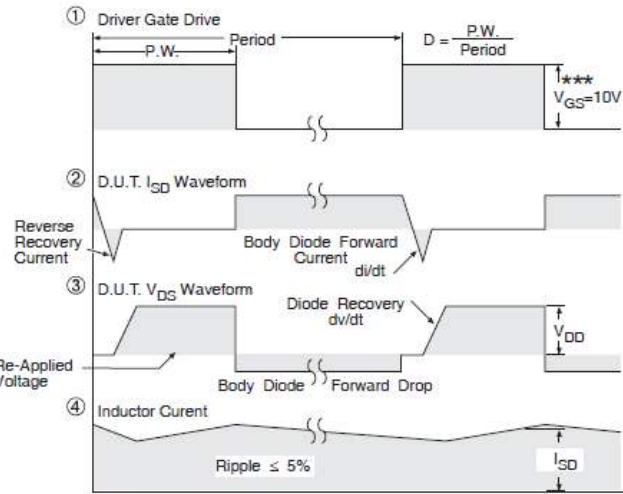


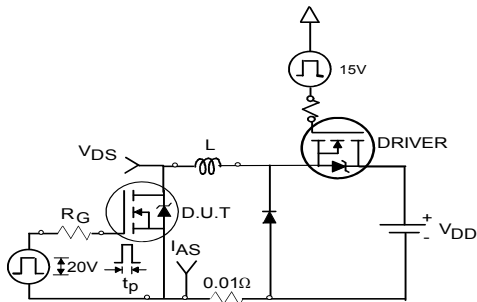
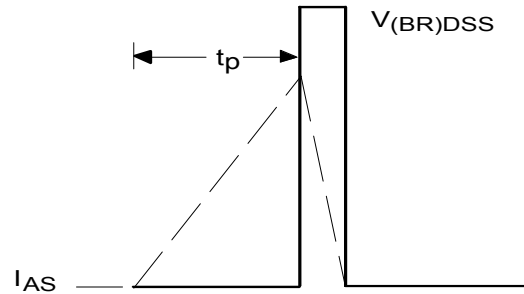
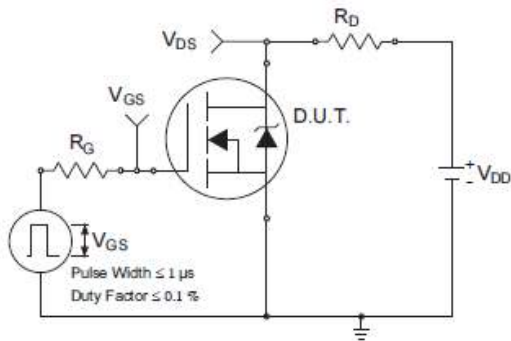
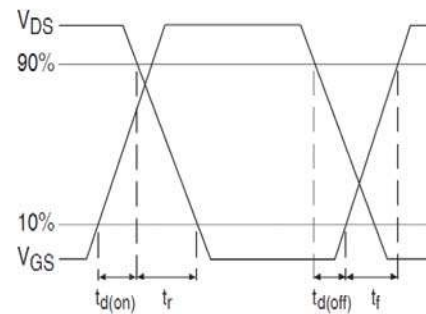
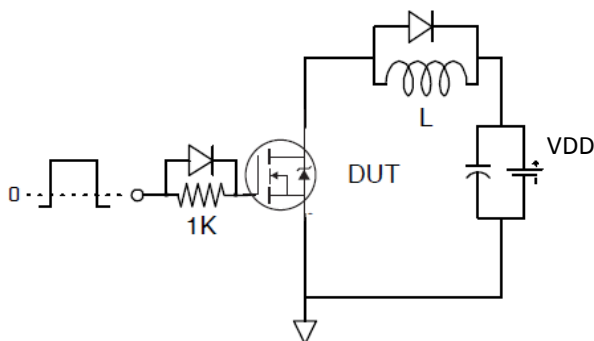
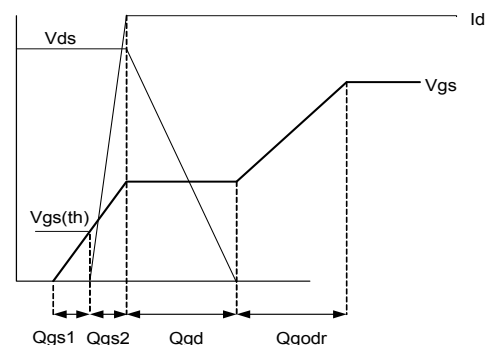
Fig 28. Single Avalanche Event: Pulse Current vs. Pulse Width (Q2)

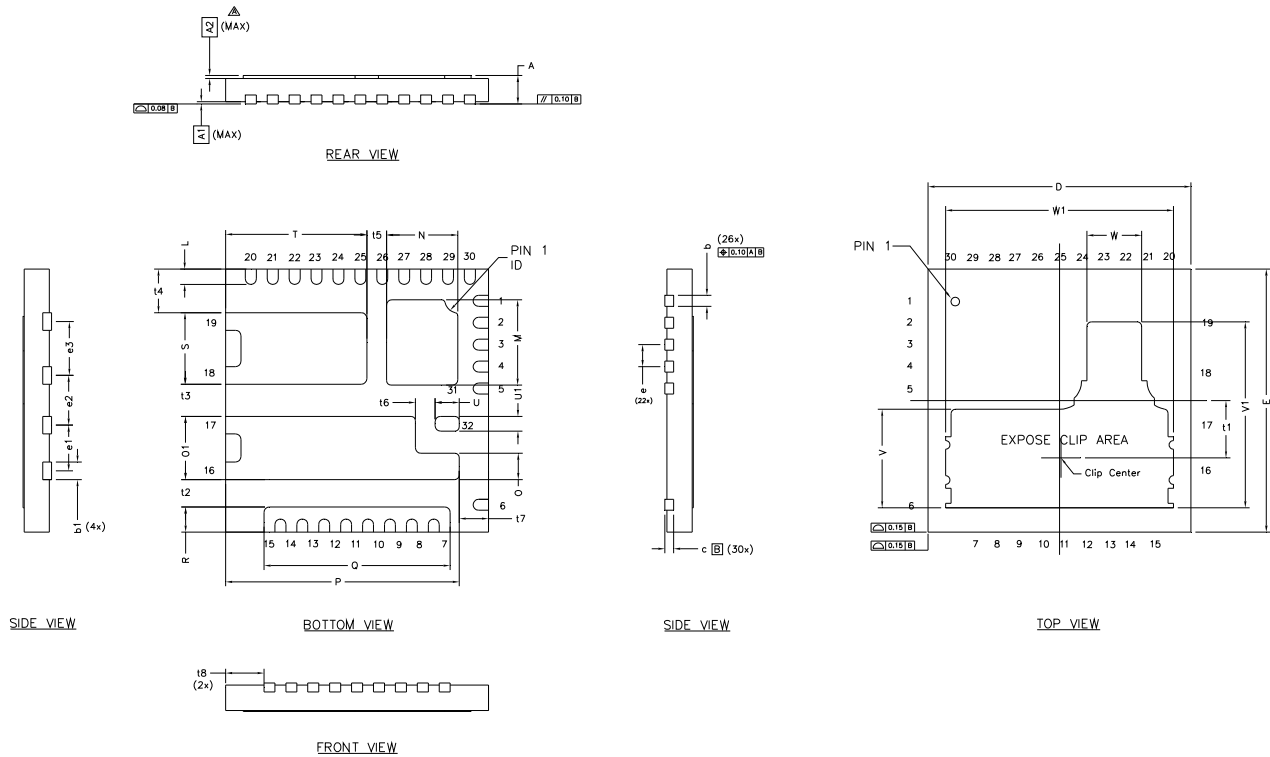


* Use P-Channel Driver for P-Channel Measurements
 ** Reverse Polarity for P-Channel

Fig 29. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs


*** $V_{GS} = 5V$ for Logic Level Devices


Fig 30a. Unclamped Inductive Test Circuit

Fig 30b. Unclamped Inductive Waveforms

Fig 31a. Switching Time Test Circuit

Fig 31b. Switching Time Waveforms

Fig 32a. Gate Charge Test Circuit

Fig 32b. Gate Charge Waveform

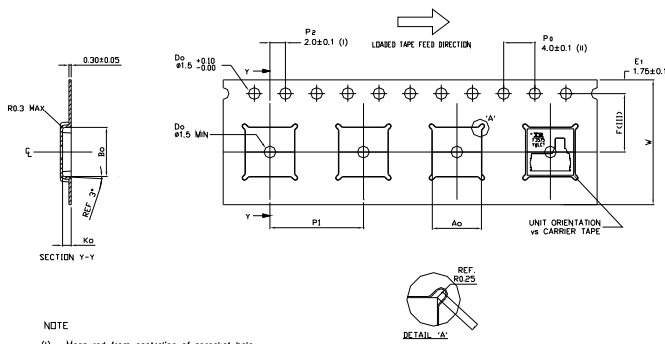
Dual PQFN 6x6 Outline Package Details


DIM	MILLIMETERS		INCHES		DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.55	0.75	.0217	.0295	Q	4.150	4.350	.1634	.1713
A1	0.000	0.050	.0000	.0020	R	0.475	0.675	.0187	.0266
A2	0.000	0.070	.0000	.0028	S	1.530	1.730	.0602	.0681
b	0.20	0.30	.0079	.0118	T	3.123	3.323	.1230	.1308
b1	0.350	0.450	.0138	.0177	t1	1.207	1.407	.0475	.0554
c	0.203	REF.	.0080	REF.	t2	0.525	0.725	.0207	.0285
D	6.000	BASIC	.2362	BASIC	t3	0.634	0.834	.0250	.0328
E	6.000	BASIC	.2362	BASIC	t4	0.896	1.096	.0353	.0431
e	0.500	BASIC	.0197	BASIC	t5	0.350	0.550	.0138	.0217
e1	1.041	BASIC	.0410	BASIC	t6	0.350	0.550	.0138	.0217
e2	1.134	BASIC	.0446	BASIC	t7	0.569	0.769	.0224	.0303
e3	1.230	BASIC	.0484	BASIC	t8	0.775	0.975	.0305	.0384
L	0.300	0.400	.0118	.0157	U	0.450	0.650	.0177	.0256
M	1.846	2.046	.0727	.0806	U1	0.237	0.437	.0093	.0172
N	1.527	1.727	.0601	.0680	v	2.147	2.347	.0845	.0924
O	0.500	0.700	.0197	.0276	V1	4.140	4.340	.1630	.1709
O1	1.341	1.541	.0528	.0607	W	1.148	1.348	.0452	.0531
P	5.231	5.431	.2059	.2138	W1	5.100	5.300	.0200	.0208

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

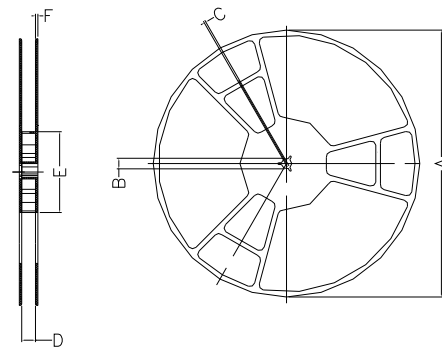
For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Dual PQFN 6x6 Outline Tape and Reel

NOTE

- (I) Measured from centreline of sprocket hole to centreline of pocket.
 - (II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
 - (III) Measured from centreline of sprocket hole to centreline of pocket.
 - (IV) Other material available.
 - (V) Typical SR of form tape Max 10 OHM/SQ.
- ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.
MATERIAL: CONDUCTIVE POLYSTYRENE (IV)

CODE	DIMENSION (MM)		DIMENSION (INCH)	
	MIN	MAX	MIN	MAX
A0	6.20	6.40	0.244	0.252
B0	6.20	6.40	0.244	0.252
K0	1.00	1.20	0.039	0.047
F	7.40	7.50	0.291	0.299
F1	11.90	12.10	0.469	0.476
W	15.70	16.30	0.618	0.642



- NOTES:
1. MATERIAL: POLYSTYRENE (WHITE)
 2. ANTISTATIC COATED
 3. FLANGE WARRAGE: ± 5 UM MAXIMUM
 4. ALL DIMENSIONS ARE IN UM
 5. SR = SURFACE RESISTIVITY: 10⁴ TO 10¹⁰ OHM²/SQ.
 6. GENERAL TOLERANCE: ±0.25 UNLESS OTHERWISE SPECIFIED.
 7. TOTAL THICKNESS OF REEL: W2=22.4 MAX.

SYMBOL	DIMENSION (MM)		DIMENSION (INCH)	
	MIN	MAX	MIN	MAX
A	126.00	130.25	12.835	13.002
B	12.80	13.20	0.504	0.520
C	1.95	2.45	0.077	0.096
D	16.40	16.90	0.646	0.744
E	98.00	102.00	3.858	4.016
F	2.00	2.00	0.079	0.110

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information†

Qualification level	Industrial (per JEDEC JESD47F †† guidelines)	
Moisture Sensitivity Level	DUAL PQFN 6mm x 6mm	MSL2 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$,
Q1: $L = 0.14 \text{ mH}$, $R_G = 50\Omega$, $I_{AS} = 32\text{A}$;
Q2: $L = 0.24 \text{ mH}$, $R_G = 50\Omega$, $I_{AS} = 63\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J approximately 90°C .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current is limited to Q1 = 60A & Q2 = 60A by source bonding technology.
- ⑧ Pulsed drain current is limited to 240A by source bonding technology.