40-A, 8-V to 14-V INPUT, 3-V to 5.25-V OUTPUT, NON-ISOLATED, ADJUSTABLE POWER MODULE

FEATURES

- Up to 40-A Output Current
- 8-V to 14-V Input Voltage
- Wide-Output Voltage Adjust (3.0 V to 5.25 V)
- ±1.5% Total Output Voltage Variation
- Efficiencies up to 96%
- Output Overcurrent Protection (Nonlatching, Auto-Reset)
- Operating Temperature: –40°C to 85°C
- Safety Agency Approvals: (Pending)
  - UL/IEC/CSA-C22.2 60950-1
- Prebias Startup
- On/Off Inhibit
- Differential Output Voltage Remote Sense
- Adjustable Undervoltage Lockout
- Auto-Track™ Sequencing
- Multi-Phase, Switch-Mode Topology
- TurboTrans™ Technology
- Designed to meet Ultra-Fast Transient Requirements up to 300 A/μs
- SmartSync Technology
- Parallel Operation

APPLICATIONS

- Complex Multi-Voltage Systems
- Servers
- Workstations

DESCRIPTION

The PTH08T255W is a high-performance 40-A rated, non-isolated power module. This module represents the 2nd generation of the popular PTH series power modules with a reduced footprint and improved features.

Operating from an input voltage range of 8 V to 14 V, the PTH08T255W requires a single resistor to set the output voltage to any value over the range, 3.0 V to 5.25 V. The wide input voltage range makes the PTH08T255W particularly suitable for advanced computing and server applications that utilize a loosely regulated 9.6-V to 12-V intermediate distribution bus.

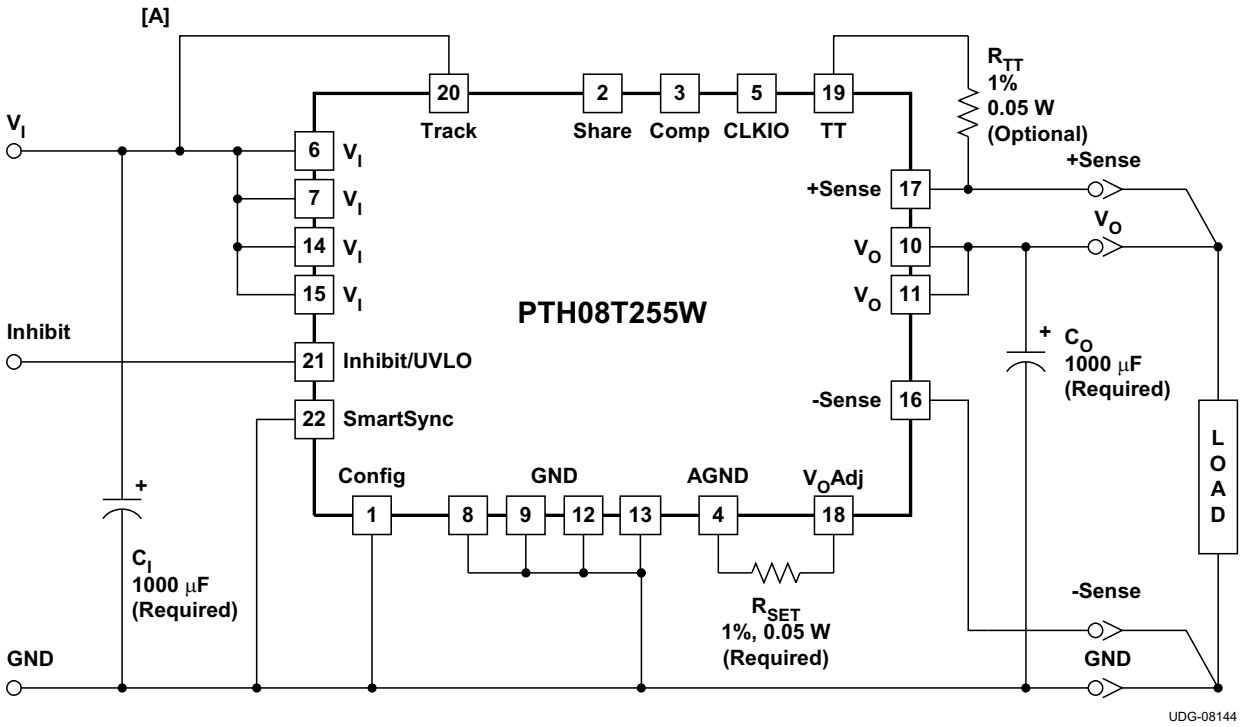
The module incorporates a comprehensive list of features. Output overcurrent and over-temperature shutdown protects against most load faults. A differential remote sense ensures tight load regulation. An adjustable under-voltage lockout allows the turn-on voltage threshold to be customized. Auto-Track™ sequencing is a popular feature that greatly simplifies the simultaneous power-up and power-down of multiple modules in a power system. Additionally, the capability to current share between multiple PTH08T255W modules allows for load currents greater than 40A on a single rail.

The PTH08T255W includes new patented technologies, **TurboTrans™** and **SmartSync**. The TurboTrans feature optimizes the transient response of the regulator while simultaneously reducing the quantity of external output capacitors required to meet a target voltage deviation specification. Additionally, for a target output capacitor bank, TurboTrans can be used to significantly improve the regulators transient response by reducing the peak voltage deviation. SmartSync allows for switching frequency synchronization of multiple modules, thus simplifying EMI noise suppression tasks and reducing input capacitor RMS current requirements.

The module uses double-sided surface mount construction to provide a low profile and compact footprint. Package options include both through-hole and surface mount configurations that are lead (Pb) - free and RoHS compatible.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

STANDARD APPLICATION



A. When using the AutoTrack feature with the PTH08T225W, a 100-kΩ pull-up resistor to V_I is required. If the AutoTrack feature is not used, this pin must be directly connected to V_I.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

DATASHEET TABLE OF CONTENTS

ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

					UNIT
V_{track}	Track pin voltage			–0.3 to V_I + 0.3	V
T_A	Operating temperature range	Over V_I range		–40 to 85	°C
T_{wave}	Wave soldering temperature	Surface temperature of module body or pins **(5 seconds maximum)**	AD suffix	260	
T_{reflow}	Solder reflow temperature	Surface temperature of module body or pins	AS suffix	235(1)	
			AZ suffix	260(1)	
T_{stg}	Storage temperature	Storage temperature of module removed from shipping package		–55 to 125	
T_{pkg}	Packaging temperature	Shipping Tray or Tape and Reel storage or bake temperature		45	
	Mechanical shock	Per Mil-STD-883D, Method 2002.3 1 msec, 1/2 sine, mounted	AD suffix	500	G
			AS and AZ suffix	125	
	Mechanical vibration	Mil-STD-883D, Method 2007.2 20-2000 Hz		20	
	Weight			16.7	grams
	Flammability	Meets UL94V-O			

(1) During reflow of surface mount package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

ELECTRICAL CHARACTERISTICS
PTH08T255W

T_A = 25°C, V_I = 12 V, V_O = 3.3 V, C_I = 1000 µF, C_O = 1000 µF, and I_O = I_O max (unless otherwise stated)

PARAMETER		TEST CONDITIONS			PTH08T255W			UNIT
					MIN	TYP	MAX	
I_O	Output current	Over V_O range	25°C, natural convection		0		40	A
			60°C, 200 LFM		0		40	
V_I	Input voltage range	Over I_O and V_O range			8.0		14	V
V_{OADJ}	Output voltage adjust range	Over I_O range			3.0		5.25	V
V_O	Set-point voltage tolerance					±0.5	±1 (1)	%V_o
	Temperature variation	–40°C < T_A < 85°C				±0.3		%V_o
	Line regulaltion	Over V_I range				±5		mV
	Load regulation	Over I_O range				±5		mV
	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C					±1.5 (1)	%V_o
η	Efficiency	I_O = 30 A	R_{SET} = 1.36 kΩ, V_O = 5.0 V			95%		
			R_{SET} = 34.5 kΩ, V_O = 3.3 V			94%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth				20		mV_{PP}
I_{LIM}	Overcurrent threshold	Reset, followed by auto-recovery				80		A
t_{tr}	Transient response	2.5 A/µs load step 50 to 100% $I_O$max	w/o TurboTrans C_O= 1000 µF, TypeC	Recovery time		200		µs
ΔV_{tr}				V_O over/undershoot		135		mV
t_{trTT}			w/ TurboTrans C_O= 5000 µF, TypeC R_{TT} = short	Recovery time		400		µs
ΔV_{trTT}				V_O over/undershoot		35		mV
I_{IL}	Track input current (pin 20)	Pin to GND					–130 (2)	µA
dV_{track}/dt	Track slew rate capability	C_O ≤ C_O (max)					1	V/ms
$UVLO_{ADJ}$	Adjustable Under-voltage lockout (pin 21)	V_I increasing, R_{UVLO} = OPEN				7.2	8.0	V
		V_I decreasing, R_{UVLO} = OPEN				6.7		
		Hysteresis				0.5		
	Inhibit control (pin 21)	Input high voltage (V_{IH})					Open (3)	V
		Input low voltage (V_{IL})			-0.2		0.6	
		Input low current (I_{IL}), Pin 21 to GND				-125		µA
I_{in}	Input standby current	Inhibit (pin 21) to GND, Track (pin 20) open				35		mA
f_s	Switching frequency	Over V_I and I_O ranges, SmartSync (pin 22) to GND				600 (4)		kHz
f_{SYNC}	Synchronization (SYNC) control (pin 22)	Synchronization frequency applied to pin 22			240 (4)		400 (4)	kHz
V_{SYNCH}		SYNC High-Level Input Voltage			2.0		5.5	V
V_{SYNCL}		SYNC Low-Level Input Voltage					0.8	V
t_{SYNC}		SYNC Minimum Pulse Width			200			nSec
C_I	External input capacitance			Nonceramic	1000 (5)			µF
				Ceramic		22		

(1) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/C or better temperature stability.
(2) A low-leakage (<100 nA), open-drain device, such as MOSFET or voltage supervisor IC, is recommended to control pin 20. When using this feature, a 100kΩ pull-up resistor to V_I is required. If unused, this pin must be directly connected to V_I. See the Auto-Track section of the datasheet for more information.
(3) Do not place an external pull-up on this pin. If it is left open-circuit, the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET is recommended for control. For additional information, see the On/Off Inhibit section of the datasheet.
(4) The PTH08T255W is a two-phase power module. Each phase switches at 300kHz typical, 180° out of phase from one another. The over-all switching frequency is 600 kHz typical. SmartSync controls the frequency of an individual phase.
(5) A 1000 µF electrolytic input capacitor is required for proper operation. The input capacitor must be rated for a minimum of 750 mA rms of ripple current.

ELECTRICAL CHARACTERISTICS
PTH08T255W
(continued)

T_A = 25°C, V_I = 12 V, V_O = 3.3 V, C_I = 1000 µF, C_O = 1000 µF, and I_O = I_O max (unless otherwise stated)

PARAMETER		TEST CONDITIONS			PTH08T255W			UNIT
					MIN	TYP	MAX	
C_O	External output capacitance	w/o TurboTrans	Capacitance Value	Nonceramic	1000 (6)		8000 (7)	µF
				Ceramic			1000	
			Equivalent series resistance (non-ceramic)		3			mΩ
		w/ TurboTrans	Capacitance Value		see table (6) (8)			µF
			Capacitance × ESR product (C_O × ESR)		1000		10000 (8)	µF×mΩ
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign			2.56			10^6 Hr

(6) 1000 µF of external non-ceramic output capacitance is required for basic operation. Adding additional capacitance at the load further improves transient response. Up to 1000 µF of ceramic capacitance may be added in addition to the required non-ceramic capacitance. See the Capacitor Application Information section and the TuboTrans Technology section for more guidance.

(7) This is the calculated maximum when not using *TurboTrans™* technology. This value includes both ceramic and non-ceramic capacitors. The minimum ESR requirement often results in a lower value of output capacitance. See the Capacitor Application Information section for further guidance.

(8) When using *TurboTrans™* technology, a minimum value of output capacitance is required for proper operation. Additionally, low ESR capacitors are required for proper operation. See the TurboTrans Technology section for further guidance.

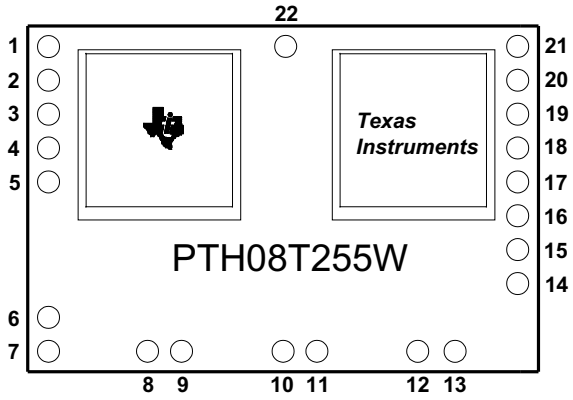


Table 1. TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	6,7,14,15	The positive input voltage power node to the module, which is referenced to common GND.
V_O	10,11	The regulated positive power output with respect to GND.
GND	8,9,12,13	This is the common ground connection for the V_I and V_O power connections. It is also the 0 V_{dc} reference for the control inputs.
Inhibit(1) and UVLO	21	The Inhibit pin is an open-collector/drain, negative logic input that is referenced to GND. Applying a low level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied. This pin is also used for input undervoltage lockout (UVLO) programming. Connecting a resistor from this pin to GND (pin 13) allows the ON threshold of the UVLO to be adjusted higher than the default value. For more information, see the Application Information section.
V_o Adjust	18	A 0.05 W 1% resistor must be directly connected between this pin and pin4 (AGND) to set the output voltage to a value higher than 3.0V. The temperature stability of the resistor should be 100 ppm/°C (or better). The setpoint range for the output voltage is from 3.0V to 5.25V. If left open circuit, the output voltage defaults to its lowest value. For further information on output voltage adjustment, resistor values and equation see the related application note.
+ Sense	17	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. The +Sense pin should always be connected to V_O, either at the load for optimal voltage accuracy, or at the module (pin 11).
– Sense	16	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. The –Sense pin should always be connected to GND, either at the load for optimal voltage accuracy, or at the module (pin 13).
Track	20	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 25 ms after a valid input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the module's output voltage follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. ***When using this feature, a 100 kΩ pull-up resistor should be placed between the Track pin and V_I. If unused, this input MUST be connected directly to V_I.*** NOTE: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, see the related application note.
TurboTrans™	19	This input pin adjusts the transient response of the regulator. To activate the *TurboTrans™* feature, a 1%, 50mW resistor, must be connected between this pin and pin 17 (+Sense) very close to the module. For a given value of output capacitance, a reduction in peak output voltage deviation is achieved by utililizing this feature. If unused, this pin must be left open-circuit. The resistance requirement can be selected from the TurboTrans resistor table in the Application Information section. External capacitance must never be connected to this pin unless the TurboTrans resistor value is a short, 0Ω.
SmartSync	22	This input pin sychronizes the switching frequency of the module to an external clock frequency. The SmartSync feature can be used to sychronize the switching frequency of multiple modules, aiding EMI noise suppression efforts. The external synchronization frequency must be present before a valid input voltage is present, or before the release of inhibit control. If unused, this pin MUST be connected to GND. For more information, please review the Application Information section.
CONFIG	1	When two modules are connected together to share load current one must be configured as the MASTER and the other as the SLAVE. This pin is used to configure the module as either MASTER or SLAVE. To configure the module as the MASTER, connect this pin to GND. To configure the module as the SLAVE, connect this pin to V_I (pin 6). When not sharing current, this pin should be connected to GND.
Share	2	This pin is used when connecting two modules together to share load current. When two modules are sharing current the Share pin of both modules must be connected together. When not sharing current, this pin MUST be left open (floating).
Comp	3	This pin is used when connecting two modules together to share load current. When two modules are sharing current the Comp pin of both modules must be connected together. When not sharing current, this pin MUST be left open (floating).
AGND	4	This pin is the internal analog ground of the module. This pin provides the return path for the V_OAdjust resistor (R_{SET}). When two modules are sharing current the AGND pin of both modules must be connected together. Also, when two modules are connected, R_{SET} must be connected only on the MASTER module.
CLKIO	5	This pin is used when connecting two modules together to share load current. When two modules are sharing current the CLKIO pin of both modules must be connected together. When not sharing current, this pin MUST be left open (floating).

(1) Denotes negative logic: Open = Normal operation, Ground = Function active

TYPICAL CHARACTERISTICS(1)(2)

CHARACTERISTIC DATA (V_I = 12 V)

EFFICIENCY vs LOAD CURRENT

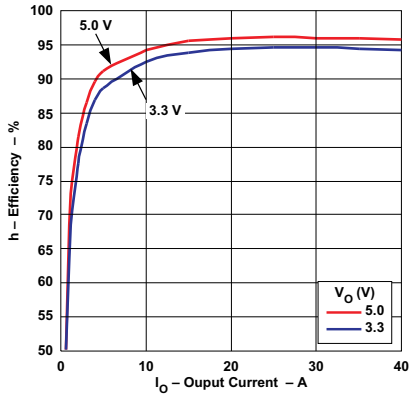


Figure 1.

OUTPUT RIPPLE vs LOAD CURRENT

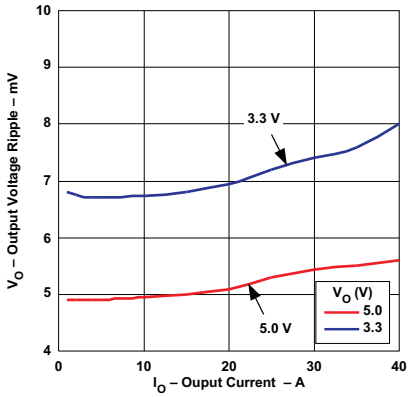


Figure 2.

POWER DISSIPATION vs LOAD CURRENT

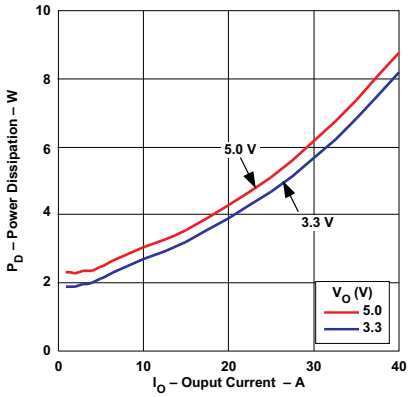


Figure 3.

AMBIENT TEMPERATURE vs LOAD CURRENT

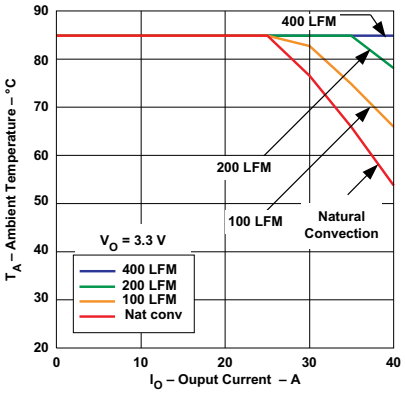


Figure 4.

AMBIENT TEMPERATURE vs LOAD CURRENT

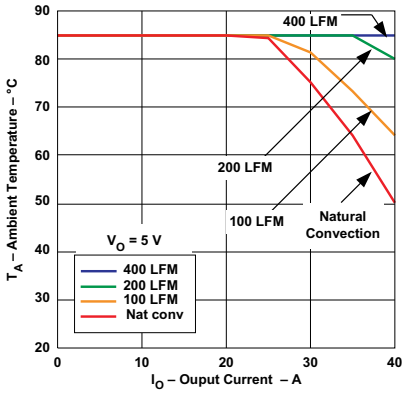


Figure 5.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm × 100 mm double-sided PCB with 2 oz. copper and the direction of airflow from pin 10 to pin 22. For surface mount packages (AS and AZ suffix), multiple vias must be utilized. Please refer to the mechanical specification for more information. Applies to Figure 4 and Figure 5.

APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE

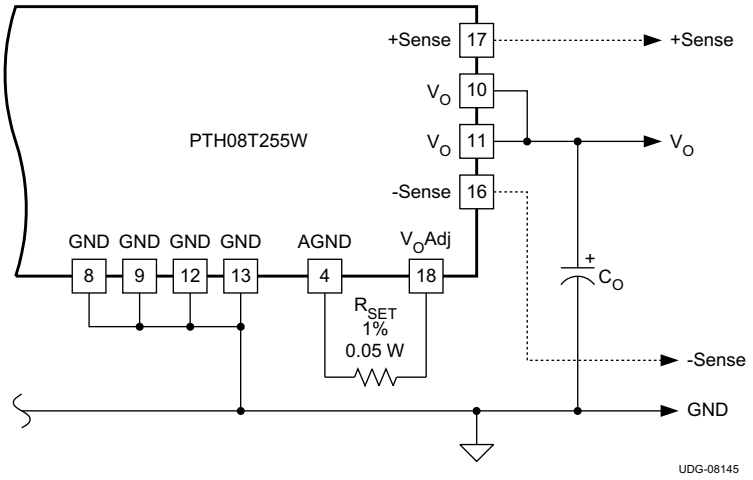
The V_o Adjust control sets the output voltage of the PTH08T255W. The adjustment range of the PTH08T255W is 3.0 V to 5.25 V. The adjustment method requires the addition of a single external resistor, R_{SET}, that must be connected directly between pins V_o Adjust (pin 18) and AGND (pin 4). Figure 6 shows the placement of the required resistor.

To set the output voltage, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of standard resistor values given in Table 2.

$$R_{SET} = \left(\frac{0.7}{\left(\frac{V_O - 0.7}{30.1} \right) - \frac{0.7}{10}} - 8.25 \right) (k\Omega) \quad (1)$$

Table 2. Output Voltage Set-Point Resistor Values

V_O Required (V)	R_{SET} (kΩ)	V_O Required (V)	R_{SET} (kΩ)
3.0	100	4.2	6.81
3.1	63.4	4.3	5.90
3.2	45.3	4.4	4.99
3.3	34.0	4.5	4.22
3.4	27.4	4.6	3.48
3.5	22.1	4.7	2.87
3.6	18.2	4.8(3)	2.32
3.7	15.4	4.9(3)	1.82
3.8	13.0	5.0(3)	1.37
3.9	11.0	5.1(3)	0.931
4.0	9.31	5.2(3)	0.549
4.1	8.06	5.25(3)	0.374



(1) **R_{SET}:** Use a 0.05-W resistor with a tolerance of 1% and temperature stability of 100 ppm/°C (or better). Connect the resistor directly between pins 18 and 4, as close to the regulator as possible, using dedicated PCB traces.

(2) Any capacitance added to the V_O Adjust pin affects the stability of the regulator.

(3) When setting the output voltage to 4.8V or greater, the Auto-Track pin must be directly connected to V_I if the feature is not used. If the Auto-Track feature is utilized, a 100kΩ resistor must connect the Auto-Track pin to V_I.

Figure 6. V_O Adjust Resistor Placement

CAPACITOR RECOMMENDATIONS FOR THE PTH08T255W POWER MODULE

Capacitor Technologies

Electrolytic Capacitors

When using electrolytic capacitors, high quality, computer-grade electrolytic capacitors are recommended. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above -20°C. For operation below -20°C, tantalum, ceramic, or OS-CON type capacitors are required.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

Tantalum, Polymer-Tantalum Capacitors

Tantalum type capacitors may only be used on the output bus, and are recommended for applications where the ambient operating temperature is less than 0°C. The AVX TPS series and Kemet capacitor series are suggested over many other tantalum types due to their lower ESR, higher rated surge, power dissipation, and ripple current capability. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

Input Capacitor (Required)

The PTH08T255W requires a minimum input capacitance of 1000µF. The ripple current rating of the input capacitor must be at least 750 mArms. An optional 22µF X5R/X7R ceramic capacitor is recommended to reduce RMS ripple current.

Input Capacitor Information

The size and value of the input capacitor is determined by the converter's transient performance capability. This minimum value assumes that the converter is supplied with a responsive, low inductance input source. This source should have ample capacitive decoupling, and be distributed to the converter via PCB power and ground planes.

Ceramic capacitors should be located as close as possible to the module's input pins, within 0.5 inch (1,3 cm). Adding ceramic capacitance is necessary to reduce the high-frequency ripple voltage at the module's input. This reduces the magnitude of the ripple current through the electroytic capacitor, as well as the amount of ripple current reflected back to the input source. Additional ceramic capacitors can be added to further reduce the RMS ripple current requirement for the electrolytic capacitor.

The main considerations when selecting input capacitors are the RMS ripple current rating, temperature stability, and less than 100 mΩ of equivalent series resistance (ESR).

Regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of 2 × (maximum dc voltage + ac ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with a sufficient voltage rating to meet this requirement.

When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered.

Output Capacitor (Required)

The PTH08T255W requires a minimum output capacitance of 1000µF of polymer-aluminum, tantulum, or polymer-tantalum type. Ceramic output capacitance can be used in addition to the required non-ceramic type.

The required capacitance above the minimum is determined by actual transient deviation requirements. See the TurboTrans Technology application section within this document for specific capacitance selection.

Output Capacitor Information

When selecting output capacitors, the main considerations are capacitor type, temperature stability, and ESR. When using the TurboTrans feature, the capacitance × ESR product should also be considered (see the following section).

Ceramic output capacitors added for high-frequency bypassing should be located as close as possible to the load to be effective. Ceramic capacitor values below 10µF should not be included when calculating the total output capacitance value.

When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered.

TurboTrans Output Capacitance

TurboTrans allows the designer to optimize the output capacitance according to the system transient design requirement. High quality, ultra-low ESR capacitors are required to maximize TurboTrans effectiveness. When using TurboTrans, the capacitor's capacitance (µF) × ESR (mΩ) product determines its capacitor type; Type A, B, or C. These three types are defined as follows:

Type A = (100 ≤ capacitance × ESR ≤ 1000) (e.g. ceramic) (use Type A capacitors in addition to Type B or C)

Type B = (1000 < capacitance × ESR ≤ 5000) (e.g. polymer-tantalum)

Type C = (5000 < capacitance × ESR ≤ 10,000) (e.g. OS-CON)

When using more than one type of output capacitor, select the capacitor type that makes up the majority of your total output capacitance. When calculating the C×ESR product, use the maximum ESR value from the capacitor manufacturer's datasheet.

Working Examples:

A capacitor with a capacitance of 330µF and an ESR of 5mΩ, has a C×ESR product of 1650µFxmΩ (330µF × 5mΩ). This is a Type B capacitor. A capacitor with a capacitance of 1000µF and an ESR of 8mΩ, has a C×ESR product of 8000µFxmΩ (1000µF × 8mΩ). This is a Type C capacitor.

See the TurboTrans Technology application section within this document for specific capacitance selection.

Table 3 includes a preferred list of capacitors by type and vendor. See the Output Bus / TurboTrans column.

Non-TurboTrans Output Capacitance

If the TurboTrans feature is not used, minimum ESR and maximum capacitor limits must be followed. System stability may be effected and increased output capacitance may be required without TurboTrans.

When using the PTH08T255W, observe the minimum ESR of the entire output capacitor bank. The minimum ESR limit of the output capacitor bank is 7mΩ. A list of preferred low-ESR type capacitors, are identified in Table 3.

When using the PTH08T255W without the TurboTrans feature, the maximum amount of capacitance is 1000 µF of ceramic type. Large amounts of capacitance may reduce system stability.

Utilizing the TurboTrans feature improves system stability, improves transient response, and reduces the amount of output capacitance required to meet system transient design requirements.

Designing for Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 2.5A/µs. The typical voltage deviation for this load transient is given in the Electrical Characteristics table using the minimum required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability.

If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional low ESR ceramic capacitor decoupling. Generally, with load steps greater than 100A/µs, adding multiple 10µF ceramic capacitors plus 10×1µF, and numerous high frequency ceramics (≤0.1µF) is all that is required to soften the transient higher frequency edges. The PCB location of these capacitors in relation to the load is critical. DSP, FPGA and ASIC vendors identify types, location and amount of capacitance required for optimum performance. Low impedance buses, unbroken PCB copper planes, and components located as close as possible to the high frequency devices are essential for optimizing transient performance.

Capacitor Table

Table 3 identifies the characteristics of acceptable capacitors from a number of vendors. The recommended number of capacitors required at both the input and output buses is identified for each capacitor.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.

Table 3. Input/Output Capacitors(1)

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity			Vendor Part No.
	Working Voltage (V)	Value (µF)	Max. ESR at 100 kHz (Ω)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Output Bus		
							No Turbo Trans	TurboTrans (Cap Type)(2)	
Panasonic	25	1000	0.043	1690	16 × 15	1	≥ 2(3)	N/R(4)	EEUFC1E102S
FC (Radial)	25	1800	0.029	2205	16 × 20	1	≥ 1(3)	N/R(4)	EEUFC1E182
FC (SMD)	25	2200	0.028	2490	18 × 21,5	1	≥ 1(3)	N/R(4)	EEVFC1E222N
FK (SMD)	25	1000	0.060	1100	12,5×13,5	1	≥ 2(5)	N/R(4)	EEVFK1V102Q
United Chemi-Con									
PTB Poly-Tant (SMD)	6.3	330	0.025	2600	7,3x4,3x 2,8	N/R(6)	3 - 4(3)	(C) ≥ 2(2)	4PTB337MD6TER
LXZ, Aluminum (Radial)	25	680	0.068	1050	10 × 16	1	2 - 3(3)	N/R(4)	LXZ25VB681M10X20LL
PS, Poly-Alum (Radial)	16	330	0.014	5060	10 × 12,5	2	3	(B) ≥ 2(2)	16PS330MJ12
PXA, Poly-Alum (SMD)	16	330	0.014	5050	10 × 12,2	2	3	(B) ≥ 2(2)	PXA16VC331MJ12TP
PS, Poly-Alum (Radial)	6.3	680	0.010	5500	10 × 12,5	N/R(6)	2	(C) ≥ 1(2)	6PS680MJ12
PXA, Poly-Alum (Radial)	6.3	680	0.010	5500	10 × 12,2	N/R(6)	2	(C) ≥ 1(2)	PXA6.3VC681MJ12TP

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products. In some instances, the capacitor product life cycle may be in decline and have short-term consideration for obsolescence.
RoHS, Lead-free and Material Details
See the capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.

(2) Required capacitors with TurboTrans. See the TransTrans Application information for Capacitor Selection
Capacitor Type Groups by ESR (Equivalent Series Resistance) :
a. Type A = (100 < capacitance × ESR ≤ 1000) (use Type A capacitors in addition to Type B or C)
b. Type B = (1,000 < capacitance × ESR ≤ 5,000)
c. Type C = (5,000 < capacitance × ESR ≤ 10,000)

(3) Total bulk nonceramic capacitors on the output bus with ESR of ≥ 15mΩ to ≤ 30mΩ requires an additional ≥ 200 µF of ceramic capacitor.

(4) Aluminum Electrolytic capacitor not recommended for the TurboTrans due to higher ESR × capacitance products. Aluminum and higher ESR capacitors can be used in conjunction with lower ESR capacitance.

(5) Output bulk capacitor's maximum ESR is ≥ 30 mΩ. Additional ceramic capacitance of ≥ 200 µF is required.

(6) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.

Table 3. Input/Output Capacitors (continued)

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity			Vendor Part No.
	Working Voltage (V)	Value (µF)	Max. ESR at 100 kHz (Ω)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Output Bus		
							No Turbo Trans	TurboTrans (Cap Type)(2)	
Nichicon, Aluminum	25	560	0.060	1060	12,5 × 15	1	≥ 2(7)	N/R(8)	UPM1E561MHH6
HD (Radial)	25	680	0.038	1430	10 × 16	1	≥ 2(7)	N/R(8)	UHD1C681MHR
PM (Radial)	35	560	0.048	1360	16 × 15	1	≥ 2(7)	N/R(8)	UPM1V561MHH6
Sanyo									
SA, OS-CON (Radial)	16	1000	0.015	9700	16 × 26	1	1 - 3	N/R(8)	16SA1000M
SP OS-CON (Radial)	10	470	0.015	4500	10 × 11,5	N/R(9)	2 - 3	(C) ≥ 2(10)	10SP470M
SEPC, OS-CON (Radial)	16	330	0.016	4700	10 × 12,7	2	3 - 4	(B) ≥ 2(10)	16SVP330M
SVPA, OS-CON (SMD)	6.3	820	0.012	4700	8 × 11,9	N/R(9)	1 - 2(7)	(C) ≥ 1(10)(7)	6SVPC820M
AVX Tantalum, Series 3	6.3	680	0.035	2400	7,3×4,3×4,1	N/R(9)	2 - 7(7)	N/R(8)	TPSE477M010R0045
TPM Multianode	6.3	470	0.018	3800	7,3×4,3×4,1	N/R(9)	2 - 3(7)	(C) ≥ 2(10)(7)	TPME687M006#0018
Kemet, Poly-Tantalum	6.3	470	0.040	2000	7,3×4,3×4	N/R(9)	2 - 7(7)	N/R(8)	T520X337M010AS
T520 (SMD)	6.3	330	0.015	3800	7,3×4,3×4	N/R(9)	3	(B) ≥ 2(10)	T530X337M010AS
Vishay-Sprague									
94SA, OS-CON (Radial)	16	1000	0.015	9740	16 × 25	1	1 - 3	N/R(8)	94SA108X0016HBP
94SVP OS-CON (SMD)	16	330	0.017	4500	10 × 12,7	2	3	(C) ≥ 1(10)	94SVP827X06R3F12
Kemet, Ceramic X5R	16	10	0.002	–	3225	1	≥ 1(11)	(A)(10)	C1210C106M4PAC
(SMD)	6.3	47	0.002			N/R(9)	≥ 1(11)	(A)(10)	C1210C476K9PAC
Murata, Ceramic X5R	6.3	100	0.002	–	3225	N/R(9)	≥ 1(11)	(A)(10)	GRM32ER60J107M
(SMD)	6.3	47				N/R(9)	≥ 1(11)	(A)(10)	GRM32ER60J476M
	25	22				1	≥ 1(11)	(A)(10)	GRM32ER61E226K
	16	10				1	≥ 1(11)	(A)(10)	GRM32DR61C106K
TDK, Ceramic X5R	6.3	100	0.002	–	3225	N/R(9)	≥ 1(11)	(A)(10)	C3225X5R0J107MT
(SMD)	6.3	47				N/R(9)	≥ 1(11)	(A)(10)	C3225X5R0J476MT
	16	10				1	≥ 1(11)	(A)(10)	C3225X5R1C106MT0
	16	22				1	≥ 1(11)	(A)(10)	C3225X5R1C226MT

(7) Total bulk nonceramic capacitors on the output bus with ESR of ≥ 15mΩ to ≤ 30mΩ requires an additional ≥ 200 µF of ceramic capacitor.
(8) Aluminum Electrolytic capacitor not recommended for the TurboTrans due to higher ESR × capacitance products. Aluminum and higher ESR capacitors can be used in conjunction with lower ESR capacitance.
(9) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.
(10) Required capacitors with TurboTrans. See the TransTrans Application information for Capacitor Selection
Capacitor Type Groups by ESR (Equivalent Series Resistance) :
a. Type A = (100 < capacitance × ESR ≤ 1000) (use Type A capacitors in addition to Type B or C)
b. Type B = (1,000 < capacitance × ESR ≤ 5,000)
c. Type C = (5,000 < capacitance × ESR ≤ 10,000)
(11) Maximum ceramic capacitance on the output bus is ≤ 1000 µF. Any combination of the ceramic capacitor values is limited to 1000 µF for non-TurboTrans applications. The total capacitance is limited to 8000 µF which includes all ceramic and non-ceramic types.

TurboTrans™ Technology

TurboTrans technology is a feature introduced in the T2 generation of the PTH/PTV family of power modules. TurboTrans optimizes the transient response of the regulator with added external capacitance using a single external resistor. Benefits of this technology include reduced output capacitance, minimized output voltage deviation following a load transient, and enhanced stability when using ultra-low ESR output capacitors. The amount of output capacitance required to meet a target output voltage deviation is reduced with TurboTrans activated. Likewise, for a given amount of output capacitance, with TurboTrans engaged, the amplitude of the voltage deviation following a load transient is reduced. Applications requiring tight transient voltage tolerances and minimized capacitor footprint area benefits greatly from this technology.

TurboTrans™ Selection

Utilizing TurboTrans requires connecting a resistor, R_{TT}, between the +Sense pin (pin17) and the TurboTrans pin (pin19). The value of the resistor directly corresponds to the amount of output capacitance required. All T2 products require a minimum value of output capacitance whether or not TurboTrans is utilized. For the PTH08T255W, the minimum required capacitance is 1000µF. When using TurboTrans, capacitors with a capacitance × ESR product below 10,000 µF×mΩ are required. (Multiply the capacitance (in µF) by the ESR (in mΩ) to determine the capacitance × ESR product.) See the Capacitor Selection section of the datasheet for a variety of capacitors that meet this criteria.

Figure 7 and Figure 8 show the amount of output capacitance required to meet a desired transient voltage deviation with and without TurboTrans for several capacitor types; TypeB (e.g. polymer-tantalum) and TypeC (e.g. OS-CON). To calculate the proper value of R_{TT}, first determine your required transient voltage deviation limits and magnitude of your transient load step. Next, determine what type of output capacitors to be used. (If more than one type of output capacitor is used, select the capacitor type that makes up the majority of your total output capacitance.) Knowing this information, use the chart in Figure 7 that corresponds to the capacitor type selected. To use the chart, begin by dividing the maximum voltage deviation limit (in mV) by the magnitude of your load step (in Amps). This gives a mV/A value. Find this value on the Y-axis of the appropriate chart. Read across the graph to the *'With TurboTrans'* plot. From this point, read down to the X-axis which lists the minimum required capacitance, C_O, to meet that transient voltage deviation. The required R_{TT} resistor value can then be calculated using the equation or selected from the TurboTrans table. The TurboTrans tables include both the required output capacitance and the corresponding R_{TT} values to meet several values of transient voltage deviation for 25%(10A), 50%(20A), and 75%(30A) output load steps.

The chart can also be used to determine the achievable transient voltage deviation for a given amount of output capacitance. Selecting the amount of output capacitance along the X-axis, reading up to the *'With TurboTrans'* curve, and then over to the Y-axis, gives the transient voltage deviation limit for that value of output capacitance. The required R_{TT} resistor value can be calculated using the equation or selected from the TurboTrans table.

As an example, let's look at a 12-V application requiring a 80 mV deviation during an 20A load transient. A majority of 560µF, 10mΩ ouput capacitors are used. Use the 12 V, Type C capacitor chart, Figure 8. Dividing 80mV by 20A gives 4mV/A transient voltage deviation per amp of transient load step. Select 4mV/A on the Y-axis and read across to the *'With TurboTrans'* plot. Following this point down to the X-axis gives us a minimum required output capacitance of approximately 1700µF. The required R_{TT} resistor value for 1700µF can then be calculated or selected from Table 5. The required R_{TT} resistor is approximately 31.6kΩ.

To see the benefit of TurboTrans, follow the 4mV/A marking across to the *'Without TurboTrans'* plot. Following that point down shows that you would need a minimum of 5500µF of output capacitance to meet the same transient deviation limit. This is the benefit of TurboTrans.

PTH08T255W Type B Capacitors

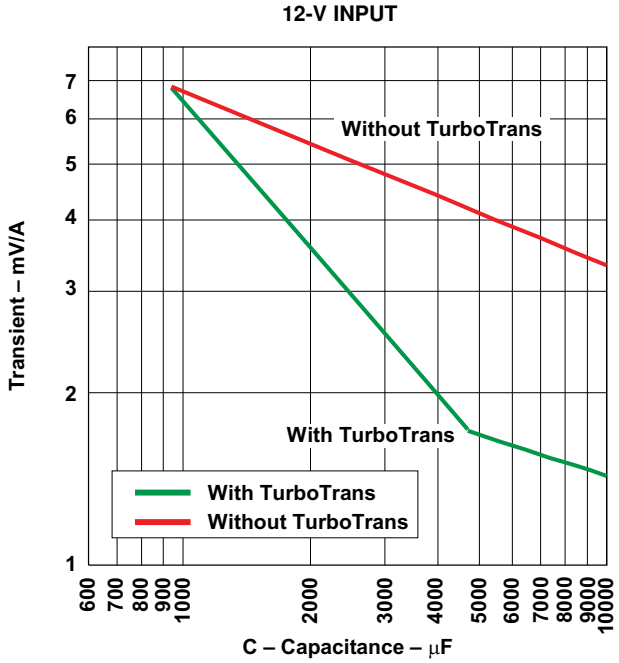


Figure 7. Capacitor Type B,
1000 < C(µF)×ESR(mΩ) ≤ 5000 (e.g. Polymer-Tantalum)

Table 4. Type B TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			12 Volt Input	
25% load step (10 A)	50% load step (20 A)	75% load step (30 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
65	130	195	1000	open
60	120	180	1100	187
50	100	150	1360	64.9
40	80	120	1760	28.7
30	60	90	2470	11.8
25	50	75	3050	6.19
20	40	60	4000	1.96
15	30	45	8000	short

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming Equation 2.

$$R_{TT} = 40 \times \frac{1-(C_O/4700)}{(5 \times C_O/4700)-1} \ (k\Omega) \quad (2)$$

Where C_O is the total output capacitance in µF. C_O values greater than or equal to 4700 µF require R_{TT} to be a short, 0Ω. (Equation 2 results in a negative value for R_{TT} when C_O > 4700 µF.)

To ensure stability, a minimum amount of output capacitance is required for a given R_{TT} resistor value. The value of R_{TT} must be calculated using the minimum required output capacitance determined from Figure 7.

PTH08T255W Type C Capacitors

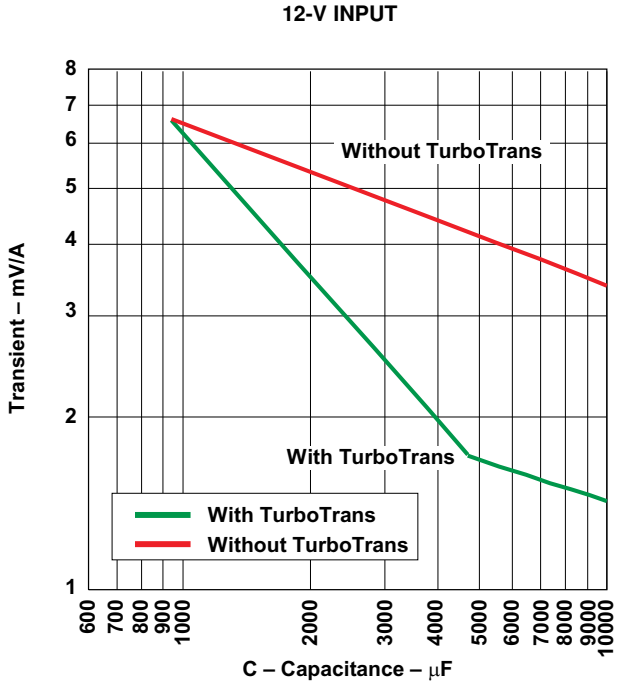


Figure 8. Capacitor Type C,
5000 < C(µF)×ESR(mΩ) ≤ 10,000(e.g. OS-CON)

Table 5. Type C TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			12 Volt Input	
25% load step (10 A)	50% load step (20 A)	75% load step (30 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
65	130	195	1000	open
60	120	180	1050	280
50	100	150	1300	75.0
40	80	120	1700	31.6
30	60	90	2400	12.4
25	50	75	3000	6.49
20	40	60	3950	2.00
15	30	45	8000	short

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming Equation 3.

$$R_{TT} = 40 \times \frac{1-(C_O/4700)}{(5 \times C_O/4700)-1} \ (k\Omega) \quad (3)$$

Where C_O is the total output capacitance in µF. C_O values greater than or equal to 4700 µF require R_{TT} to be a short, 0Ω. (Equation 3 results in a negative value for R_{TT} when C_O > 4700 µF). To ensure stability, a minimum amount of output capacitance is required for a given R_{TT} resistor value. The value of R_{TT} must be calculated using the minimum required output capacitance determined from Figure 8.

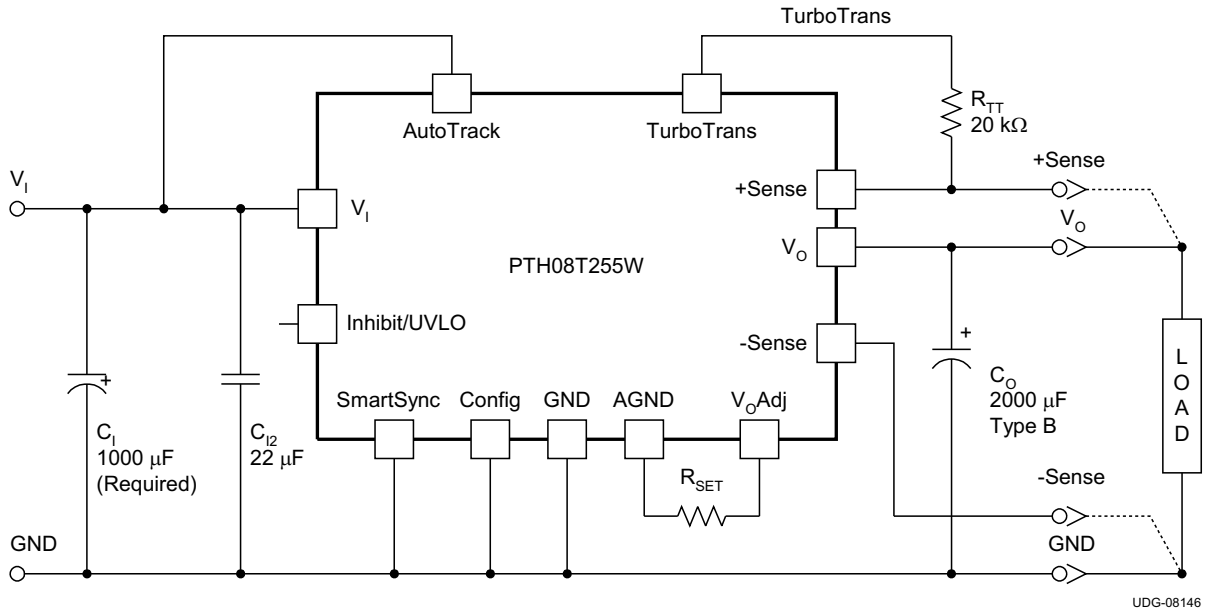


Figure 9. Typical TurboTrans™ Application

Soft-Start Power Up

The Auto-Track feature allows the power-up of multiple PTH/PTV modules to be directly controlled from the Track pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the Track pin should be directly connected to the input voltage, V_I (see Figure 10).

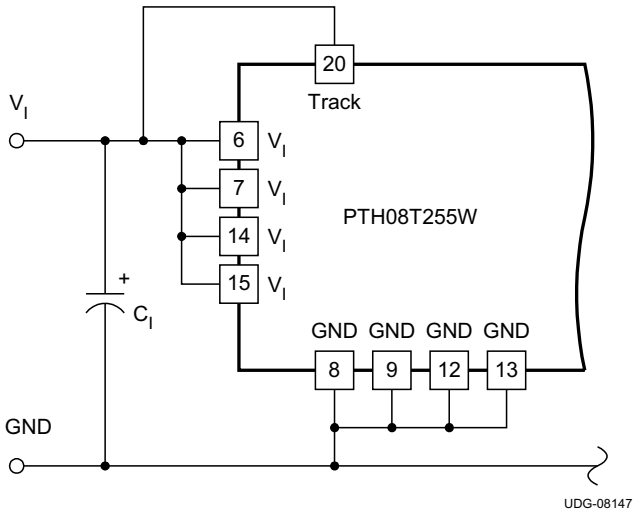


Figure 10. Defeating the Auto-Track Function

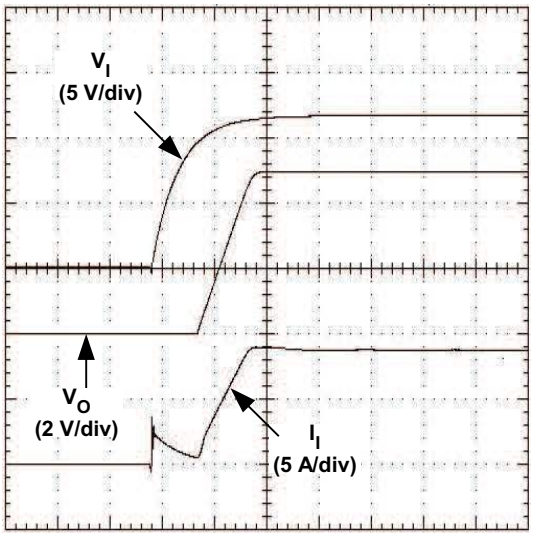


Figure 11. Power-Up Waveform

When the Track pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 10 ms–15 ms) before allowing the output voltage to rise.

The output then progressively rises to the module's setpoint voltage. Figure 11 shows the soft-start power-up characteristic of the PTH08T255W operating from a 12-V input bus and configured for a 5.0-V output. The waveforms were measured with a 25-A constant current load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 30 ms.

Differential Output Voltage Remote Sense

Differential remote sense improves the load regulation performance of the module by allowing it to compensate for any IR voltage drop between its output and the load in either the positive or return path. An IR drop is caused by the output current flowing through the small amount of pin and trace resistance. With the sense pins connected, the difference between the voltage measured directly between the V_O and GND pins, and that measured at the Sense pins, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3V.

If the remote sense feature is not used at the load, connect +Sense (pin 17) to V_O (pin11) and connect –Sense (pin 16) to the module GND (pin 13).

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

On/Off Inhibit

For applications requiring output voltage on/off control, the PTH08T255W incorporates an Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off. The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND.

Figure 12 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit input has its own internal pull-up. An external pull-up resistor should never be used with the inhibit pin. The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

When Q1 it turned on, low voltage is applied to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 20 ms. Figure 13 shows the typical rise in both the output voltage and input current, following the turn-off of Q1. The turn off of Q1 corresponds to the rise in the waveform, V_{INH}. The waveforms were measured with a 25-A constant current load.

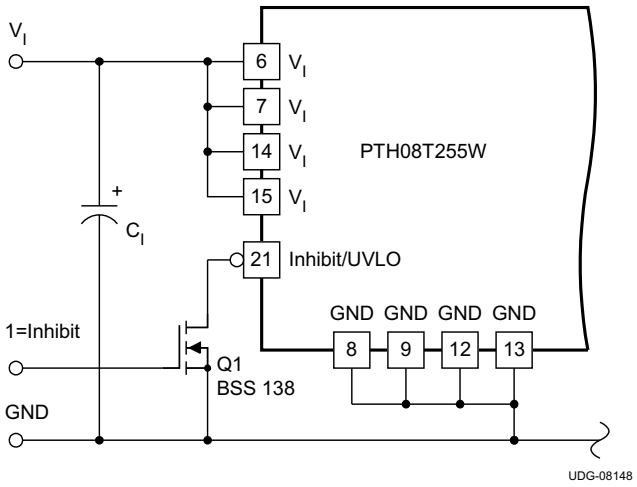


Figure 12. On/Off Inhibit Control Circuit

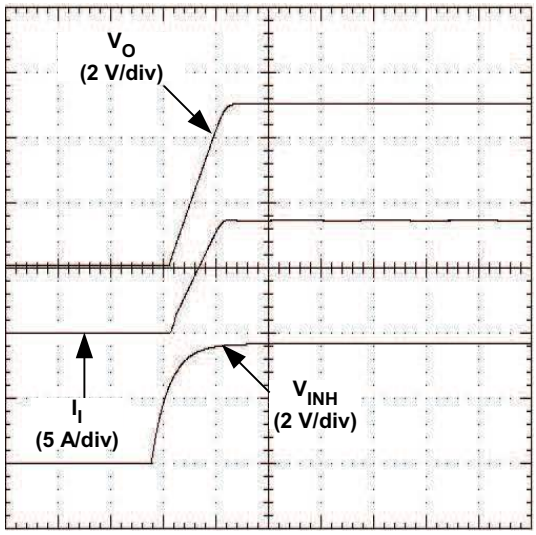


Figure 13. Power-Up Response from Inhibit Control

Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up. This is described as a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Overtemperature Protection (OTP)

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's Inhibit control is internally pulled low. This turns the output off. The output voltage drops as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the sensed temperature decreases by about 10°C below the trip point.

The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and reduces the long-term reliability of the module. Always operate the regulator within the specified safe operating area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Smart Sync

Smart Sync is a feature that allows multiple power modules to be synchronized to a common frequency. When not used, this pin must be connect to GND. Driving the Smart Sync pins with an external oscillator set to the desired frequency, synchronizes all connected modules to the selected frequency. The synchronization frequency can be higher or lower than the nominal switching frequency of the modules within the range of 240 kHz to 400 kHz.

Synchronizing modules powered from the same bus eliminates beat frequencies reflected back to the input supply, and also reduces EMI filtering requirements. Eliminating the low beat frequencies (usually<10kHz) allows the EMI filter to be designed to attenuate only the synchronization frequency. Power modules can also be synchronized out of phase to minimize ripple current and reduce input capacitance requirements.

The PTH08T255W requires that the external synchronization frequency be present before a valid input voltage is present or before release of the inhibit control.

Figure 14 shows a typical circuit with two modules synchronized 180° out of phase using a D flip-flop.

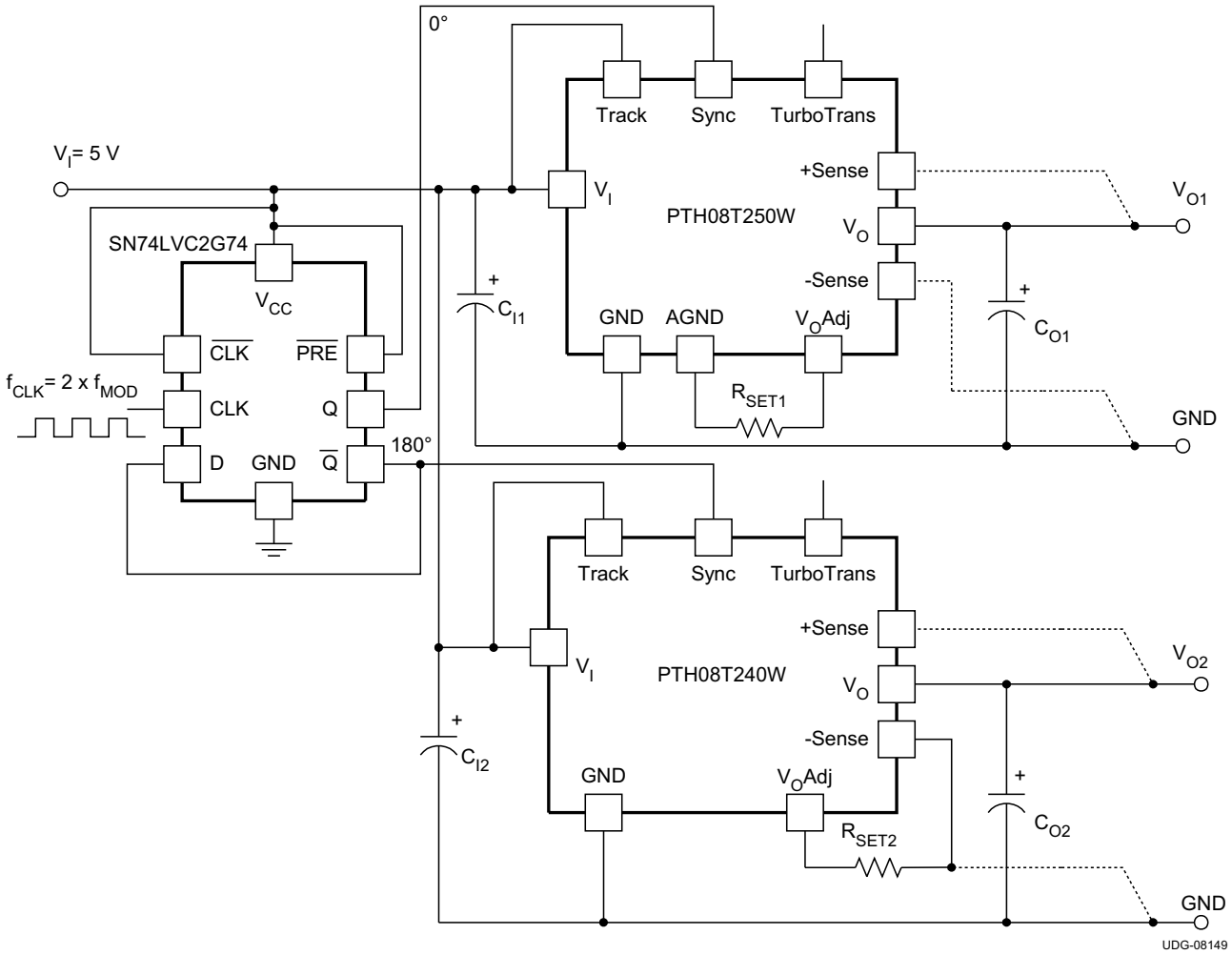


Figure 14. Typical Smart Sync Schematic

Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI ICs such as the TMS320™ DSP family, microprocessors, and ASICs.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin (1). This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module output remains at its set-point (2). As an example, if the *Track* pin of a 5.0-V regulator is at 4.0 V, the regulated output is 4.0 V. If the voltage at the *Track* pin rises to 6.0 V, the regulated output does not go higher than 5.0 V.

When under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit (3). For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

******NOTE*** When using the Auto-Track feature with the PTH08T255W, a 100 kΩ pull-up resistor to the input voltage is required. If the Auto-Track feature is not used, this pin must be directly connected to the input voltage.***

Typical Auto-Track Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common Track control signal. This can be an open-collector (or open-drain) device, such as a power-up reset voltage supervisor IC. See U3 in Figure 15.

To coordinate a power-up sequence, the Track control must first be pulled to ground potential. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 20 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization (4), enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, with a built-in time delay, is an ideal component for automatically controlling the Track inputs at power up.

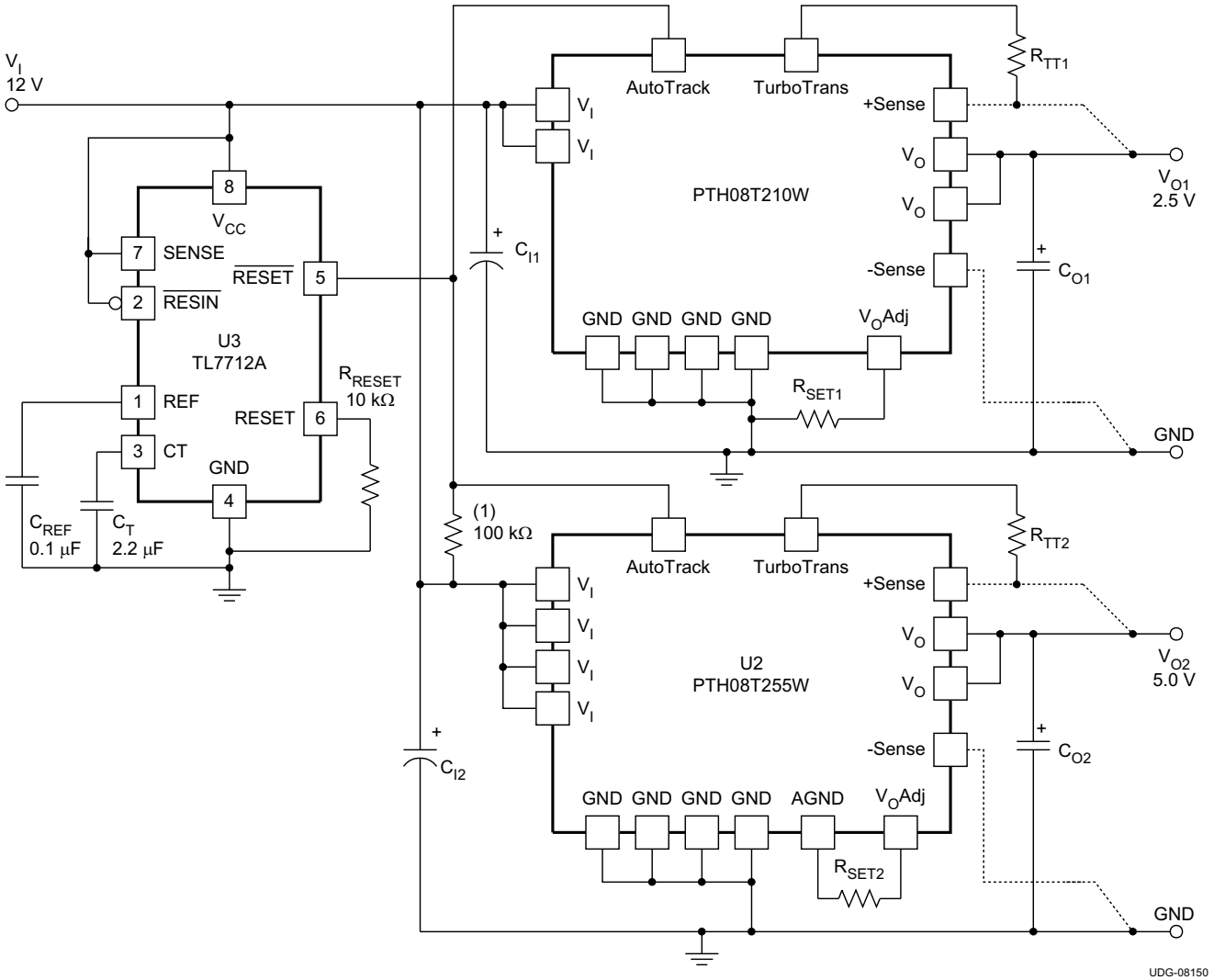
Figure 15 shows how the TL7712A supply voltage supervisor IC (U3) can be used to coordinate the sequenced power up of PTH08T255W modules. The output of the TL7712A supervisor becomes active above an input voltage of 3.6 V, enabling it to assert a ground signal to the common track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 28 ms after the input voltage has risen above U3's voltage threshold, which is 10.95 V. The 28-ms time period is controlled by the capacitor C_T. The value of 2.2 µF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the track control voltage is allowed to rise. When U3 removes the ground signal, the track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

Figure 16 shows the output voltage waveforms after input voltage is applied to the circuit. The waveforms, V_O1 and V_O2, represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. V_{TRK}, V_O1, and V_O2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is re-applied to the common track control. This pulls the track inputs to zero volts, forcing the output of each module to follow, as shown in Figure 17. Power down is normally complete before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that an input voltage is no longer present, their outputs can no longer follow the voltage applied at their track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the Auto-Track slew rate capability.

Notes on Use of Auto-Track™

1. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage V_I.
4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 20 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises according to its softstart rate after input power has been applied.
6. The Auto-Track pin should never be used to regulate the module's output voltage for long-term, steady-state operation.



(1) **When using Auto-Track with the PTH08T255W, a 100-kΩ resistor must be placed between the V_I and AutoTrack pins.**

Figure 15. Sequenced Power Up and Power Down Using Auto-Track

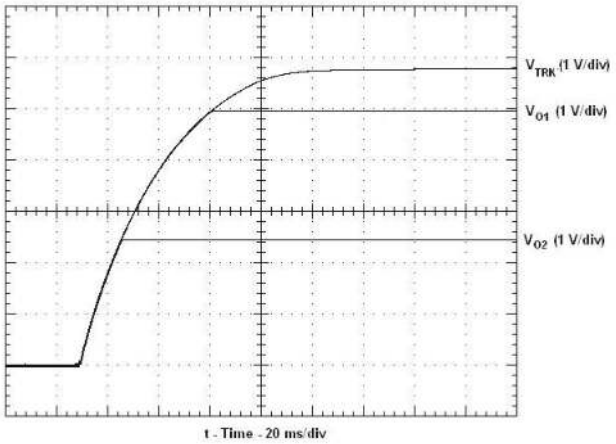


Figure 16. Simultaneous Power Up With Auto-Track Control

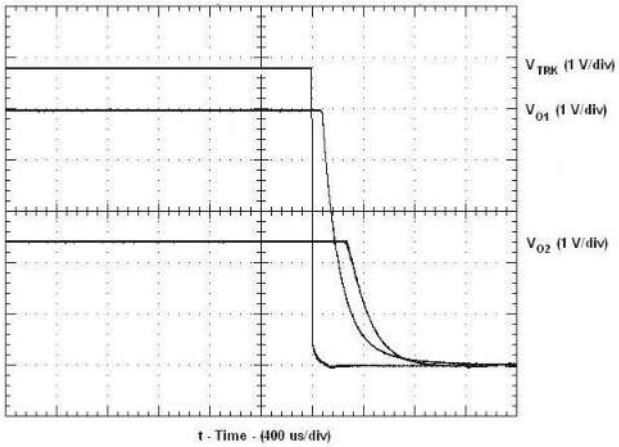


Figure 17. Simultaneous Power Down With Auto-Track Control

ADJUSTING THE UNDERVOLTAGE LOCKOUT (UVLO)

The PTH08T255W power modules incorporate an input undervoltage lockout (UVLO). The UVLO feature prevents the operation of the module until there is sufficient input voltage to produce a valid output voltage. This enables the module to provide a clean, monotonic powerup for the load circuit, and also limits the magnitude of current drawn from the regulator's input source during the power-up sequence.

The UVLO characteristic is defined by the ON threshold (V_{THD}) voltage. Below the *ON* threshold, the Inhibit control is overridden, and the module does not produce an output. The hysteresis voltage, which is the difference between the *ON* and *OFF* threshold voltages, is set at 500 mV. The hysteresis prevents start-up oscillations, which can occur if the input voltage droops slightly when the module begins drawing current from the input source.

The UVLO feature of the PTH08T255W module allows for limited adjustment of the *ON* threshold voltage. The adjustment is made via the *Inhbit/UVLO Prog* control pin (pin 11) using a single resistor (see Figure 18). When pin 11 is left open circuit, the *ON* threshold voltage is internally set to its default value, which is 7.2 volts. The *ON* threshold might need to be raised if the module is powered from a tightly regulated 12-V bus. Adjusting the threshold prevents the module from operating if the input bus fails to completely rise to its specified regulation voltage.

Equation 4 determines the value of R_{UVLO} required to adjust V_{THD} to a new value. The default value is 7.2 V, and it may only be adjusted to a higher value.

$$R_{UVLO} = \frac{250}{V_{THD} - 7.3} \ (k\Omega) \tag{4}$$

Table 6 lists the standard resistor values for R_{UVLO} for different values of the on-threshold (V_{THD}) voltage.

Table 6. Standard R_{UVLO} values for Various V_{THD} values

V_{THD} (V)	8.0	8.5	9.0	9.5	10.0	10.5	11.0
R_{UVLO} (kΩ)	357	210	147	113	93.1	78.7	68.1

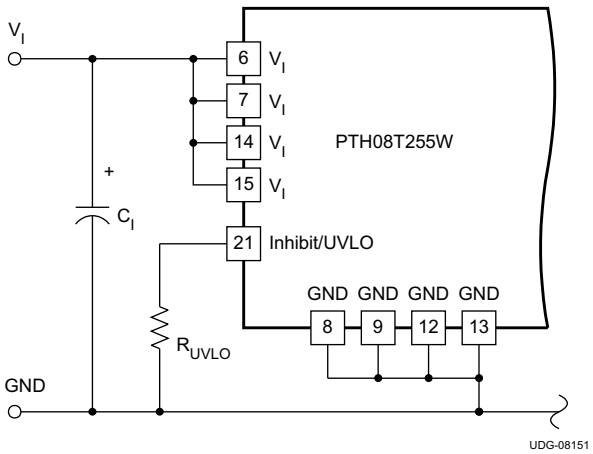


Figure 18. Undervoltage Lockout Adjustment Resistor Placement

CURRENT SHARING

The PTH08T255W module is capable of being configured in parallel with another PTH08T255W module to share load current. To parallel the two modules, it is necessary to configure one module as the Master and one module as the Slave. To configure a module as the Master, connect the CONFIG pin (pin 1) to GND. The CONFIG pin of the Slave must be connected to V_I. In order to share current, pins 2 thru 5 of both the Master and Slave must be connected between the two modules. See Figure 22 for the recommended layout of pins 2 thru 5. The module that is configured as the MASTER is used to control all of the functions of the two modules including Inhibit ON/OFF control, AutoTrack sequencing, TurboTrans, SmartSync, +/- Remote Sense, and Output Voltage Adjust. See the current sharing diagram in Figure 19 for connections. The MASTER and the SLAVE must be powered from the same input voltage supply.

See Figure 19 and Table 7 for a diagram and connection description of each pin when two PTH08T255W modules are being used in a MASTER/SLAVE configuration.

CURRENT SHARING DIAGRAM

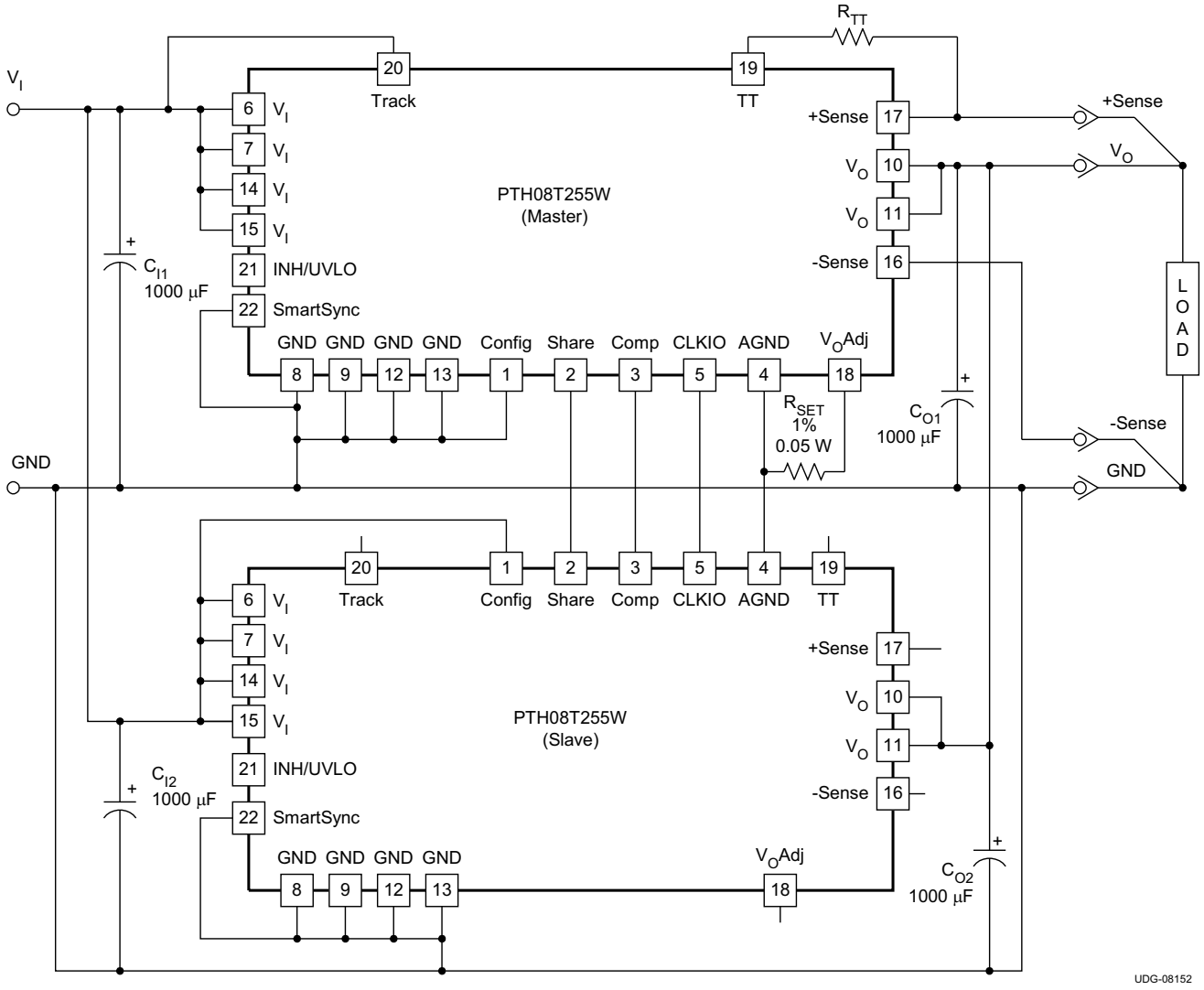


Figure 19. Typical Current Sharing Diagram

Table 7. Required Connections for Current Sharing(1)

TERMINAL		MASTER	SLAVE
NAME	NO.		
V_I	6,7,14,15	Connect to the Input Bus.	Connect to the Input Bus.
V_O	10,11	Connect to the Output Bus.	Connect to the Output Bus.
GND	8,9,12,13	Connect to Common Power GND.	Connect to Common Power GND.
Inhibit and UVLO	21	Use for Inhibit control & UVLO adjustments. If unused leave open-circuit.	No Connection. Leave open-circuit.
V_o Adjust	18	Use to set the output voltage. Connect R_{SET} resistor between this pin and AGND (pin 4).	No Connection. Leave open-circuit.
+Sense	17	Connect to the output voltage either at the load or at the module (pin 11).	No Connection. Leave open-circuit.
–Sense	16	Connect to the output GND either at the load or at the module (pin 13).	No Connection. Leave open-circuit.
Track	20	Connect to Track control or to V_I (pin 15).	No Connection. Leave open-circuit.
TurboTrans™	19	Connect TurboTrans resistor, R_{TT}, between this pin and +Sense (pin 17).	No Connection. Leave open-circuit.
SmartSync	22	Connect to an external clock. If unused connect to GND.	Connect to Common Power GND.
CONFIG	1	Connect to GND. (2)	Connect to the Input Bus.
Share	2	Connect to pin 2 of Slave. (2)	Connect to pin 2 of Master.
Comp	3	Connect to pin 3 of Slave. (2)	Connect to pin 3 of Master.
AGND	4	Connect to pin 4 of Slave. (3)	Connect to pin 4 of Master.
CLKIO	5	Connect to pin 5 of Slave. (2)	Connect to pin 5 of Master.

(1) For more details on the pin descriptions, please refer to the 'Terminal Functions' described in Table 1
(2) See Layer A in Figure 22 for recommended layout
(3) See Layer B in Figure 22 for recommended layout

Current Sharing and TurboTrans™

When using TurboTrans while paralleling two modules, the TurboTrans resistor, R_{TT}, must be connected from the TurboTrans pin (pin 19) of the Master module to the +Sense pin (pin 17) of the Master module. When paralleling modules the procedure to calculate the proper value of output capacitance and R_{TT} is similar to that explained in the TurboTrans Selection section, however the values must be calculated for a single module. Therefore, the total output current load step must be halved before determining the required output capacitance and the R_{TT} value as explained in the TurboTrans Selection section. The value of output capacitance calculated is the minimum required output capacitance per module and the value of R_{TT} must be calculated using this value of output capacitance. The TurboTrans pin of the Slave module must be left open.

As an example, let's look at a 12-V application requiring a 40 mV deviation during a 20 A load transient. A majority of 470 µF, 10 mΩ output capacitors are used. Use the 12 V, Type B capacitor chart, Figure 7. First, halving the load transient gives 10 A. Dividing 40 mV by 10 A gives 4 mV/A transient voltage deviation per amp of transient load step. Select 4 mV/A on the Y-axis and read across to the 'With TurboTrans' plot. Following this point down to the X-axis gives us a minimum required output capacitance of approximately 1800 µF. This is the minimum required output capacitance per module. Hence, the total minimum output capacitance would be 2 × 1800 µF = 3600 µF. The required R_{TT} resistor value for 1800 µF can then be calculated or selected from Table 4. The required R_{TT} resistor is approximately 26.7 kΩ.

Current Sharing Thermal Derating Curves

The temperature derating curves in Figure 20 and Figure 21 represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to two PTH08T255W modules soldered directly to a 100 mm × 200 mm double-sided PCB with 2 oz. copper and the direction of airflow from pins 10 to pins 22. For surface mount packages (AS and AZ suffix), multiple vias must be utilized. Please refer to the mechanical specification for more information.

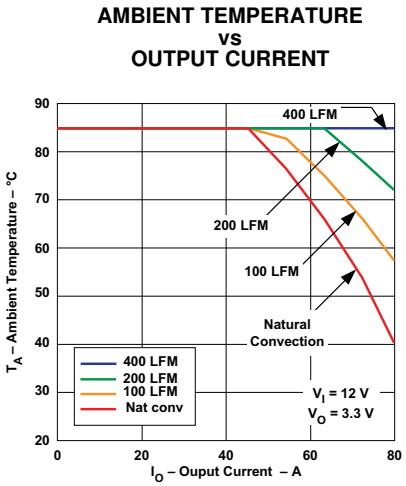


Figure 20.

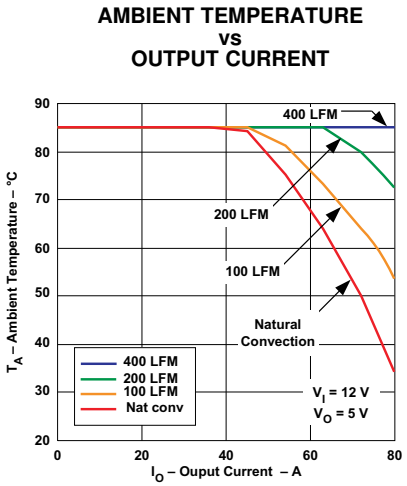


Figure 21.

Current Sharing Layout

In current sharing applications the V_I pins of both modules must be connected to the same input bus. The V_O pins of both modules are connected together to power the load. The GND pins of both modules are connected via the GND plane. Four other inter-connection pins are connected between the modules. Figure 22 shows the required layout of the inter-connection pins for two modules configured to share current. Notice that the Share (pin 2) connection is routed between the Comp (pin 3) and CLKIO (pin 5) connections. AGND (pin 4) should be connected as a thicker trace on an adjacent layer, running parallel to pins 2, 3 and 5. AGND must not be connected to the GND plane.

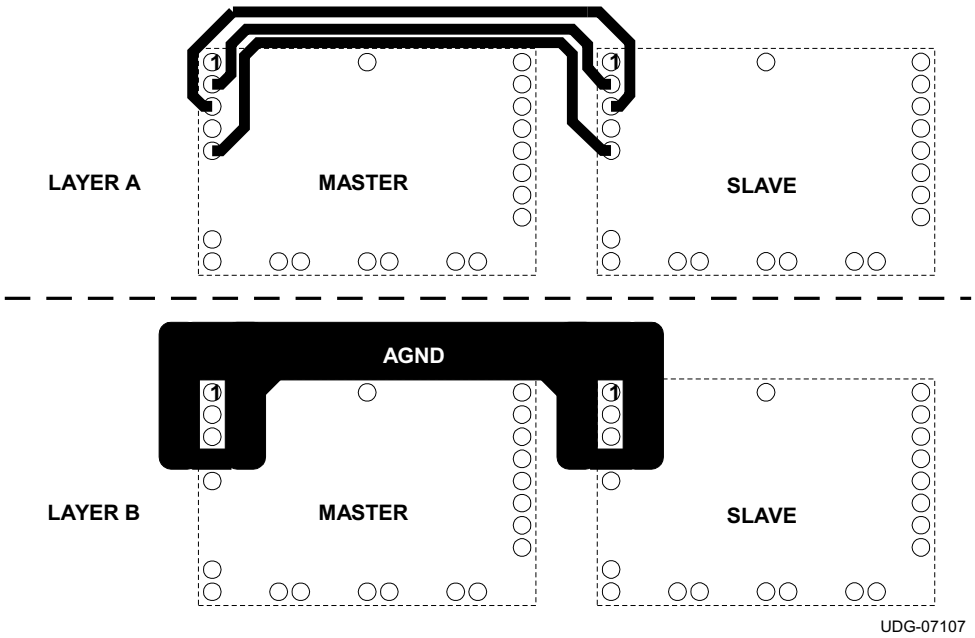


Figure 22. Recommended Layout of Inter-Connection Pins Between Two Current Sharing Modules

Prebias Startup Capability

A prebias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, these types of modules can sink as well as source output current.

The PTH family of power modules incorporate synchronous rectifiers, but does not sink current during startup(1), or whenever the Inhibit pin is held low. However, to ensure satisfactory operation of this function, certain conditions must be maintained(2). Figure 24 shows an application demonstrating the prebias startup capability. The startup waveforms are shown in Figure 23. Note that the output current (I_O) is negligible until the output voltage rises above the voltage backfed through the intrinsic diodes.

The prebias start-up feature is not compatible with Auto-Track. When the module is under Auto-Track control, it sinks current if the output voltage is below that of a back-feeding source. To ensure a pre-bias hold-off one of two approaches must be followed when input power is applied to the module. The Auto-Track function must either be disabled(3), or the module's output held off (for at least 50 ms) using the Inhibit pin. Either approach ensures that the Track pin voltage is above the set-point voltage at start up.

1. Startup includes the short delay (approximately 10 ms) prior to the output voltage rising, followed by the rise of the output voltage under the module's internal soft-start control. Startup is complete when the output voltage has risen to either the set-point voltage or the voltage at the Track pin, whichever is lowest.
2. To ensure that the regulator does not sink current when power is first applied (even with a ground signal applied to the Inhibit control pin), the input voltage must always be greater than the output voltage *throughout* the power-up and power-down sequence.
3. The Auto-Track function can be disabled at power up by immediately applying a voltage to the module's Track pin that is greater than its set-point voltage. This can be easily accomplished by connecting the Track pin to V_I.

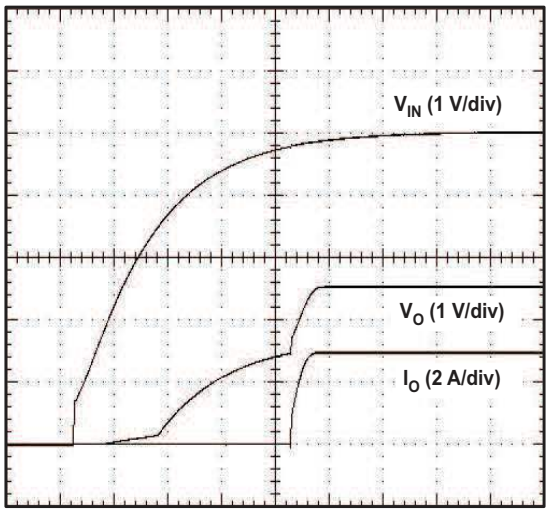


Figure 23. Prebias Startup Waveforms

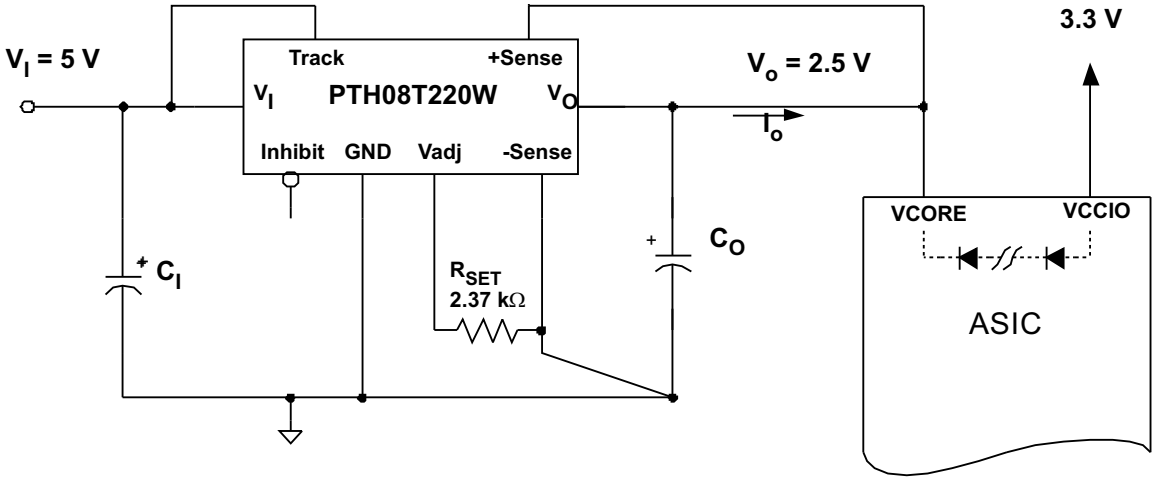
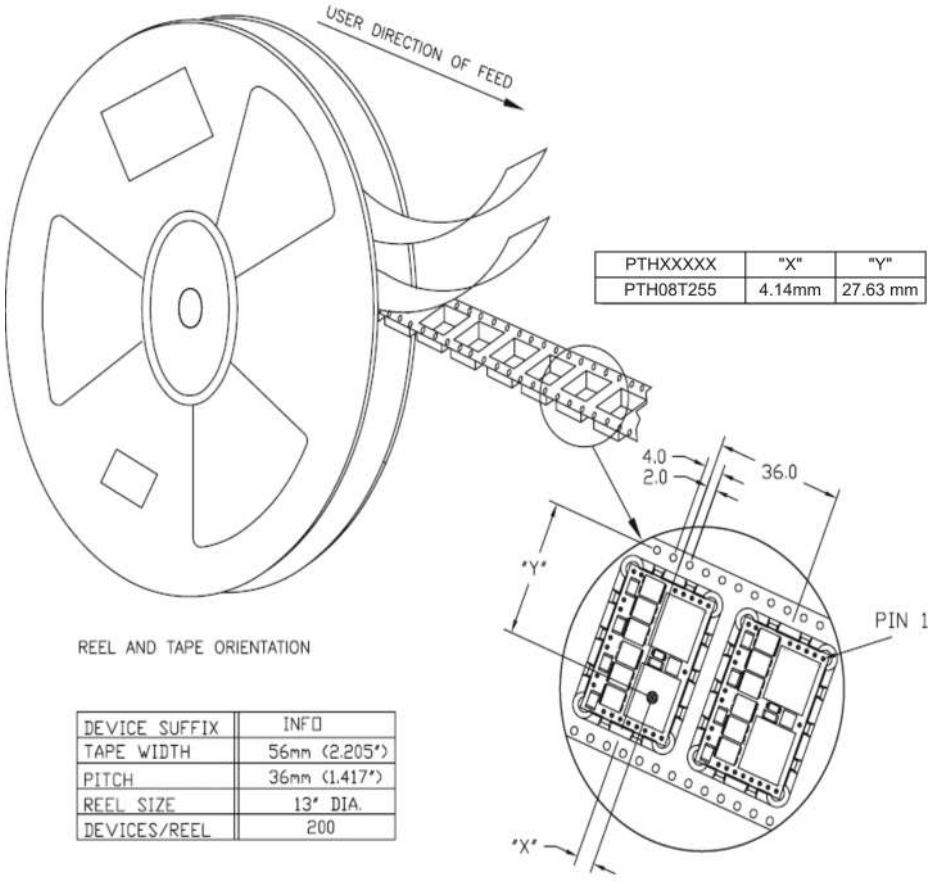
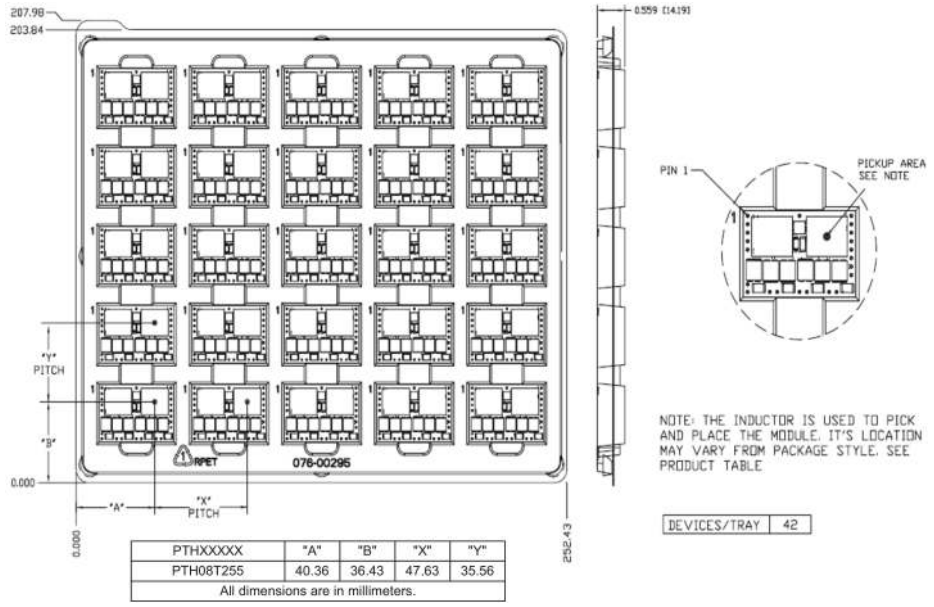


Figure 24. Application Circuit Demonstrating Prebias Startup

Tape & Reel and Tray Drawings





PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTH08T255WAD	ACTIVE	Through-Hole Module	ECT	22	25	RoHS Exempt & Green	SN	N / A for Pkg Type	-40 to 85		Samples
PTH08T255WAS	ACTIVE	Surface Mount Module	ECU	22	25	Non-RoHS & Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH08T255WAST	ACTIVE	Surface Mount Module	ECU	22	225	Non-RoHS & Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH08T255WAZ	ACTIVE	Surface Mount Module	BCU	22	25	RoHS Exempt & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH08T255WAZT	ACTIVE	Surface Mount Module	BCU	22	225	RoHS Exempt & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

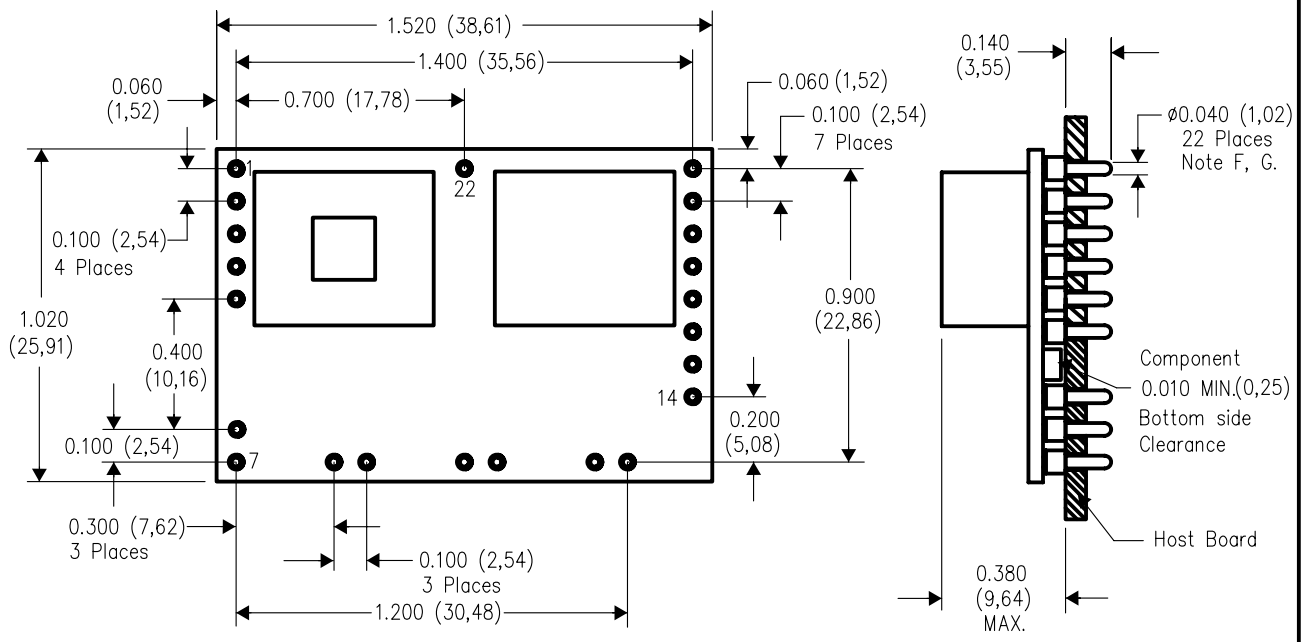
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

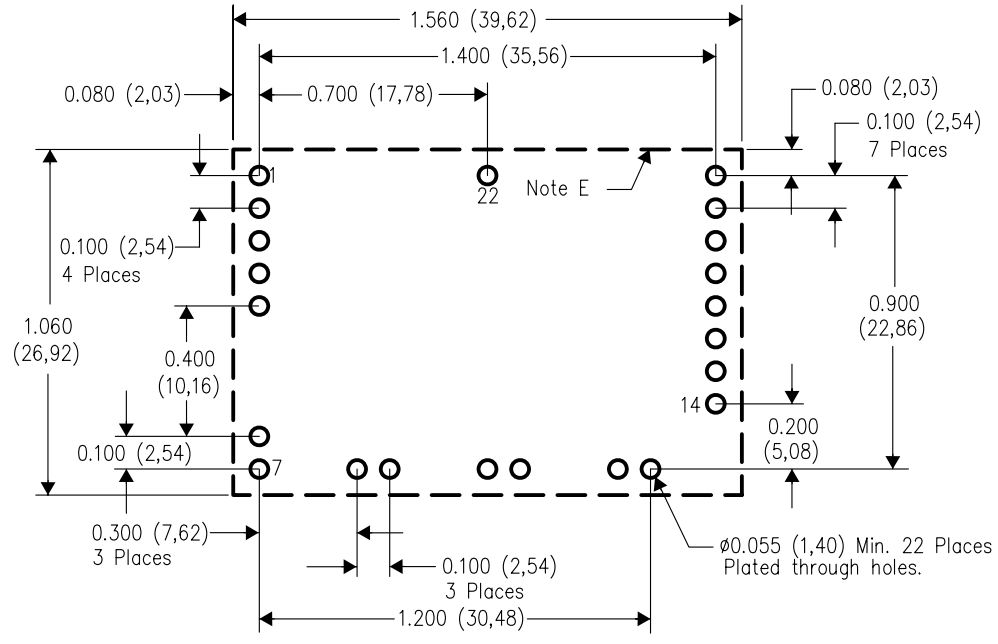
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

ECT (R–PDSS–T22) DOUBLE SIDED MODULE

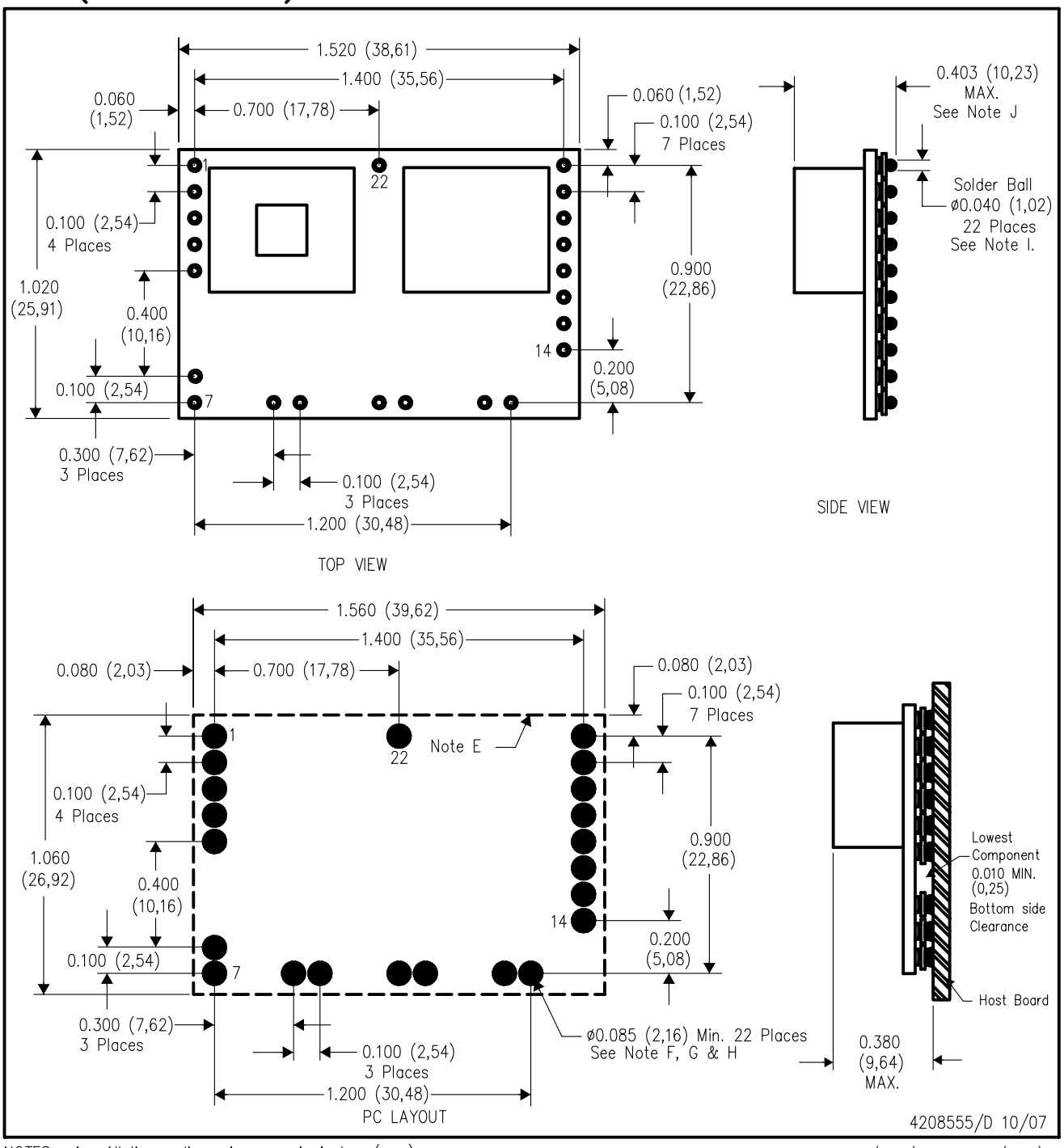




4208554/C 10/07

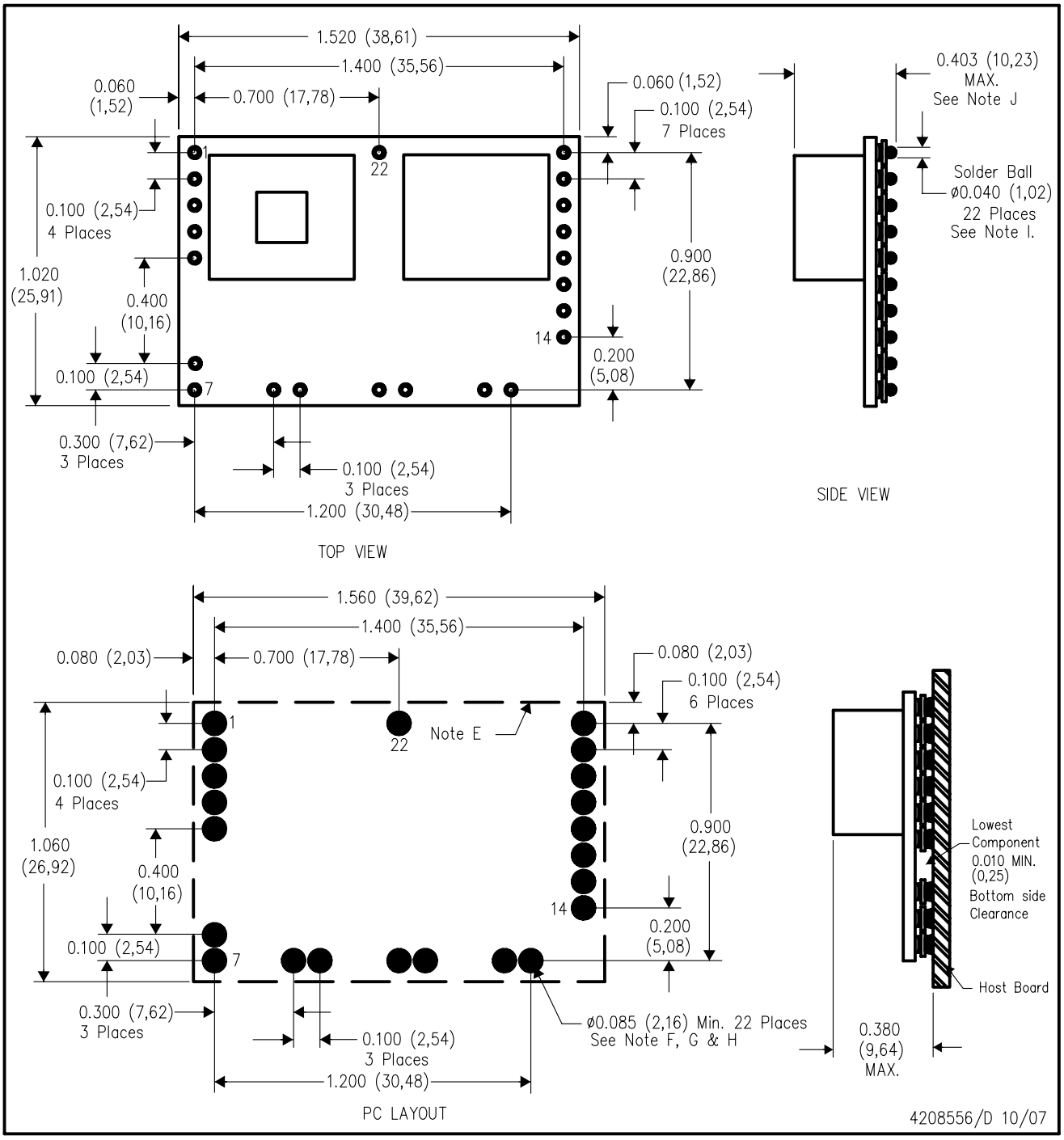
NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

ECU (R–PDSS–B22) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

BCU (R–PDSS–B22) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. This is a lead–free solder ball design.
Finish: Tin (100%) over Nickel plate
Solder ball: 96.5 Sn/3.0 Ag/0.5 Cu
J. Dimension prior to reflow solder.

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