LVHSTL TO CMOS CLOCK DIVIDER

ICS558A-02

Description

The ICS558A-02 accepts a high-speed LVHSTL input and provides four CMOS low skew outputs from a selectable internal divider (divide by 3, divide by 4). The four outputs are split into two banks of two outputs. Each bank has a separate output enable to tri-state the output buffers.

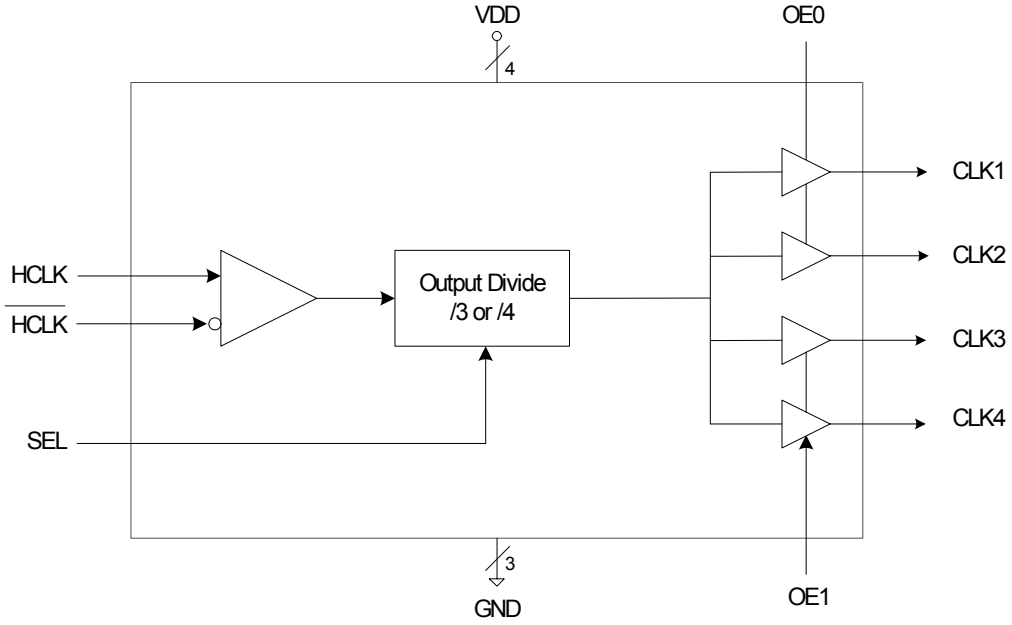
The ICS558A-02 is a member of the IDT Clock Blocks™ family of clock generation, synchronization, and distribution devices.

Features

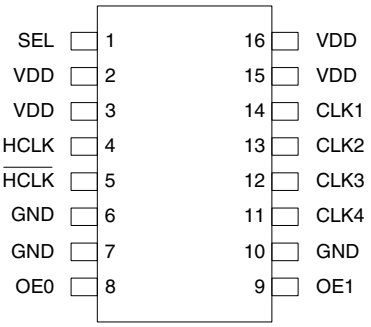
- 16-pin TSSOP package
- LVHSTL inputs
- Accepts up to 250 MHz input frequency
- Four low skew (<250 ps) outputs
- Selectable internal divider of 3 or 4
- Operating voltage of 3.3 V
- Available in a lead-free, RoHS compliant package

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



16 Pin 173 Mil (0.65mm) TSSOP

Tri-State Table

OE1	OE0	CLK 1, CLK 2	CLK 3, CLK 4
0	0	Tri-state	Tri-state
0	1	Clock ON	Tri-state
1	0	Tri-state	Clock ON
1	1	Clock ON	Clock ON

Output Divide Selection

SEL	Output Divide
0	/3
1	/4

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	SEL	Input	Select pin for output divider. See table above. Internal pull-up to VDD.
2	VDD	Power	Connect to +3.3 V.
3	VDD	Power	Connect to +3.3 V.
4	HCLK	Input	Differential LVHSTL input (true input).
5	$\overline{\text{HCLK}}$	Input	Differential LVHSTL input (complimentary input).
6	GND	Power	Connect to ground.
7	GND	Power	Connect to ground.
8	OE0	Input	Output enable for CLK1 and CLK2. See table above. Internal pull-up to VDD.
9	OE1	Input	Output enable for CLK3 and CLK4. See table above. Internal pull-up to VDD.
10	GND	Power	Connect to ground.
11	CLK4	Output	Low skew clock output.
12	CLK3	Output	Low skew clock output.
13	CLK2	Output	Low skew clock output.
14	CLK1	Output	Low skew clock output.
15	VDD	Power	Connect to +3.3 V.
16	VDD	Power	Connect to +3.3 V.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS558A-02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage	4.6 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70 °C
Storage Temperature	-65 to +150 °C
Junction Temperature	125 °C
Soldering Temperature	260 °C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.5	V

DC Electrical Characteristics

VDD=3.3 V ±5%, Ambient temperature 0 to +70° C, unless stated otherwise stated.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135	3.3	3.465	V
Operating Supply Current	IDD	No load, 100 MHz		60		mA
Input High Voltage	V_{IH}	OE pins	VDD-0.5		VDD	V
Input Low Voltage	V_{IL}	OE pins			0.5	V
Input High Voltage	V_{IH}	HCLK	Vx + 0.1		1.2	V
Input Low Voltage	V_{IL}	HCLK	-0.3		Vx - 0.1	V
Peak to Peak Input Voltage		HCLK	0.3		1.0	V
HCLK Input Leakage Current	I_{IL}		-20		20	µA
Input Common Mode Voltage	Vx	Input Common Mode	0.68		0.90	V
Output High Voltage	V_{OH}	I_{OH} = -14.5 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 9.4 mA			0.4	V
Nominal Output Impedance	Z_O			20		Ω
Internal Pull-up Resistor	R_{PU}			250		kΩ
Input Capacitance	C_{IN}			7		pF

AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise stated.

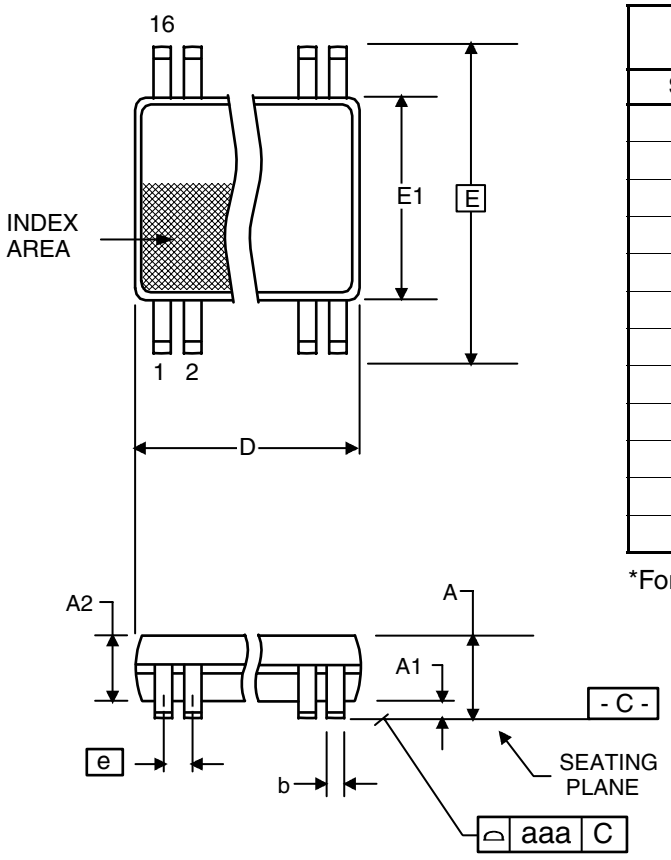
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		250	MHz
Output Rise Time	t_{OR}	0.4 to 2.4 V, C_L=30 pF	0.5	1.1	2.0	ns
Output Fall Time	t_{OF}	2.4 to 0.4 V, C_L=30 pF	0.5	1.0	2.0	ns
Skew (between any two output clocks)		30 pF load		0	250	ps
Propagation Delay				9	12	ns
Output Clock Duty Cycle		at VDD/2, C_L=30 pF	45	50	55	%

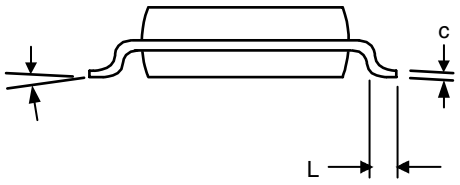
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153





	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimension in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
558AG-02*	558AG-02	Tubes	16-pin TSSOP	0 to 70° C
558AG-02LN	558AG02LN	Tubes	16-pin TSSOP	0 to 70° C
558AG-02T*	558AG-02	Tape and Reel	16-pin TSSOP	0 to 70° C
558AG-02LNT	558AG02LT	Tape and Reel	16-pin TSSOP	0 to 70° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

*LN denotes a lead-free, RoHS compliant package.

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