FAIRCHILD SEMICONDUCTOR

May 2007

DM74ALS564A
Octal D-Type Edge-Triggered Flip-Flop with

Features

- Switching specifications at 50pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer-type outputs drive bus lines directly

General Description

These 8-bit registers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the DM74ALS564A are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

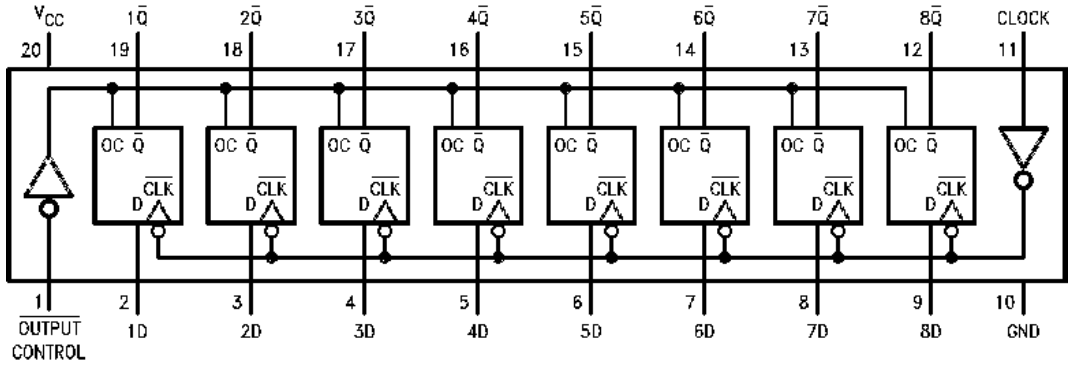
The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

Ordering Information

Order Number	Package Number	Package Description
DM74ALS564AWM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering number.

Connection Diagram



Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = LOW State

H = HIGH State

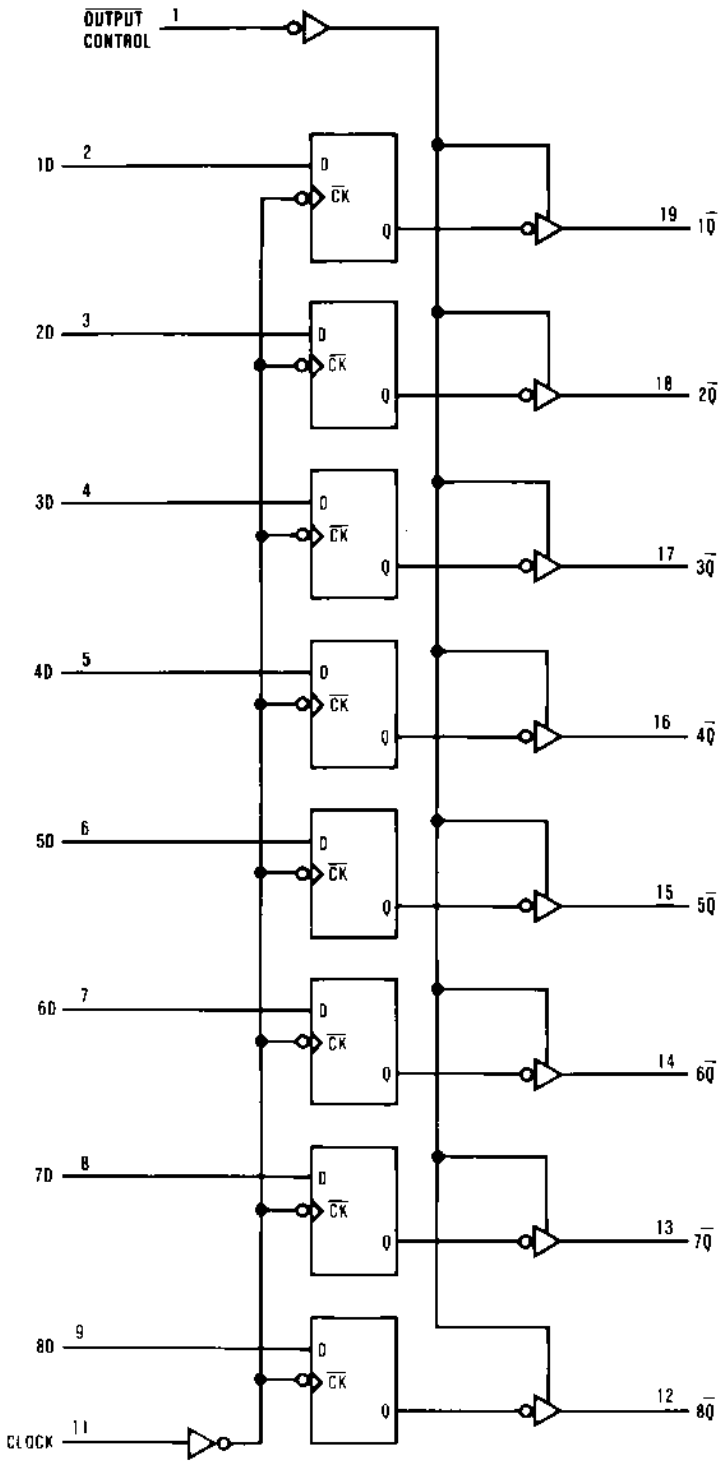
X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Logic Diagram



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	7V
V_I	Input Voltage	7V
	Voltage Applied to Disabled Output	5.5V
T_A	Operating Free Air Temperature Range	0°C to +70°C
T_{STG}	Storage Temperature Range	–65°C to +150°C
θ_{JA}	Typical Thermal Resistance	75.0°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Nom.	Max.	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				–2.6	mA
I_{OL}	LOW Level Output Current				24	mA
f_{CLOCK}	Clock Frequency		0		30	MHz
t_W	Width of Clock Pulse	HIGH	14			ns
		LOW	14			ns
t_{SU}	Data Setup Time(2)		15↑			ns
t_H	Data Hold Time(2)		0↑			ns
T_A	Free Air Operating Temperature		0		70	°C

Notes:

1. This product meets application requirements of 500 temperature cycles from –65°C to +150°C.
2. The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = –18 mA				–1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL}Max., I_{OH} = Max.		2.4	3.2		V
		V_{CC} = 4.5V to 5.5V, I_{OH} = –400µA		V_{CC} – 2			
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4	V
			I_{OL} = 24mA		0.35	0.5	V
I_I	Input Current @ Maximum Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				–0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		–30		–112	mA
I_{OZH}	OFF-State Output Current HIGH Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				20	µA
I_{OZL}	OFF-State Output Current LOW Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				–20	µA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs OPEN	Outputs HIGH		10	18	mA
			Outputs LOW		15	24	
			Outputs Disabled		16	30	

Switching Characteristics

Over recommended operating free air temperature range.

Symbol	Parameter	Conditions	From	To	Min.	Max.	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50pF			30		MHz
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output		Clock	Any $\overline{Q}$	4	14	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		Clock	Any $\overline{Q}$	4	14	ns
t_{PZH}	Output Enable Time to HIGH Level Output		Output Control	Any $\overline{Q}$	4	18	ns
t_{PZL}	Output Enable Time to LOW Level Output		Output Control	Any $\overline{Q}$	4	18	ns
t_{PHZ}	Output Disable Time from HIGH Level Output		Output Control	Any $\overline{Q}$	2	10	ns
t_{PLZ}	Output Disable Time from LOW Level Output		Output Control	Any $\overline{Q}$	3	15	ns

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

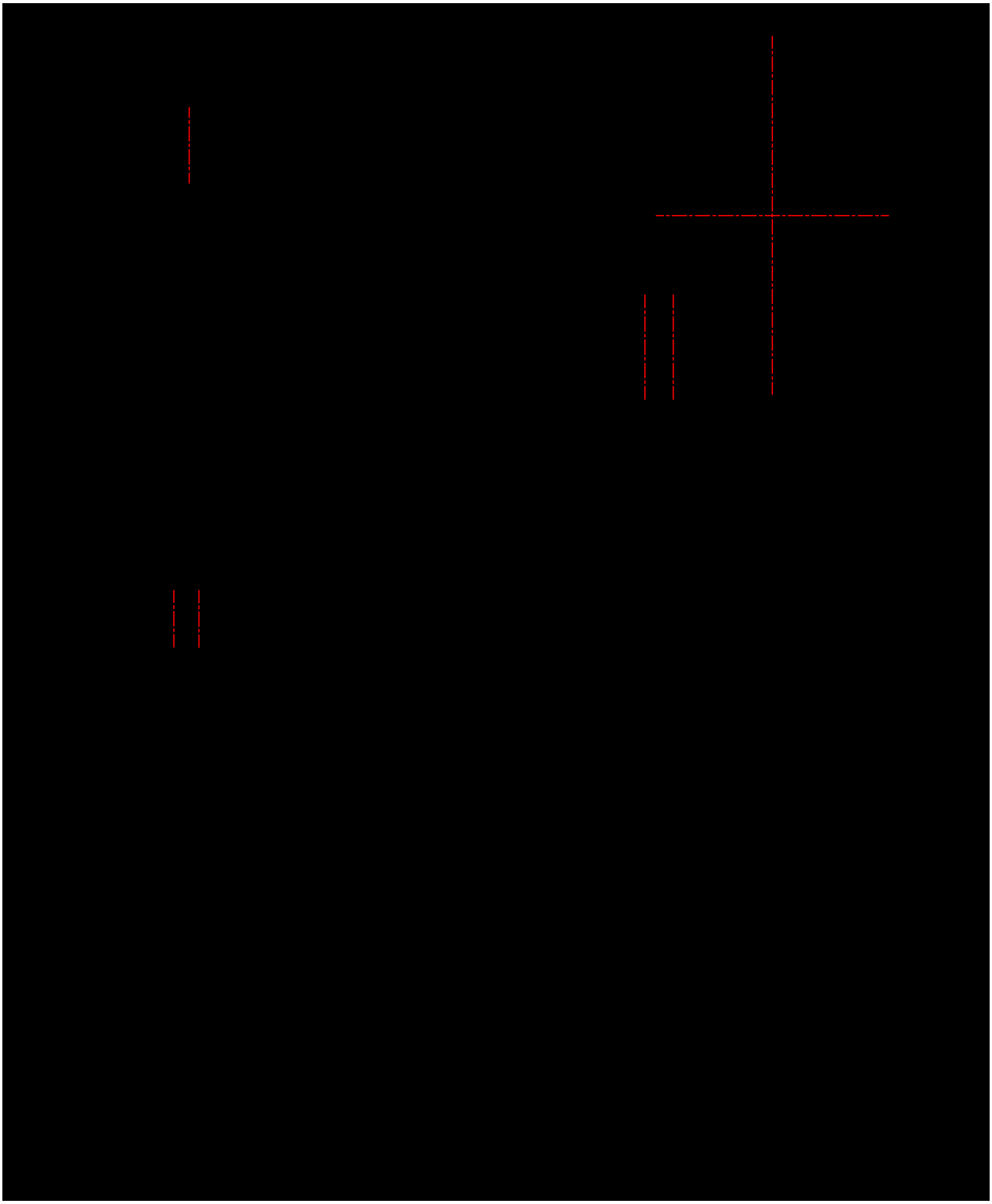


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B