

CMOS Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers with Shutdown

AD8591/AD8592/AD8594

FEATURES

Single-supply operation: 2.5 V to 6 V High output current: ±250 mA Extremely low shutdown supply current: 100 nA Low supply current: 750 µA/Amp Wide bandwidth: 3 MHz Slew rate: 5 V/µs No phase reversal Very low input bias current High impedance outputs when in shutdown mode Unity-gain stable

APPLICATIONS

Mobile communication handset audio PC audio PCMCIA/modem line driving Battery-powered instrumentation Data acquisition ASIC input or output amplifiers LCD display reference level drivers

GENERAL DESCRIPTION

The AD8591, AD8592, and AD8594 are single, dual, and quad rail-to-rail, input and output single-supply amplifiers featuring 250 mA output drive current and a power saving shutdown mode. The AD8592 includes an independent shutdown function for each amplifier. When both amplifiers are in shutdown mode, the total supply current is reduced to less than 1 µA. The AD8591 and AD8594 include a single master shutdown function that reduces the total supply current to less than 1 µA. All amplifier outputs are in a high impedance state when in shutdown mode.

These amplifiers have very low input bias currents, making them suitable for integrators and diode amplification. Outputs are stable with virtually any capacitive load. Supply current is less than 750 µA per amplifier in active mode.

Applications for these amplifiers include audio amplification for portable computers, portable phone headsets, sound ports, sound cards, and set-top boxes. The AD859x family is capable of driving heavy capacitive loads, such as LCD panel reference levels.

The ability to swing rail to rail at both the input and output enables designers to buffer CMOS DACs, ASICs, and other wide output swing devices in single-supply systems.

Rev. B

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PIN CONFIGURATIONS

The AD8591, AD8592, and AD8594 are specified over the industrial temperature range (−40°C to +85°C). The AD8591, single, is available in the tiny 6-lead SOT-23 package. The AD8592, dual, is available in the 10-lead surface-mount MSOP package. The AD8594, quad, is available in 16-lead narrow SOIC and 16-lead TSSOP packages.

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ELECTRICAL CHARACTERISTICS

 $\rm V_S$ = 2.7 V, $\rm V_{\rm CM}$ = 1.35 V, $\rm T_A$ = 25°C, unless otherwise noted.

 V_s = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 2.

ABSOLUTE MAXIMUM RATINGS

 1 For supplies less than \pm 5 V, the differential input voltage is limited to the supplies.
 ESD CAUTION

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. THERMAL RESISTANCE

 θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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THEORY OF OPERATION

The AD859x amplifiers are CMOS, high output drive, rail-torail input and output single-supply amplifiers designed for low cost and high output current drive. The parts include a power saving shutdown function that makes the AD8591/AD8592/ AD8594 op amps ideal for portable multimedia and telecommunications applications.

[Figure 33](#page-10-1) shows the simplified schematic for the AD8591/AD8592/ AD8594 amplifiers. Two input differential pairs, consisting of an n-channel pair (M1, M2) and a p-channel pair (M3, M4), provide a rail-to-rail input common-mode range. The outputs of the input differential pairs are combined in a compound foldedcascode stage that drives the input to a second differential pair gain stage. The outputs of the second gain stage provide the gate voltage drive to the rail-to-rail output stage.

The rail-to-rail output stage consists of M15 and M16, which are configured in a complementary common source configuration. As with any rail-to-rail output amplifier, the gain of the output stage, and thus the open-loop gain of the amplifier, is dependent on the load resistance. In addition, the maximum output voltage swing is directly proportional to the load current. The difference between the maximum output voltage to the supply rails, known as the dropout voltage, is determined by the on-channel resistance of the AD8591/AD8592/AD8594 output transistors. The output dropout voltage is given in [Figure 5](#page-5-1) and [Figure 6](#page-5-2).

INPUT VOLTAGE PROTECTION

Although not shown in the simplified schematic, ESD protection diodes are connected from each input to each power supply rail. These diodes are normally reverse-biased, but turn on if either input voltage exceeds either supply rail by more than 0.6 V. If this condition occurs, limit the input current to less than ±5 mA. This is done by placing a resistor in series with the input(s). The minimum resistor value should be

$$
R_{IN} \ge \frac{V_{IN,MAX}}{5 \text{ mA}}
$$
 (1)

OUTPUT PHASE REVERSAL

The AD8591/AD8592/AD8594 are immune to output voltage phase reversal with an input voltage within the supply voltages of the device. However, if either of the inputs of the device exceeds 0.6 V outside of the supply rails, the output could exhibit phase reversal. This is due to the ESD protection diodes becoming forward-biased, thus causing the polarity of the input terminals of the device to switch.

The technique recommended in the [Input Voltage Protection](#page-10-2) section should be applied in applications where the possibility of input voltages exceeding the supply voltages exists.

OUTPUT SHORT-CIRCUIT PROTECTION

To achieve high output current drive and rail-to-rail performance, the outputs of the AD859x family do not have internal shortcircuit protection circuitry. Although these amplifiers are designed to sink or source as much as 250 mA of output current, shorting the output directly to the positive supply could damage or destroy the device. To protect the output stage, limit the maximum output current to ±250 mA.

By placing a resistor in series with the output of the amplifier, as shown in [Figure 34](#page-10-3), the output current can be limited. The minimum value for R_X is

$$
R_X \ge \frac{V_{SY}}{250 \text{ mA}}
$$
 (2)

For a 5 V single-supply application, R_X should be at least 20 Ω . Because R_X is inside the feedback loop, V_{OUT} is not affected. The trade-off in using R_X is a slight reduction in output voltage swing under heavy output current loads. R_x also increases the effective output impedance of the amplifier to $R_0 + R_x$, where R_0 is the output impedance of the device.

Figure 34. Output Short-Circuit Protection

POWER DISSIPATION

Although the AD859x amplifiers are able to provide load currents of up to 250 mA, proper attention should be given to not exceeding the maximum junction temperature for the device. The junction temperature equation is

$$
T_J = P_{DISS} \times \theta_{JA} + T_A \tag{3}
$$

where:

 T_J is the AD859x junction temperature.

 P_{DISS} is the AD859x power dissipation.

 θ_{JA} is the AD859x junction-to-ambient thermal resistance of the package.

 T_A is the ambient temperature of the circuit.

In any application, the absolute maximum junction temperature must be limited to 150°C. If the junction temperature is exceeded, the device could suffer premature failure. If the output voltage and output current are in phase, for example, with a purely resistive load, the power dissipated by the AD859x can be found as

$$
P_{DISS} = I_{LOAD} \times (V_{SY} - V_{OUT})
$$
\n(4)

where:

I_{LOAD} is the AD859x output load current. V_{SY} is the AD859x supply voltage. V_{OUT} is the output voltage.

By calculating the power dissipation of the device and using the thermal resistance value for a given package type, the maximum allowable ambient temperature for an application can be found using Equation 3.

CAPACITIVE LOADING

The AD859x exhibits excellent capacitive load driving capabilities and can drive to 10 nF directly. Although the device is stable with large capacitive loads, there is a decrease in amplifier bandwidth as the capacitive load increases. [Figure 35](#page-11-1) shows a graph of the AD8592 unity-gain bandwidth under various capacitive loads.

When driving heavy capacitive loads directly from the AD859x output, a snubber network can be used to improve the transient response. This network consists of a series RC connected from the output of the amplifier to ground, placing it in parallel with the capacitive load. The configuration is shown in [Figure 36](#page-11-2). Although this network does not increase the bandwidth of the amplifier, it significantly reduces the amount of overshoot, as shown in [Figure 37](#page-11-3).

Caused by Driving Heavy Capacitive Loads

The optimum values for the snubber network should be determined empirically based on the size of the capacitive load. [Table 5](#page-11-4) shows a few sample snubber network values for a given load capacitance.

PC98-COMPLIANT HEADPHONE/SPEAKER AMPLIFIER

Because of its high output current performance and shutdown feature, the AD8592 makes an excellent amplifier for driving an audio output jack in a computer application. [Figure 38](#page-11-5) shows how the AD8592 can be interfaced with an AC'97 codec to drive headphones or speakers.

Figure 38. PC98-Compliant Headphone/Line Out Amplifier

Figure 36. Configuration for Snubber Network to Compensate for Capacitive Loads

When headphones are plugged into the jack, the normalizing contacts disconnect from the audio contacts. This allows the voltage to the AD8592 shutdown pins to be pulled to 5 V, activating the amplifiers. With no plug in the output jack, the shutdown voltage is pulled to 100 mV through the R1 and R3 + R5 voltage divider. This powers the AD8592 down when it is not needed, saving current from the power supply or battery.

If gain is required from the output amplifier, add four additional resistors, as shown in [Figure 39](#page-12-1). The gain of the AD8592 can be set as

Figure 39. PC98-Compliant Headphone/Line Out Amplifier with Gain

Input coupling capacitors are not required for either circuit because the reference voltage is supplied from the [AD1881A.](http://www.analog.com/AD1881A)

R4 and R5 help protect the AD8592 output in case the output jack or headphone wires accidentally are shorted to ground. The output coupling capacitors, C1 and C2, block dc current from the headphones and create a high-pass filter with a corner frequency of

$$
f_{-3dB} = \frac{1}{2\pi C \Gamma (R4 + R_L)}
$$
(6)

where R_L is the resistance of the headphones.

A COMBINED MICROPHONE AND SPEAKER AMPLIFIER FOR CELLPHONE AND PORTABLE HEADSETS

The dual amplifiers in the AD8592 make an efficient design for interfacing with a headset containing a microphone and speaker. [Figure 40](#page-12-2) demonstrates a simple method for constructing an interface to a codec.

Figure 40. Speaker/Microphone Headset Amplifier Circuit

U1-A is used as a microphone preamplifier, where the gain of the preamplifier is set as R3/R2. R1 is used to bias an electret microphone, and C1 blocks any dc voltages from the amplifier. U1-B is the speaker amplifier, and its gain is set at R5/R4. To sum a stereo output, add R6, equal in value to R4.

Using the same principle described in the [PC98-Compliant](#page-11-6) [Headphone/Speaker Amplifier](#page-11-6) section, the normalizing contact on the microphone/speaker jack can be used to put the AD8592 into shutdown when the headset is not plugged in. The AD8592 shutdown inputs can also be controlled with TTL- or CMOScompatible logic, allowing microphone or speaker muting, if desired.

AN INEXPENSIVE SAMPLE-AND-HOLD CIRCUIT

The independent shutdown control of each amplifier in the AD8592 allows a degree of flexibility in circuit design. One particular application for which this feature is useful is in designing a sample-and-hold circuit for data acquisition. [Figure 41](#page-12-3) shows a schematic of a simple, yet extremely effective, sampleand-hold circuit using a single AD8592 and one capacitor.

Figure 41. An Efficient Sample-and-Hold Circuit

The U1-A amplifier is configured as a unity-gain buffer driving a 1 nF capacitor. The input signal is connected to the noninverting input, and the sample clock controls the shutdown for that amplifier. When the sample clock is high, the U1-A amplifier is active and the output follows V_{IN} . When the sample clock goes low, U1-A shuts down with the output of the amplifier going to a high impedance state, holding the voltage on the C1 capacitor.

The U1-B amplifier is used as a unity-gain buffer to prevent loading on C1. Because of the low input bias current of the U1-B CMOS input stage and the high impedance state of the U1-A output in shutdown, there is little voltage droop from C1 during the hold period. This circuit can be used with sample frequencies as high as 500 kHz and as low as 1 Hz. By increasing the C1 value, lower voltage droop is achieved for very low sample rates.

DIRECT ACCESS ARRANGEMENT FOR PCMCIA MODEMS (TELEPHONE LINE INTERFACE)

[Figure 42](#page-13-1) illustrates a 5 V transmit/receive telephone line interface for 600 Ω systems. It allows full duplex transmission of signals on a transformer-coupled 600 Ω line in a differential manner. Amplifier A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured to apply the largest possible signal on a single supply to the transformer. Because of the high output current drive and low dropout voltages of the AD8594, the largest signal available on a single 5 V supply is approximately 4.5 V p-p into a 600 Ω transmission system. Amplifier A3 is configured as a difference amplifier for two reasons. It prevents the transmit signal from interfering with the receive signal, and it extracts the receive signal from the transmission line for amplification by A4. The gain of A4 can be adjusted in the same manner as the gain of A1 to meet the input signal requirements of the modem. Standard resistor values permit the use of single inline package (SIP) format resistor arrays. Couple this with the 16-lead TSSOP or SOIC footprint of the AD8594, and this circuit offers a compact, cost-effective solution.

Figure 42. Single-Supply Direct Access Arrangement for PCMCIA Modems

SINGLE-SUPPLY DIFFERENTIAL LINE DRIVER

[Figure 43](#page-13-2) shows a single-supply differential line driver circuit that can drive a 600 Ω load with less than 0.7% distortion from 20 Hz to 15 kHz with an input signal of 4 V p-p and a single 5 V supply. The design uses an AD8594 to mimic the performance of a fully balanced transformer-based solution. However, this design occupies much less board space, while maintaining low distortion, and can operate down to dc. Like the transformer-based design, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1.

Figure 43. Low Noise, Single-Supply Differential Line Driver

R8 and R9 set up the common-mode output voltage equal to half of the supply voltage. C1 is used to couple the input signal and can be omitted if the dc voltage of the input is equal to half of the supply voltage.

The circuit can also be configured to provide additional gain, if desired. The gain of the circuit is

$$
A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R3}{R2}
$$
 (7)

where:

 $V_{OUT} = V_{O1} - V_{O2}$ $R2 = R7 = R10 = R11$ $R3 = R6 = R12 = R1$

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OUTLINE DIMENSIONS

Figure 47. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16) Dimensions shown in millimeters

ORDERING GUIDE

 $1 Z =$ RoHS Compliant Part, # denotes RoHS compliant part may be top or bottom marked.

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