NXP Semiconductors
Technical Data

Document Number: MC34VR500
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Multi-output DC/DC regulator for QorIQ LS1/T1 family of communications processors

34VR500

Power Management

ES SUFFIX (WF-TYPE)
98ASA00589D
56 QFN-EP WF8X8

The 34VR500 is a high performance, highly integrated, multi-output, SMARTMOS, DC/DC regulator solution, with integrated power MOSFETs ideally suited for the LS1/T1 family of communication processors. Integrating four switching and five linear regulators, the 34VR500 provides power to the complete system, including the processor, DDR memory, and system peripherals.

Features:

- Four buck converters:
  - SW1: 4.5 A
  - SW2: 2.0 A
  - SW3: 2.5 A
  - SW4: 1.0 A, (VTT tracking regulator)
- Five general purpose linear regulators
- DDR termination reference voltage (DDR3L and DDR4)
- Programmable low-power modes
- I^2C control of all the regulators
- Power Control Logic with processor interface and event detection

Applications:

- Internet of things (IoT) gateway
- Mobile wireless router
- MFP printer
- Network attached storage
- Automatic teller machine

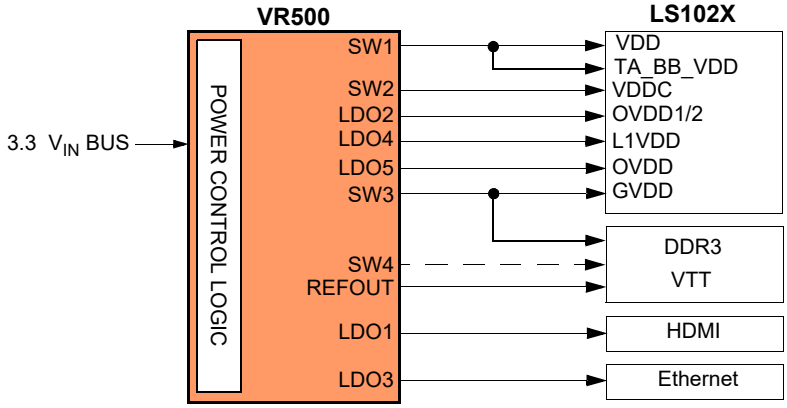


Figure 1. 34VR500 simplified application diagram

Table of Contents

1 Orderable parts

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search for the following device numbers.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	SW4 VTT mode	Processor	Reference design	DDR memory	Notes
MC34VR500V1ES	-40 °C to +105 °C	56 QFN 8x8 mm	Enabled	LS1020/21/22A	LS1021A IOT Gateway TWR-LS1021A	DDR3L (VTT = 0.675 V)	(1)(2)
MC34VR500V2ES			Disabled			N/A	
MC34VR500V3ES			Enabled			DDR4 (VTT = 0.6 V)	
MC34VR500V4ES			Enabled	LS1043/23A T1023/13	LS1043ARDB T1023RDB		
MC34VR500V5ES			Enabled			DDR3L (VTT = 0.675 V)	
MC34VR500V6ES			Enabled	LS1024A			
MC34VR500V7ES			Enabled	LS1020/21/22A		DDR4 (VTT = 0.6 V)	
MC34VR500V8ES			Disabled	LS1046A	LS1046ARDB-PA		
MC34VR500V9ES			Disabled	LS1028	LS1028A-RDB		
MC34VR500VAES			Enabled	LS1043/23A T1023/13	LS1043ARDB T1023RDB	DDR4 (VTT = 0.6 V)	
MC34VR500VBES			Disabled	LX2160		N/A	
MC34VR500VCES			Disabled	LS1046A	LS1046ARDB-PB		

Notes
1. For tape and reel, add an R2 suffix to the part number.
2. See Table 8 for the start-up configuration.

2 Internal block diagram

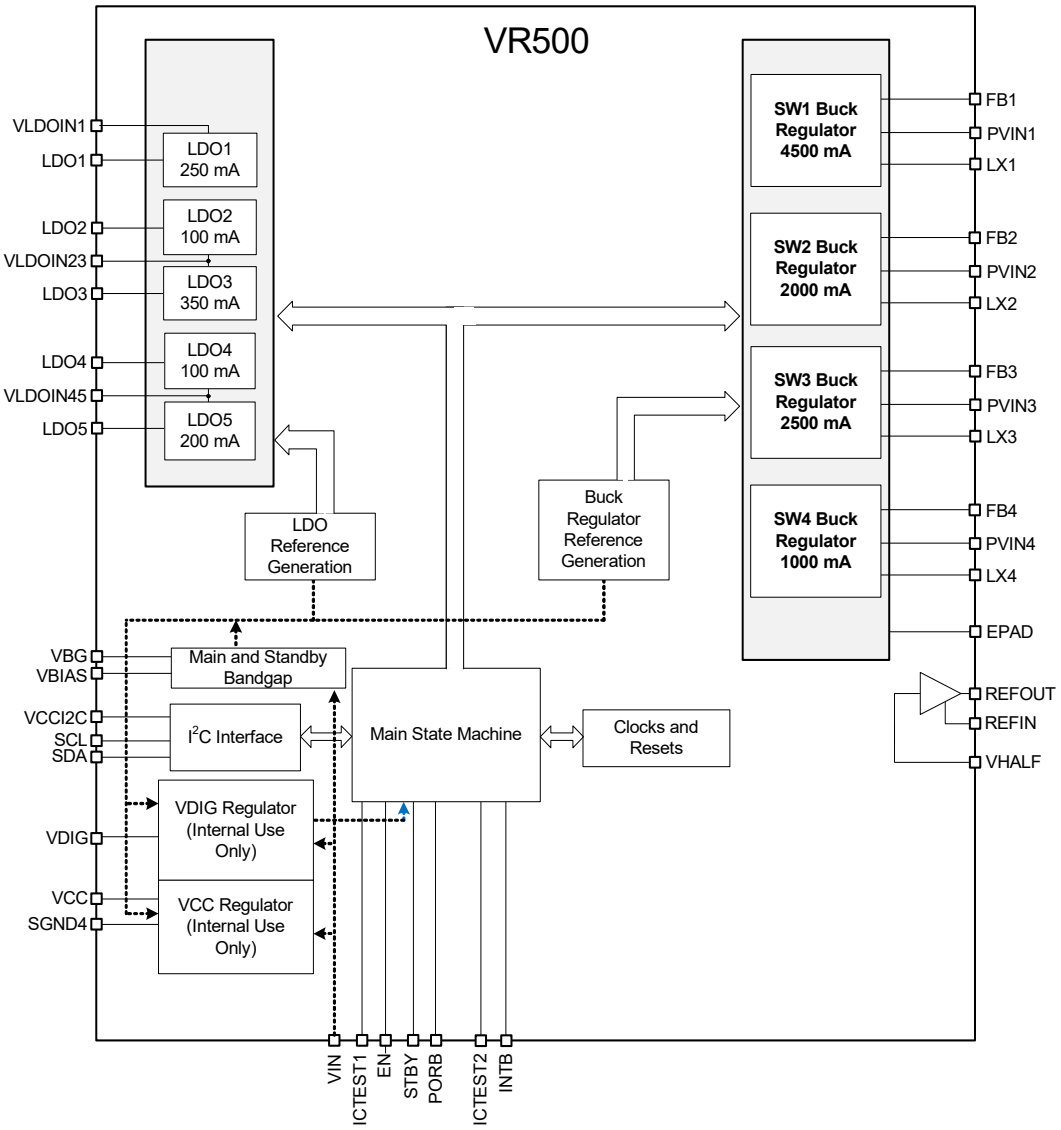


Figure 2. 34VR500 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

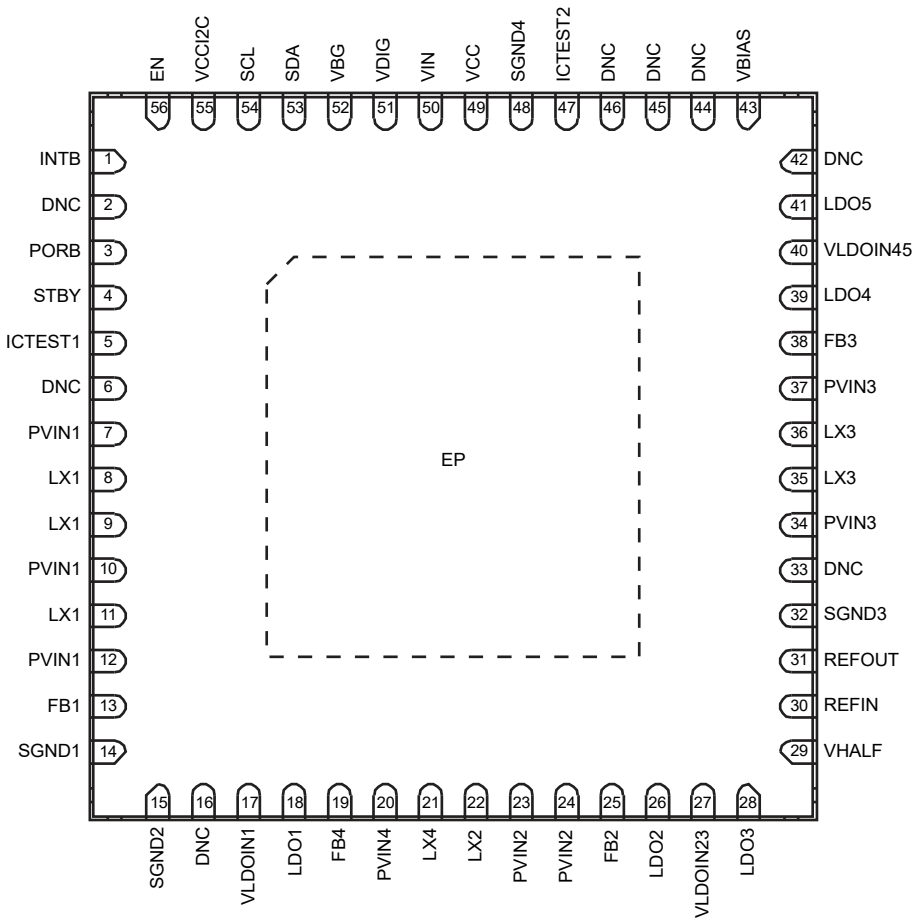


Figure 3. 34VR500 pinout diagram

3.2 Pin definitions

Table 2. 34VR500 Pin Definitions

Pin number	Pin name	Pin function	Max. rating	Type	Definition
1	INTB	O	3.6 V	Digital	Open drain interrupt signal to processor
2, 6, 16, 33, 42, 44, 45, 46	DNC	—	—	Reserved	Leave floating
3	PORB	O	3.6 V	Digital	Open drain reset output to processor.
4	STBY	I	3.6 V	Digital	Standby input signal from processor
5	ICTEST1	I	7.5 V	Digital/ Analog	Reserved pin. Connect to GND in application.

Table 2. 34VR500 Pin Definitions (continued)

Pin number	Pin name	Pin function	Max. rating	Type	Definition
7, 10, 12	PVIN1 (3)	I	4.8 V	Analog	Input to SW1 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
8, 9, 11	LX1 (3)	O	4.8 V	Analog	SW1 switching node connection
13	FB1 (3)	I	3.6 V	Analog	Output voltage feedback for SW1. Route this trace separately from the high current path and terminate at the output capacitance.
14	SGND1	GND	-	GND	Signal ground for SW1 regulator. Connect to ground plane directly.
15	SGND2	GND	-	GND	Signal ground for SW2 and SW4 regulators. Connect to ground plane directly.
17	VLDOIN1	I	3.6 V	Analog	Input supply for LDO1. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible.
18	LDO1	O	2.5 V	Analog	LDO1 regulator output, Bypass with a 4.7 µF ceramic output capacitor.
19	FB4 (3)	I	3.6 V	Analog	Output voltage feedback for SW4. Route this trace separately from the high current path and terminate at the output capacitance.
20	PVIN4 (3)	I	4.8 V	Analog	Input to SW4 regulator. Bypass with at least a 4.7µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
21	LX4 (3)	O	4.8 V	Analog	Regulator 4 switching node connection
22	LX2 (3)	O	4.8 V	Analog	Regulator 2 switching node connection
23, 24	PVIN2 (3)	I	4.8 V	Analog	Input to SW2 regulator. Connect pins 23 and 24 together and bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to these pins as possible.
25	FB2 (3)	I	3.6 V	Analog	Output voltage feedback for SW2. Route this trace separately from the high current path and terminate at the output capacitance.
26	LDO2	O	3.6 V	Analog	LDO2 regulator output. Bypass with a 2.2 µF ceramic output capacitor.
27	VLDOIN23	I	3.6 V	Analog	Input supply for LDO2 and LDO3. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible.
28	LDO3	O	3.6 V	Analog	LDO3 regulator output, Bypass with a 4.7 µF ceramic output capacitor.
29	VHALF	I	3.6 V	Analog	Half supply reference for DDR reference.
30	REFIN	I	3.6 V	Analog	REFOUT regulator input. Bypass with at least 1.0 µF decoupling capacitor as close to the pin as possible.
31	REFOUT	O	3.6 V	Analog	REFOUT regulator output
32	SGND3	GND	-	GND	Ground reference for the SW3 regulator. Connect directly to ground plane.
34, 37	PVIN3 (3)	I	4.8 V	Analog	Input to SW3 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
35, 36	LX3 (3)	O	4.8 V	Analog	Regulator SW3 switching node connection
38	FB3 (3)	I	3.6 V	Analog	Output voltage feedback for SW3. Route this trace separately from the high current path and terminate at the output capacitance.
39	LDO4	O	3.6 V	Analog	LDO4 regulator output. Bypass with a 2.2 µF ceramic output capacitor.
40	VLDOIN45	I	4.8 V	Analog	Input supply for LDO4 and LDO5. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible.
43	VBIAS	I	1.8 V	Analog	Bypass the pin with a 0.47 µF capacitor.
41	LDO5	O	3.6 V	Analog	LDO5 regulator output. By pass with a 2.2 µF ceramic output capacitor.
47	ICTEST2	I	7.5 V	Digital/ Analog	Reserved pin. Connect to GND in application.
48	SGND4	GND	-	GND	Ground for the main band gap regulator. Connect directly to ground plane.
49	VCC	O	3.6 V	Analog	Analog Core supply

Table 2. 34VR500 Pin Definitions (continued)

Pin number	Pin name	Pin function	Max. rating	Type	Definition
50	VIN	I	4.8 V	Analog	Main chip supply
51	VDIG	O	1.5 V	Analog	Digital Core supply
52	VBG	O	1.5 V	Analog	Main band gap reference. Bypass with 0.22uF capacitor.
53	SDA	I/O	3.6 V	Digital	I^2C data line (Open drain)
54	SCL	I	3.6 V	Digital	I^2C clock
55	VCCI2C	I	3.6 V	Analog	Supply for I^2C bus. Bypass with 0.1 μF ceramic capacitor
56	EN	I	3.6 V	Digital	Enable input. Connect to the processor. Pull-up via an 8.0 kΩ to 100 kΩ to VBIAS if required
-	EP	GND	-	GND	Expose pad. Functions as ground return for buck regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation.

Notes

3. Unused switching regulators should be connected as follow: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to the VIN pin with a 0.1 μF bypass capacitor.

4 General product characteristics

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Symbol	Description	Value	Unit	Notes
Electrical ratings				
V_{IN}	Main input supply voltage	-0.3 to 4.8	V	
V_{ESD}	ESD Ratings Human Body Model Charge Device Model	 ±2000 ±500	V	(4)

Notes

4. ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF).

4.2 Thermal characteristics

Table 4. Thermal ratings

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Thermal ratings					
T_A	Ambient Operating Temperature Range	-40	105	°C	
T_J	Operating Junction Temperature Range	-40	125	°C	(5)
T_{ST}	Storage Temperature Range	-65	150	°C	
T_{PPRT}	Peak Package Reflow Temperature	–	Note 7	°C	(6) (7)
QFN56 Thermal resistance and package dissipation ratings					
$R_{\theta JA}$	Junction to Ambient Natural Convection Four layer board (2s2p) Eight layer board (2s6p)	 – –	 28 15	°C/W	(8) (9) (10)
$R_{\theta JMA}$	Junction to Ambient (at 200 ft/min) Four layer board (2s2p)	 –	 22	°C/W	(8) (10)
$R_{\theta JB}$	Junction to Board	–	10	°C/W	(11)
$R_{\Theta JCBOTTOM}$	Junction to Case Bottom	–	1.2	°C/W	(12)

Table 4. Thermal ratings *(continued)*

Symbol	Description (rating)	Min.	Max.	Unit	Notes
ΨJT	Junction to Package Top Natural Convection	–	2.0	°C/W	(12)

Notes

5. Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See Table 5 for thermal protection features.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
7. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
8. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
9. The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
10. Per JEDEC JESD51-6 with the board horizontal.
11. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
12. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
13. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.2.1 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in Table 4. To optimize the thermal management and to avoid overheating, the 34VR500 provides thermal protection. An internal comparator monitors the die temperature. Interrupts THERM110I, THERM120I, THERM125I, and THERM130I will be generated when the respective thresholds specified in Table 5 are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry will shut down the 34VR500. This thermal protection will act above the thermal protection threshold listed in Table 5. To avoid any unwanted power downs resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured such that this protection is not tripped under normal conditions.

Table 5. Thermal protection thresholds

Parameter	Min.	Typ.	Max.	Units	Notes
Thermal 110 °C Threshold (THERM110)	100	110	120	°C	
Thermal 120 °C Threshold (THERM120)	110	120	130	°C	
Thermal 125 °C Threshold (THERM125)	115	125	135	°C	
Thermal 130 °C Threshold (THERM130)	120	130	140	°C	
Thermal Warning Hysteresis	2.0	–	4.0	°C	
Thermal Protection Threshold	130	140	150	°C	

4.3 Electrical characteristics

4.3.1 I/O specifications

Table 6. General PMIC static characteristics.

T_A = -40 to 105 °C, V_{VIN} = 2.8 to 4.5 V, V_{VCCI2C} = 1.7 to 3.6 V, V_{VBIAS} = 1.0 V ±4.0%, typical external component values and full load current range, unless otherwise noted.

Pin Name	Parameter	Load Condition	Min.	Max.	Unit	Notes
EN	V_{IL}	–	0.0	0.2 *V_{VBIAS}	V	
	V_{IH}	–	0.8 *V_{VBIAS}	3.6	V	
PORB	V_{OL}	-2.0 mA	0.0	0.4	V	
	V_{OH}	Open Drain	0.7* V_{VIN}	V_{VIN}	V	
SCL	V_{IL}	–	0.0	0.2 * V_{VCCI2C}	V	
	V_{IH}	–	0.8 * V_{VCCI2C}	3.6	V	
SDA	V_{IL}	–	0.0	0.2 * V_{VCCI2C}	V	
	V_{IH}	–	0.8 * V_{VCCI2C}	3.6	V	
	V_{OL}	-2.0 mA	0.0	0.4	V	
	V_{OH}	Open Drain	0.7 * V_{VCCI2C}	V_{VCCI2C}	V	
INTB	V_{OL}	-2.0 mA	0.0	0.4	V	
	V_{OH}	Open Drain	0.7* V_{VIN}	V_{VIN}	V	
STBY	V_{IL}	–	0.0	0.2 *V_{VBIAS}	V	
	V_{IH}	–	0.8 *V_{VBIAS}	3.6	V	

4.3.2 Current consumption

Table 7. Current consumption summary

T_A = -40 to 105 °C, (See Table 3), V_{VIN} = 3.6 V, V_{VCCI2C} = 1.7 to 3.6 V, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{VIN} = 3.6 V, V_{VCCI2C} = 3.3 V, and 25 °C, unless otherwise noted.

Mode	34VR500 conditions	System conditions	Typ.	Max.	Unit	Notes
Off	Wake-up from EN active 32 k RC on All other blocks off VIN ≥ UVDET	PMIC able to wake-up	17	25	µA	(14) (15)
Sleep	Wake-up from EN active Trimmed reference active SW3 PFM Trimmed 16 MHz RC off 32 k RC on REFOUT disabled	DDR memories in self refresh	122	250	µA	(15)

Table 7. Current consumption summary (continued)

T_A = -40 to 105 °C, (See Table 3), V_{VIN} = 3.6 V, V_{VCCI2C} = 1.7 to 3.6 V, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{VIN} = 3.6 V, V_{VCCI2C} = 3.3 V, and 25 °C, unless otherwise noted.

Mode	34VR500 conditions	System conditions	Typ.	Max.	Unit	Notes
Standby	SW1 in PFM SW2 in PFM SW3 in PFM SW4 in PFM Trimmed 16 MHz RC enabled Trimmed reference active LDO1 - 5 enabled REFOUT enabled	Processor enabled in low power mode. All rails powered on except boost (load = 0 mA)	297	550	µA	(15)

Notes

14. When VIN is below the UVDET threshold, in the range of 1.8 V ≤ VIN < 2.65 V, the quiescent current increases by 50 µA, typically.
15. For PFM operation (as defined in Table 23).

5 General description

The 34VR500 is a high performance, highly integrated, multi-output, DC/DC regulator solution, with integrated power MOSFETs ideally suited for the LS1/T1 family of communication processors.

5.1 Features

This section summarizes the 34VR500 features.

- Input voltage range: 2.8 V to 4.5 V
- Buck regulators
- Four independent outputs
  - SW1, 4.5 A; 0.625 V to 1.875 V
  - SW2, 2.0 A; 0.625 V to 3.3 V
  - SW3, 2.5 A; 0.625 V to 3.3 V
  - SW4, 1.0 A; operates in VTT mode for DDR termination at 50 % of SW3 for 34VR500V1, 34VR500V3, 34VR500V4, 34VR500V5, 34VR500V6, 34VR500V7, 34VR500VA and 0.625 V to 1.975 V for 34VR500V2, 34VR500V8, 34VR500V9
- Dynamic voltage scaling
- Modes: PWM, PFM, APS
- Programmable output voltage
- Programmable current limit
- Programmable soft start
- Programmable PWM switching frequency
- Programmable OCP with fault interrupt
  - LDOs
- Five general purpose LDOs
  - LDO1, 0.80 V to 1.55 V, 250 mA
  - LDO2, 1.8 V to 3.3 V, 100 mA
  - LDO3, 1.8 V to 3.3 V, 350 mA
  - LDO4, 1.8 V to 3.3 V, 100 mA
  - LDO5, 1.8 V to 3.3 V, 200 mA
- Soft start
  - DDR memory reference voltage
- REFOUT, 10 mA
  - 16 MHz internal master clock
  - I^2C interface
  - User programmable Standby, Sleep, and OFF modes

5.2 Functional block diagram

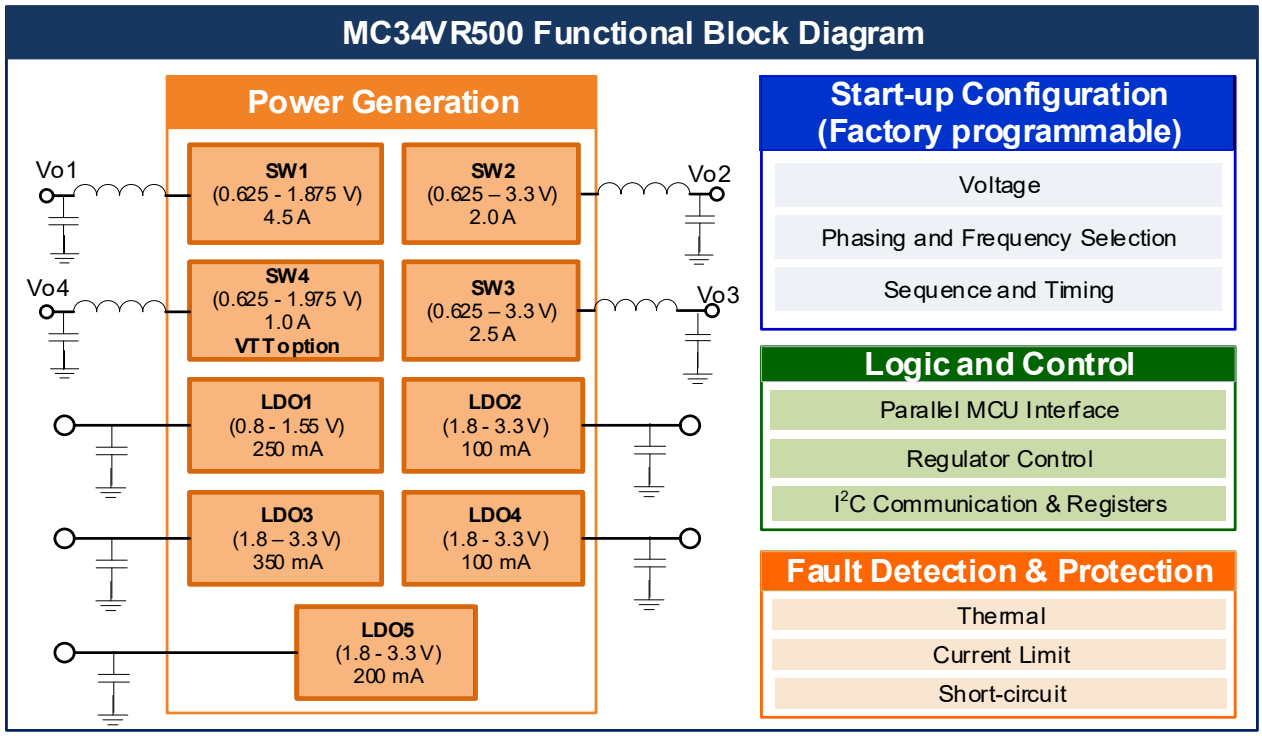


Figure 4. 34VR500 functional block diagram

5.3 Functional description

5.3.1 Power generation

The 34VR500 PMIC features four buck regulators, five general purpose LDOs, and a DDR voltage reference to supply voltages for the processor, memory, and peripheral devices.

Depending on the system power path configuration, the five general purpose LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, Wireless LAN, etc. A specific REFOUT voltage reference is included to provide accurate reference voltage for DDR memories operating with or without VTT termination

5.3.2 Control logic

The 34VR500 PMIC is fully programmable via the I^2C interface. Additional communication is provided by direct logic interfacing including interrupt and reset. Startup voltage and sequence are internally programed. After power up, the regulator voltages can be changed via I^2C. The 34VR500 PMIC has the interfaces for the power buttons and dedicated signaling interfacing with the processor.

5.3.2.1 Interface signals

EN

EN is an input signal to the IC that generates a turn-on event. Refer to section Turn on events for more details.

STBY

STBY is an input signal to the IC. When it is asserted the part enters standby mode and when de-asserted, the part exits standby mode. STBY can be configured as active high or active low using the STBYINV bit. Refer to the section Standby mode for more details.

PORB

PORB is an open-drain, active low output. In its default mode, it is de-asserted 2.0 to 4.0 ms after the last regulator in the start-up sequence is enabled; refer to Figure 8 as an example. In this mode, the signal can be used to bring the processor out of reset, or as an indicator that all supplies have been enabled; it is only asserted for a turn-off event.

INTB

INTB is an open-drain, active low output. It is asserted when any fault occurs, provided that the fault interrupt is unmasked. INTB is de-asserted after the fault interrupt is cleared by software, which requires writing a “1” to the fault interrupt bit.

6 Functional block requirements and behaviors

6.1 Start-up

The 34VR500 starts up from the internal configuration, which is hard-coded into the device. However, the 34VR500 can be controlled through the I^2C port after the Start-up sequence. It is also possible to modify the contents of the Internal Registers via the bus I^2C to modify the start up parameters (see section Start sequence creation).

6.1.1 Device start-up configuration

Table 8 shows the internal configuration for the 34VR500V1, 34VR500V2, 34VR500V3, 34VR500V4, 34VR500V5, 34VR500V6, 34VR500V7, 34VR500V8, 34VR500V9, 34VR500VA, 34VR500VB, 34VR500VC.

Table 8. Start-up configuration

Registers	34VR500V1	34VR500V2	34VR500V3	34VR500V4	34VR500V5	34VR500V6	34VR500V7	34VR500V8	34VR500V9	34VR500VA	34VR500VB	34VR500VC
Default I^2C	0x08											
LDO2_VOLT	1.8 V	1.8 V	1.8 V	2.5 V	2.5 V	1.8 V	1.8 V	2.5 V	2.5 V	2.5 V	3.3 V	2.5 V
LDO2_SEQ	1	1	1	2	2	2	1	4	5	2	2	4
LDO3_VOLT	2.5 V								—	2.5 V	2.5 V	2.5 V
LDO3_SEQ	1	1	3	2	2	4	3	4	—	2	2	4
LDO4_VOLT	2.5 V	2.5 V	2.5 V	1.8 V	1.8 V	3.0 V	2.5 V	1.8 V	2.5 V	1.8 V	1.8 V	1.8 V
LDO4_SEQ	1	1	1	3	3	5	1	5	8	3	—	5
LDO5_VOLT	1.8 V	1.8 V	1.8 V	3.3 V	3.3 V	3.3 V	1.8 V	3.3 V	—	3.3 V	3.3 V	3.3 V
LDO5_SEQ	1	1	1	3	3	5	1	7	—	3	—	7
SW1_VOLT	1.0 V	1.0 V	1.0 V	1.5 V	1.5 V	1.2 V	1.0 V	0.85 V	1.0 V	1.8 V	1.2 V	0.7 V
SW1_SEQ	2							1	5	1	3	1
SW2_VOLT	1.0 V	1.0 V	1.0 V	1.8 V	1.8 V	1.1 V	1.0 V	1.35 V	2.5 V	1.35 V	0.9 V	1.35 V
SW2_SEQ	2	2	2	1	1	1	2	1	2	1	1	1
SW3_VOLT	1.35 V	1.35 V	1.2 V	1.2 V	1.35 V	1.5 V	1.2 V	1.8 V	1.8 V	1.2 V	1.8 V	1.8 V
SW3_SEQ	3	3	3	12	12	3	3	1	3	12	1	1
SW4_VOLT	VTT	1.8 V	VTT	VTT	VTT	VTT	VTT	1.0 V	1.35 V	VTT	VTT	1.0 V
SW4_SEQ	3	3	3	12	12	3	3	5	4	12	—	5
REFOUT_SEQ	3	3	3	12	12	3	3	—	4	12	3	—
LDO1_VOLT	1.2 V	1.2 V	1.2 V	1.35 V	1.35 V	1.1 V	1.35 V	—	—	1.35 V	1.35 V	—
LDO1_SEQ	4	4	4	1	12	1	4	—	—	1	—	—
PU CONFIG, SEQ_CLK_SPEED	1.0 ms											
PU CONFIG, SWDVS_CLK	6.25 mV/µs											
SW1 CONFIG	2.0 MHz											
SW2 CONFIG	2.0 MHz											
SW3 CONFIG	2.0 MHz											
SW4 CONFIG	2.0 MHz											

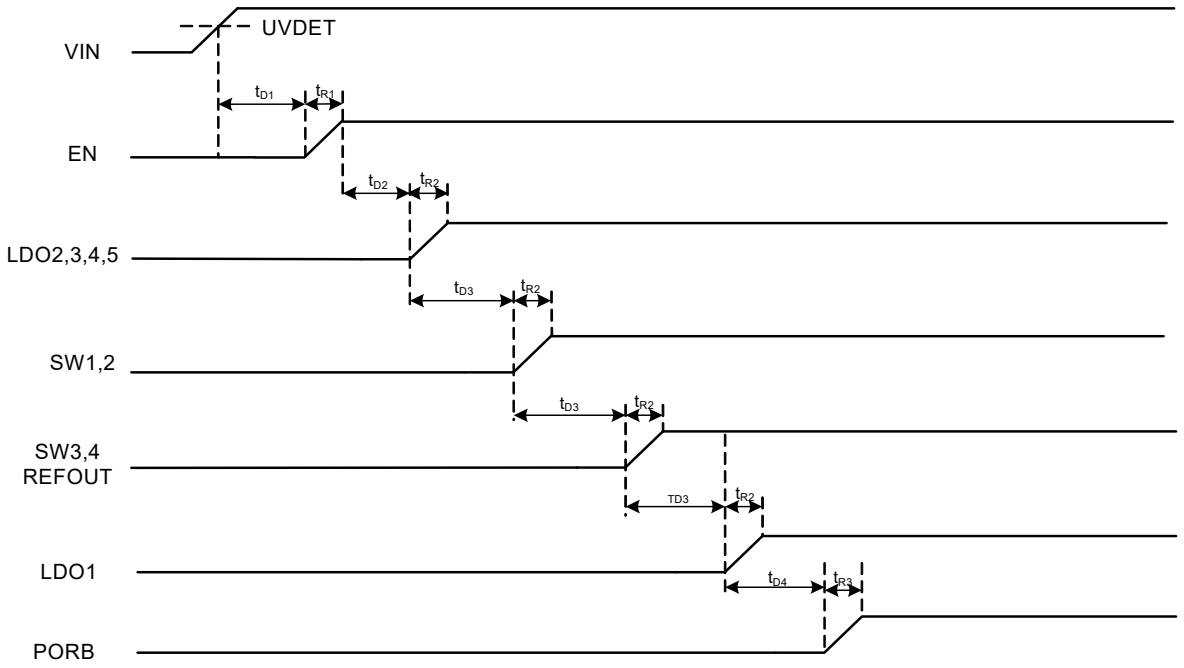


Figure 5. Starting sequence: example for V1 and V2

Table 9. 34VR500V1 and V2 start-up sequence timing

Parameter	Description	Typ.	Unit
t_{D1}	Turn-on delay	6.0	ms
t_{R1}	Rise time of EN	(16)	ms
t_{D2}	Turn-on delay of first regulator	2.5	ms
t_{R2}	Rise time of regulators (17)	0.2	ms
t_{D3}	Delay between regulators	1.0	ms
t_{D4}	Turn-on delay of PORB	2.0	ms
t_{R3}	Rise time of PORB	0.2	ms

Notes
16. Depends on the external signal driving EN.
17. Rise time is a function of slew rate of regulators and nominal voltage selected.

6.1.2 Start sequence creation

The 34VR500 powers up based on the contents of the internal registers. Depending on certain bit settings, the internal registers are loaded from different sources, as shown in Figure 6.

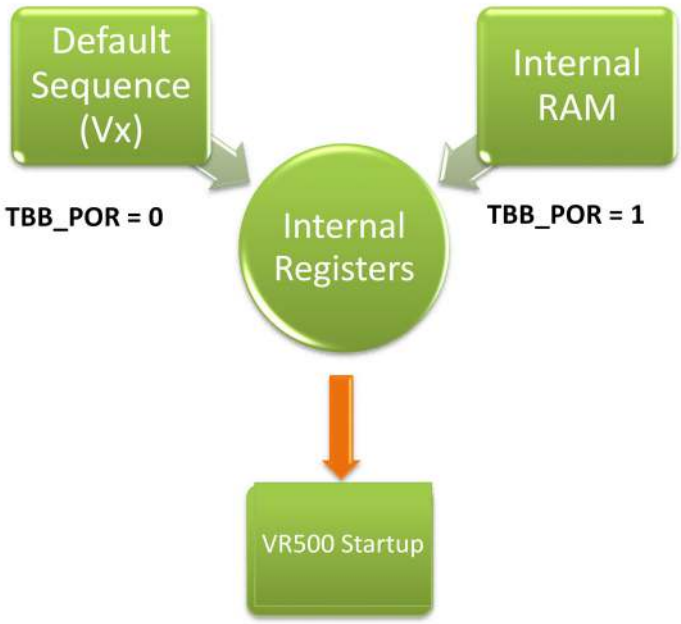


Figure 6. Starting sequence

The contents of the internal registers are initialized to zero when a valid V_{IN} is first applied. The values that are then loaded into the internal registers depend on the value of the TBB_POR (the initial value of TBB_POR is always “0”):

- If TBB_POR = 0 the values are loaded from the Default Sequence (this is the case always for first starting)
- If TBB_POR = 1 the values are loaded from the internal RAM. V_{IN} must be valid to maintain the contents of the internal RAM.

To power on with the contents of the internal RAM, the following conditions must exist:

- V_{IN} is valid
- TBB_POR = 1 and there is a valid turn-on event via the EN pin

To keep a regulator off during a start-up sequence is to set its sequence to 0. This corresponds to the XX_SEQ setting of 0x00.

For example, 0x01 corresponds to a sequence of 1, and so on.

Figure 7 explains how to start from a new configuration.

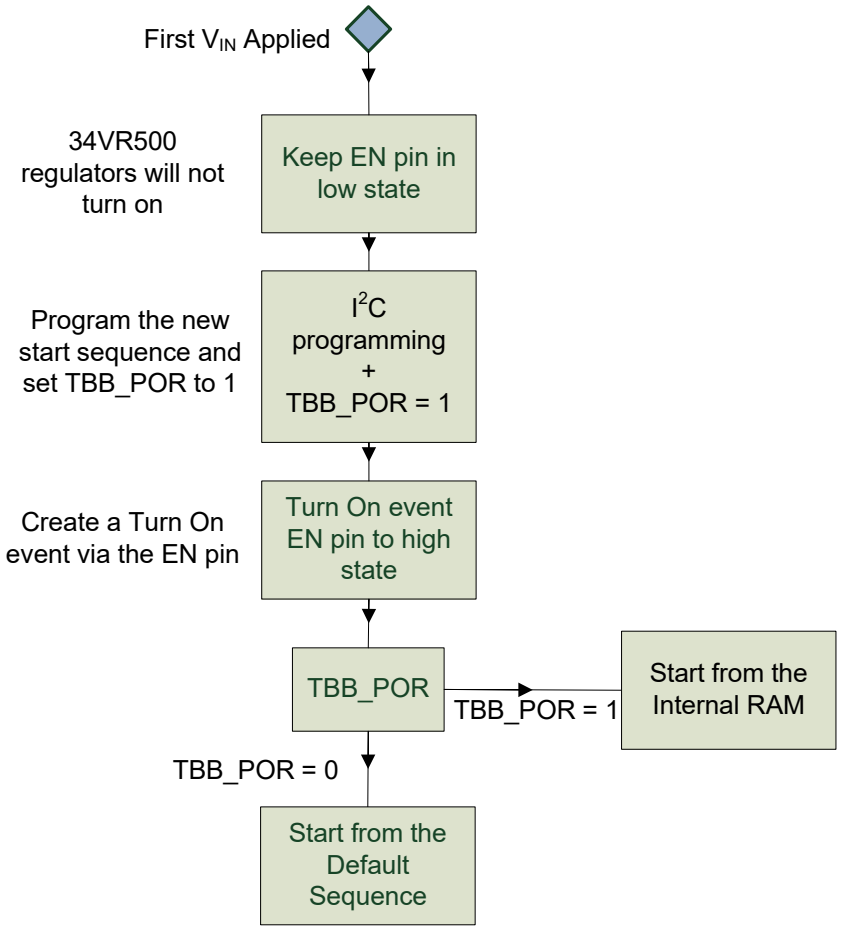


Figure 7. Modifying a starting sequence

Table 95 shows the portion of the register map concerning the programming of a new starting sequence.

6.2 16 MHz and 32 kHz clocks

There are two clocks: a trimmed 16 MHz, RC oscillator and an untrimmed 32 kHz, RC oscillator. The 16 MHz oscillator is specified within -8.0/+8.0%. The 32 kHz untrimmed clock is only used in the following conditions:

- V_{IN} < UVDET
- All regulators are in SLEEP mode
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start-up, V_{IN} > UVDET

In addition, when the 16 MHz is active in the ON mode, the debounce times in Table 20 are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and ENI interrupts, which are referenced to the 32 kHz untrimmed clock.

Table 10. 16 MHz clock specifications

T_A = -40 to 105 °C (See Table 3), V_{VIN} = 2.8 to 4.5 V, V_{VBIAS} = 1.0 V ±4.0%, and typical external component values. Typical values are characterized at V_{VIN} = 3.6 V, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
V_{IN}	Operating Voltage from the VIN pin	2.8	–	4.5	V	

Table 10. 16 MHz clock specifications

T_A = -40 to 105 °C (See Table 3), V_{VIN} = 2.8 to 4.5 V, V_{VBIAS} = 1.0 V ±4.0%, and typical external component values. Typical values are characterized at V_{VIN} = 3.6 V, and 25 °C, unless otherwise noted.

f_{16MHZ}	16 MHz Clock Frequency	14.7	16	17.3	MHz	
f_{2MHZ}	2.0 MHz Clock Frequency	1.84	–	2.16	MHz	(18)

Notes

18. 2.0 MHz clock is derived from the 16 MHz clock.

6.2.1 Clock adjustment

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16 MHz clock, the user may add an offset as small as ±3.0% of the nominal frequency. Contact a NXP representative for detailed information on this feature.

6.3 Bias and references block description

6.3.1 Internal core voltage references

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VBG. The bandgap and the rest of the core circuitry are supplied from VCC. Table 11 shows the main characteristics of the core circuitry.

Table 11. Core voltages electrical specifications(20)

T_A = -40 to 105 °C (See Table 3), V_{VIN} = 2.8 to 4.5 V, V_{VBIAS} = 1.0 V ±4.0%, and typical external component values. Typical values are characterized at V_{VIN} = 3.6 V, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
VDIG (digital core supply)						
V_{DIG}	Output Voltage ON mode OFF mode	 – –	 1.5 1.3	 – –	V	(19)
VCC (Analog core supply)						
V_{CC}	Output Voltage ON mode OFF mode	 – –	 2.775 0.0	 – –	V	(19)
VBG (bandgap / regulator reference)						
V_{BG}	Output Voltage	–	1.2	–	V	(19)
VBG_{ACC}	Absolute Accuracy	–	0.5	–	%	
VBG_{TACC}	Temperature Drift	–	0.25	–	%	

Notes

19. 3.0 V < V_{IN} < 4.5 V, no external loading on VDIG, VCC, or VBG. Extended operation down to UVDET, but no system malfunction.
20. For information only.

6.3.1.1 External components

Table 12. External components for core voltages

Regulator	Capacitor value (µF)
VDIG	1.0
VCC	1.0
VBG	0.22

6.3.2 REFOUT voltage reference

REFOUT is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. Its typically used as the reference voltage for DDR memories. A filtered resistor divider is utilized to create a low frequency pole. This divider then utilizes a voltage follower to drive the load.

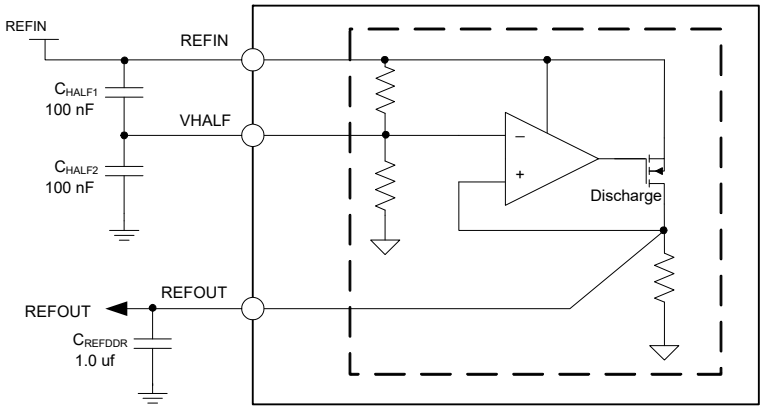


Figure 8. REFOUT block diagram

6.3.2.1 REFOUT control register

The REFOUT voltage reference is controlled by a single bit in REFOUTCTRL register in Table 13.

Table 13. Register REFOUTCTRL - ADDR 0x6A

Name	Bit #	R/W	Default	Description
UNUSED	3:0	–	0x00	UNUSED
REFOUTEN	4	R/W	0x00	Enable or disables REFOUT output voltage 0 = REFOUT Disabled 1 = REFOUT Enabled
UNUSED	7:5	–	0x00	UNUSED

External components

Table 14. REFOUT external components[21]

Capacitor	Capacitance (μF)
REFIN[22] to VHALF	0.1
VHALF to GND	0.1
REFOUT	1.0

Notes
21. Use X5R or X7R capacitors.
22. REFIN to GND, 1.0 μF minimum capacitance is provided by buck regulator output.

REFOUT specifications

Table 15. REFOUT electrical characteristics

T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, V_{REFIN} = 1.5 V, V_{VBIAS} = 1.0 V ±4.0%, and typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, V_{REFIN} = 1.5 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
REFOUT						
V_{REFIN}	Operating Input Voltage Range	1.2	–	1.8	V	
I_{REFDDR}	Operating Load Current Range	0.0	–	10	mA	
$I_{REFDDRLIM}$	Current Limit, I_{REFDDR} when V_{REFOUT} is forced to V_{REFIN}/4	10.5	15	25	mA	
$I_{REFDDRQ}$	Quiescent Current	–	8.0	–	µA	(23)
Active mode – DC						
V_{REFOUT}	Output Voltage 1.2 V < V_{REFIN} < 1.8 V, 0.0 mA < I_{REFDDR} < 10 mA	–	V_{REFIN}/2	–	V	
$V_{REFOUTTOL}$	Output Voltage Tolerance 1.2 V < V_{REFIN} < 1.8 V, 0.6 mA ≤ I_{REFDDR} ≤ 10 mA	–1.0	–	1.0	%	
$V_{REFOUTLOR}$	Load Regulation 1.0 mA < I_{REFDDR} < 10 mA, 1.2 V < V_{REFIN} < 1.8 V	–	0.40	–	mV/mA	
Active mode – AC						
$t_{ONREFDDR}$	Turn-on Time, Enable to 90% of end value V_{REFIN} = 1.2 V, 1.8 V, I_{REFDDR} = 0.0 mA	–	–	100	µs	
$t_{OFFREFDDR}$	Turn-Off Time, Disable to 10% of initial value V_{REFIN} = 1.2 V, 1.8 V, I_{REFDDR} = 0.0 mA	–	–	10	ms	
$V_{REFOUTOSH}$	Start-up Overshoot V_{REFIN} = 1.2 V, 1.8 V, I_{REFDDR} = 0.0 mA	–	1.0	6.0	%	
$V_{REFOUTTLR}$	Transient Load Response V_{REFIN} = 1.2 V, 1.8 V	–	5.0	–	mV	

Notes

23. When REFOUT is off there is a quiescent current of 1.5 µA typical.

6.4 Power generation

6.4.1 Modes of operation

The operation of the 34VR500 can be reduced to four states, or modes: ON, OFF, Sleep, and Standby. Figure 9 shows the state diagram of the 34VR500, along with the conditions to enter and exit from each state.

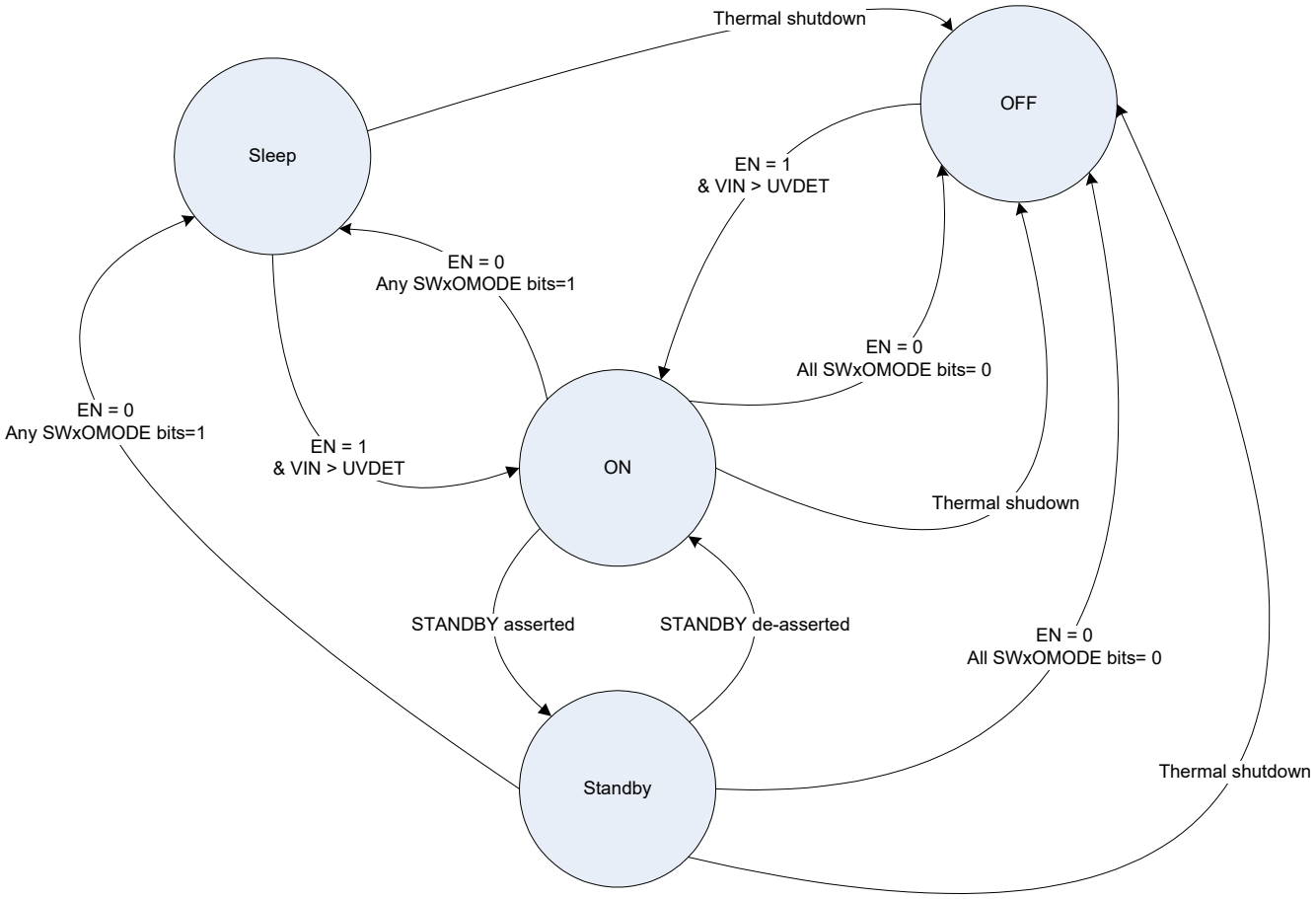


Figure 9. State diagram

To complement the state diagram in Figure 9, a description of the states is provided in following sections. Note that V_{IN} must exceed the rising UVDET threshold to allow a power up. Refer to Table 22 for the UVDET thresholds. Additionally, the interrupt signal and INTB are only active in Sleep, Standby, and ON states.

6.4.1.1 On mode

The 34VR500 enters the ON mode after a turn-on event. PORB is de-asserted, high, in this mode of operation.

6.4.1.2 Off mode

The 34VR500 enters the OFF mode after a turn-off event. A thermal shutdown event also forces the 34VR500 into the OFF mode. Only VDIG is powered in this mode of operation. To exit the OFF mode, a valid turn-on event is required. PORB is asserted, LOW, in this mode.

6.4.1.3 Standby mode

- Depending on STBY pin configuration, Standby is entered when the STBY pin is asserted. This is typically used for low-power mode of operation.
- When STBY is de-asserted, Standby mode is exited.

A product may be designed to go into a Low-power mode after periods of inactivity. The STBY pin is provided for board level control of going in and out of such deep sleep modes (DSM).

When a product is in DSM, it may be able to reduce the overall platform current by lowering the regulator output voltage, changing the operating mode of the regulators or disabling some regulators. The configuration of the regulators in Standby are pre-programmed through the I^2C interface.

Note that the STBY pin is programmable for Active High or Active Low polarity, and that decoding of a Standby event will take into account the programmed input polarity as shown in Table 16. When the 34VR500 is powered up first, regulator settings for the Standby mode are mirrored from the regulator settings for the ON mode. To change the STBY pin polarity to Active Low, set the STBYINV bit via software first, and then change the regulator settings for Standby mode as required. For simplicity, STBY will generally be referred to as active high throughout this document.

Table 16. STBY pin and polarity control

STBY (Pin)[25]	STBYINV (I^2C bit)[26]	STBY Control [24]
0	0	0
0	1	1
1	0	1
1	1	0

Notes

24. STBY = 0: System is not in Standby, STBY = 1: System is in Standby
25. The state of the STBY pin only has influence in On mode.
26. Bit 6 in Power Control Register (ADDR - 0x1B)

Since STBY pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes. A programmable delay is provided to hold off the system response to a Standby event. This allows the processor and peripherals some time after a standby instruction has been received to terminate processes to facilitate seamless entering into Standby mode.

When enabled (STBYDLY = 01, 10, or 11) per Table 17, STBYDLY will delay the Standby initiated response for the entire IC, until the STBYDLY counter expires.

An allowance should be made for three additional 32 k cycles required to synchronize the Standby event.

Table 17. STBY delay - initiated response

STBYDLY[1:0][27]	Function
00	No Delay
01	One 32 k period (default)
10	Two 32 k periods
11	Three 32 k periods

Notes

27. Bits [5:4] in Power Control Register (ADDR - 0x1B)

6.4.1.4 Sleep mode

- Depending on EN pin configuration, Sleep mode is entered when EN is de-asserted and SWxOMODE bit is set.
- To exit Sleep mode, assert the EN pin.

In the Sleep mode, the regulator will use the set point as programmed by SW1OFF[5:0] for SW1, SW2, SW3, and SW4. The activated regulators will maintain settings for this mode and voltage until the next turn-on event. Table 18 shows the control bits in Sleep mode. During Sleep mode, interrupts are active and the INTB pin will report any unmasked fault event.

Table 18. Regulator mode control

SWxOMODE	Off operational mode (sleep) (28)
0	Off
1	PFM

Notes

28. For sleep mode, an activated switching regulator, should use the off mode set point as programmed by SW1OFF[5:0] for SW1, SW2, SW3, and SW4.

6.4.2 State machine flow summary

Table 19 provides a summary matrix of the 34VR500 flow diagram to show the conditions needed to transition from one state to another.

Table 19. State machine flow summary

STATE		Next state			
		OFF	Sleep	Standby	ON
Initial state	OFF	X	X	X	EN = 1 & V_{IN} > UVDET
	Sleep	Thermal Shutdown	X	X	EN = 1 & V_{IN} > UVDET
	Standby	Thermal Shutdown	EN = 0, Any SWxOMODE = 1	X	Standby de-asserted
		EN = 0, All SWxOMODE = 0			
	ON	Thermal Shutdown	EN = 0, Any SWxOMODE = 1	Standby asserted	X
		EN = 0, All SWxOMODE = 0			

6.4.2.1 Turn on events

From OFF and Sleep modes, the PMIC is powered on by a turn ON event. V_{IN} must be greater than UVDET for the PMIC to turn-on. When V_{IN} is greater than UVDET, a logic high on the EN pin is a turn ON event, when EN is high before V_{IN} is valid, a V_{IN} transition, from 0.0 V to a voltage greater than UVDET, also a Turn ON event. See the State diagram, Figure 9, and the Table 19 for more details. Any regulator enabled in the Sleep mode will remain enabled when transitioning from Sleep to ON, i.e., the regulator will not be turned OFF and then ON again to match the start-up sequence. The following is a more detailed description of the EN configuration:

- The EN signal is high and V_{IN} > UVDET, the PMIC will turn ON; the interrupt and sense bits, ENI and ENS respectively, will be set.

The sense bit will show the real time status of the EN pin. In this configuration, the EN input can be a mechanical switch debounced through a programmable debouncer, ENDBNC[1:0], to avoid a response to a very short (i.e., unintentional) key press. The interrupt is generated for both the falling and the rising edge of the EN pin. By default, a 30 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with ENDBNC[1:0] as defined in the table below. The interrupt is cleared by software, or when cycling through the OFF mode.

Table 20. EN hardware debounce bit settings

Bits	State	Turn on debounce (ms)	Falling edge INT debounce (ms)	Rising edge INT debounce (ms)
ENDBNC[1:0]	00	0.0	31.25	31.25
	01	31.25	31.25	31.25
	10	125	125	31.25
	11	750	750	31.25

Notes
29. The sense bit, ENS, is not debounced and follows the state of the EN pin.

6.4.2.2 Turn off events

EN pin

The EN pin is used to power off the 34VR500. The Off mode is entered when the EN pin is low and SWxOMODE = 0.

Thermal protection

If the die temperature surpasses a given threshold, the thermal protection circuit will power off the 34VR500 to avoid damage. A turn-on event will not power on the PMIC while it is in thermal protection. The part will remain in Off mode until the die temperature decreases below a given threshold. There are no specific interrupts related to this other than the warning interrupt. See Power dissipation section for more detailed information.

Undervoltage detection

The state machine will transition to the OFF mode when the voltage at the VIN pin drops below the UVDET undervoltage falling threshold.

6.4.3 Power tree

The 34VR500 features four buck regulators, five general purpose LDOs, and a DDR voltage reference, to supply voltages for the application and peripheral devices. The buck regulators are supplied directly from the main input supply (V_{IN}). The inputs to all of the buck regulators must be tied to V_{IN}, whether they are powered ON or OFF. The five general use LDO regulators are directly supplied from the main input supply or from the switching regulators depending on the application requirements. Since REFOUT is intended to provide DDR memory reference voltage, it should be supplied by any rail supplying voltage to DDR memories; the typical application recommends the use of SW3 as the input supply for REFOUT. Refer to Table 21 for a summary of all power supplies provided by the 34VR500.

Table 21. Power tree summary

Supply	Output voltage (V)	Step size (mV)	Maximum load current (mA)
SW1	0.625 - 1.875	25	4500
SW2	0.625 - 1.975 / 0.8 - 3.3	25 / 50	2000
SW3	0.625 - 1.975 / 0.8 - 3.3	25 / 50	2500
SW4	0.5*SW3_OUT (VTT for V1, V3, V4, V5), 0.625 - 1.975 (for V2)		1000
LDO1	0.80 – 1.55	50	250
LDO2	1.8 – 3.3	100	100
LDO3	1.8 – 3.3	100	350
LDO4	1.8 – 3.3	100	100
LDO5	1.8 – 3.3	100	200
REFOUT	0.5*SW3_OUT	NA	10

The minimum operating voltage for the main V_{IN} supply is 2.8 V, for lower voltages proper operation is not guaranteed. However at initial power up, the input voltage must surpass the rising UVDET threshold before proper operation is guaranteed. Refer to the representative tables and text specifying each supply for information on performance metrics and operating ranges. Table 22 summarizes the UVDET thresholds.

Table 22. UVDET threshold

UVDET threshold	V_{IN}
Rising	3.1 V
Falling	2.65 V

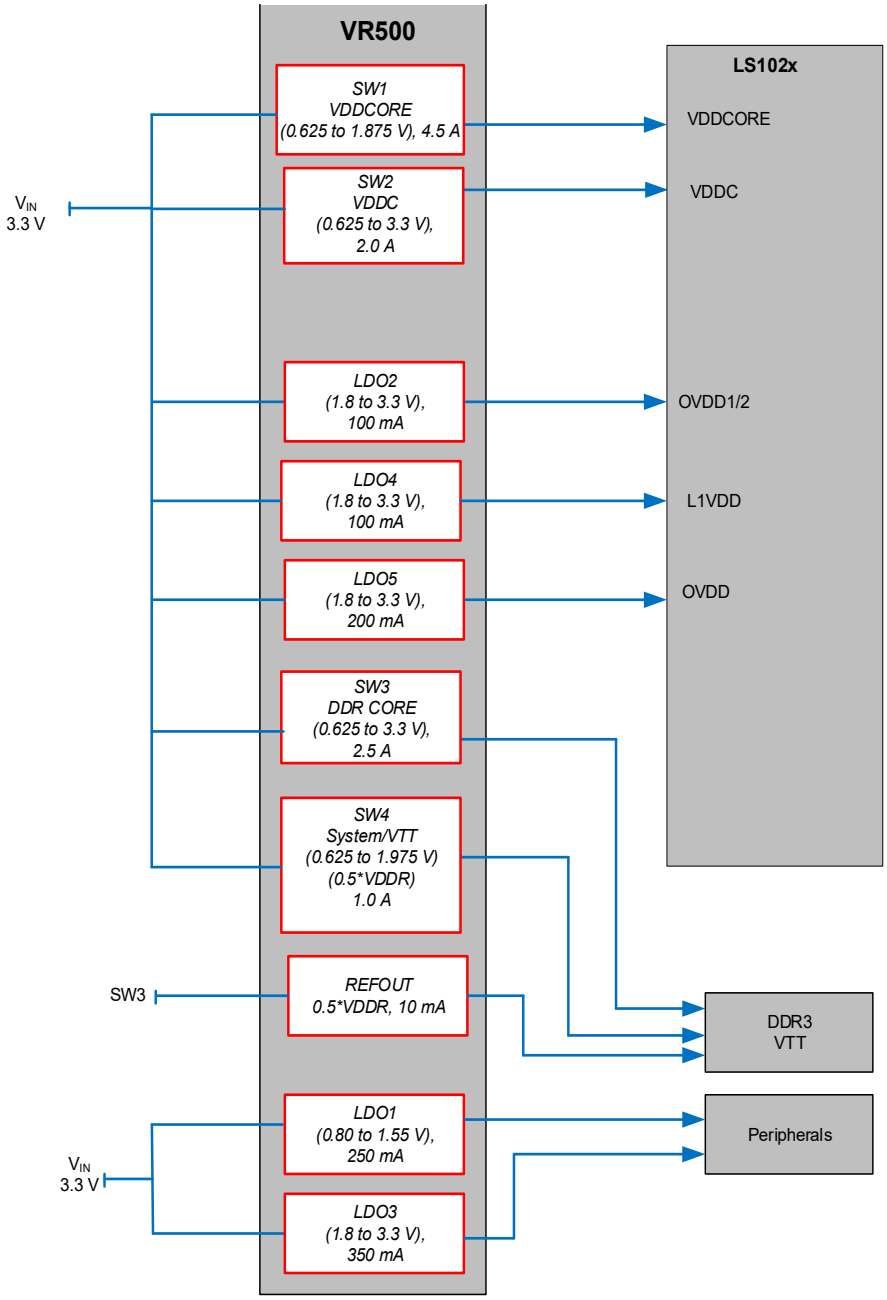


Figure 10. 34VR500 typical power map

6.4.4 Buck regulators

Each buck regulator is capable of operating in PFM, APS, and PWM switching modes.

6.4.4.1 Current limit

Each buck regulator has a programmable current limit. In an overcurrent condition, the current is limited cycle-by-cycle. If the current limit condition persists for more than 8.0 ms, a fault interrupt is generated.

6.4.4.2 General control

To improve system efficiency the buck regulators can operate in different switching modes. Changing between switching modes can occur by any of the following means: I^2C programming, exiting/entering the Standby mode, exiting/entering Sleep mode, and load current variation. Available switching modes for buck regulators are presented in Table 23.

Table 23. Switching mode description

Mode	Description
OFF	The regulator is switched off and the output voltage is discharged.
PFM	In this mode, the regulator is always in PFM mode, which is useful at light loads for optimized efficiency.
PWM	In this mode, the regulator is always in PWM mode operation regardless of load conditions.
APS	In this mode, the regulator moves automatically between pulse skipping mode and PWM mode depending on load conditions.

During soft-start of the buck regulators, the controller transitions through the PFM, APS, and PWM switching modes. 3.0 ms (typical) after the output voltage reaches regulation, the controller transitions to the selected switching mode. Depending on the particular switching mode selected, additional ripple may be observed on the output voltage rail as the controller transitions between switching modes.

Table 24 summarizes the Buck regulator programmability for Normal and Standby modes.

Table 24. Regulator mode control

SWxMODE[3:0]	Normal Mode	Standby Mode	SWxMODE[3:0]	Normal Mode	Standby Mode
0000	Off	Off	1000	APS	APS
0001	PWM	Off	1001	Reserved	Reserved
0010	Reserved	Reserved	1010	Reserved	Reserved
0011	PFM	Off	1011	Reserved	Reserved
0100	APS	Off	1100	APS	PFM
0101	PWM	PWM	1101	PWM	PFM
0110	PWM	APS	1110	Reserved	Reserved
0111	Reserved	Reserved	1111	Reserved	Reserved

Transitioning between Normal and Standby modes can affect a change in switching modes as well as output voltage. The rate of the output voltage change is controlled by the Dynamic Voltage Scaling (DVS), explained in Dynamic voltage scaling. For each regulator, the output voltage options are the same for Normal and Standby modes.

When in Standby mode, the regulator outputs the voltage programmed in its standby voltage register and will operate in the mode selected by the SWxMODE[3:0] bits. Upon exiting Standby mode, the regulator will return to its normal switching mode and its output voltage programmed in its voltage register.

Any regulators whose SWxOMODE bit is set to “1” will enter Sleep mode if a EN turn-off event occurs, and any regulator whose SWxOMODE bit is set to “0” will be turned off. In Sleep mode, the regulator outputs the voltage programmed in its off (Sleep) voltage register and operates in the PFM mode. The regulator will exit the Sleep mode when a turn-on event occurs. Any regulator whose SWxOMODE bit is set to “1” will remain on and change to its normal configuration settings when exiting the Sleep state to the ON state. Any regulator whose SWxOMODE bit is set to “0” will be powered up with the same delay in the start-up sequence as when powering On from Off. At this point, the regulator returns to its default ON state output voltage and switch mode settings.

Table 18 shows the control bits in Sleep mode. When Sleep mode is activated by the SWxOMODE bit, the regulator will use the set point as programmed by SWxOFF[5:0] for SW1, SW2, SW3, and SW4.

6.4.4.3 Dynamic voltage scaling

To reduce overall power consumption, processor core voltages can be varied depending on the mode or activity level of the processor.

1. Normal operation: The output voltage is selected by I^2C bits SWx[5:0] for SW1, SW2, SW3, and SW4. A voltage transition initiated by I^2C is governed by the DVS stepping rates shown in Table 26.
2. Standby Mode: The output voltage can be higher, or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by I^2C bits SWxSTBY[5:0] for SW1, SW2, SW3, and SW4. Voltage transitions initiated by a Standby event are governed by the SWxDVSSPEED[1:0] and I^2C bits shown in Table 26.
3. Sleep Mode: The output voltage can be higher or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by I^2C bits SWxOFF[5:0] for SW1, SW2, SW3, and SW4. Voltage transitions initiated by a turn-off event are governed by the SWxDVSSPEED[1:0] I^2C bits shown in Table 26.

Table 25, Table 26, summarize the set point control and DVS time stepping applied to all regulators.

Table 25. DVS control logic for SW1, SW2, SW3, and SW4

STBY	Set Point Selected by
0	SWx[5:0]
1	SWxSTBY[5:0]

Table 26. DVS speed selection for SW1, SW2, SW3, and SW4

SWxDVSSPEED[1:0]	Function
00	25 mV step each 2.0 µs
01 (default)	25 mV step each 4.0 µs
10	25 mV step each 8.0 µs
11	25 mV step each 16 µs

The regulators have a strong sourcing capability and sinking capability in PWM mode, therefore the fastest rising and falling slopes are determined by the regulator in PWM mode. However, if the regulators are programmed in PFM or APS mode during a DVS transition, the falling slope can be influenced by the load. Additionally, as the current capability in PFM mode is reduced, controlled DVS transitions in PFM mode could be affected. Critically timed DVS transitions are best assured with PWM mode operation.

The following diagram shows the general behavior for the regulators when initiated with I^2C programming, or standby control.

During the DVS period the overcurrent condition on the regulator should be masked.

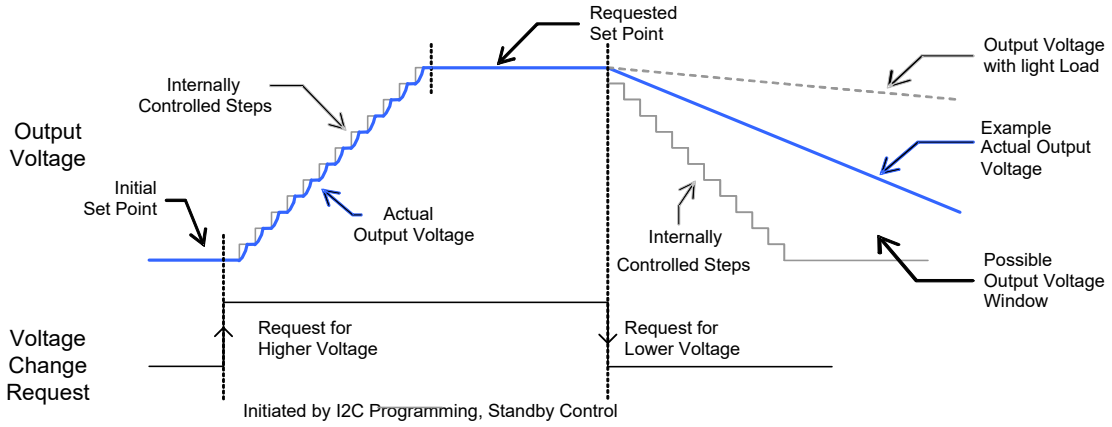


Figure 11. Voltage stepping with DVS

6.4.4.4 Regulator phase clock

The SWxPHASE[1:0] bits select the phase of the regulator clock as shown in Table 27. By default, each regulator is initialized at 90 ° out of phase with respect to each other. For example, SW1 is set to 0 °, SW2 is set to 90 °, SW3 is set to 180 °, and SW4 is set to 270 ° by default at power up.

Table 27. Regulator phase clock selection

SWxPHASE[1:0]	Phase of Clock Sent to Regulator (degrees)
00	0
01	90
10	180
11	270

The SWxFREQ[1:0] register is used to set the desired switching frequency for each one of the buck regulators. Table 29 shows the selectable options for SWxFREQ[1:0]. For each frequency, all phases will be available, this allows regulators operating at different frequencies to have different relative switching phases. However, not all combinations are practical. For example, 2.0 MHz, 90 ° and 4.0 MHz, 180 ° are the same in terms of phasing. Table 28 shows the optimum phasing when using more than one switching frequency.

Table 28. Optimum phasing

Frequencies	Optimum phasing
1.0 MHz 2.0 MHz	0 ° 180 °
1.0 MHz 4.0 MHz	0 ° 180 °
2.0 MHz 4.0 MHz	0 ° 180 °
1.0 MHz 2.0 MHz 4.0 MHz	0 ° 90 ° 90 °

Table 29. Regulator frequency configuration

SWxFREQ[1:0]	Frequency
00	1.0 MHz
01	2.0 MHz
10	4.0 MHz
11	Reserved

6.4.4.5 SW1 regulator

The SW1 is a 4.5 A regulator capable of providing an output from 0.625 to 1.875 V. Figure 12 shows a high level block diagram of the SW1 regulator.

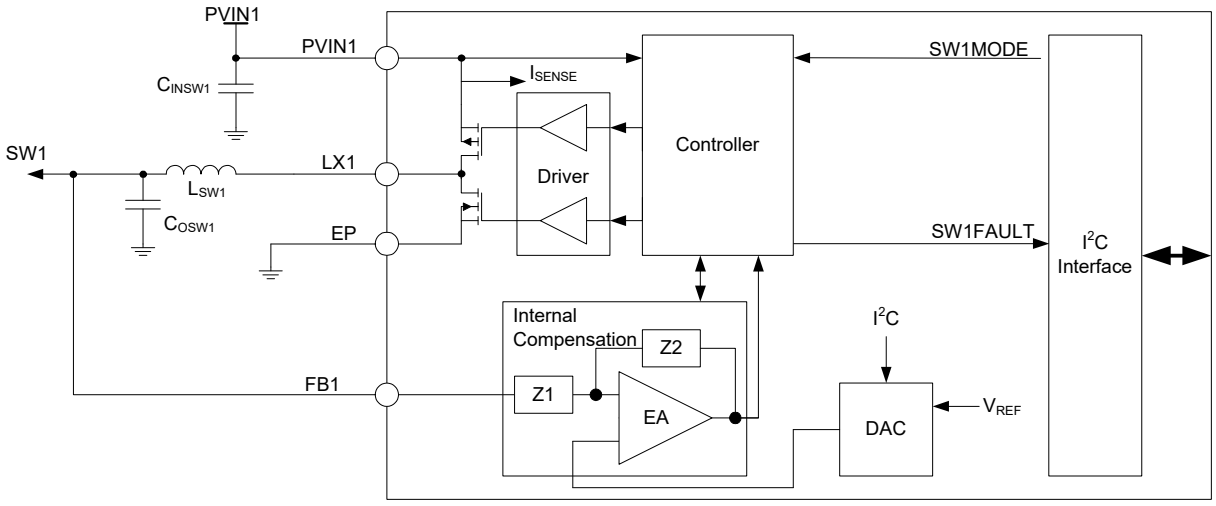


Figure 12. SW1 regulator block diagram

6.4.4.6 SW1 setup and control registers

SW1 output voltage is programmable from 0.625 to 1.875 V in steps of 25 mV. After power up in the default voltage, the output voltage can be changed in the Normal, Standby and Sleep mode by writing to the SW1[5:0], SW1STBY[5:0], and SW1OFF[5:0] respectively. Figure 30 shows the output voltage coding for these registers.

Table 30. SW1 output voltage configuration

Set point	SW1[5:0] SW1STBY[5:0] SW1OFF[5:0]	SW1 output (V)	Set point	SW1[5:0] SW1STBY[5:0] SW1OFF[5:0]	SW1 output (V)
13	001101	0.6250	39	100111	1.2750
14	001110	0.6500	40	101000	1.3000
15	001111	0.6750	41	101001	1.3250
16	010000	0.7000	42	101010	1.3500
17	010001	0.7250	43	101011	1.3750
18	010010	0.7500	44	101100	1.4000
19	010011	0.7750	45	101101	1.4250
20	010100	0.8000	46	101110	1.4500
21	010101	0.8250	47	101111	1.4750

Table 30. SW1 output voltage configuration (continued)

Set point	SW1[5:0] SW1STBY[5:0] SW1OFF[5:0]	SW1 output (V)	Set point	SW1[5:0] SW1STBY[5:0] SW1OFF[5:0]	SW1 output (V)
22	010110	0.8500	48	110000	1.5000
23	010111	0.8750	49	110001	1.5250
24	011000	0.9000	50	110010	1.5500
25	011001	0.9250	51	110011	1.5750
26	011010	0.9500	52	110100	1.6000
27	011011	0.9750	53	110101	1.6250
28	011100	1.0000	54	110110	1.6500
29	011101	1.0250	55	110111	1.6750
30	011110	1.0500	56	111000	1.7000
31	011111	1.0750	57	111001	1.7250
32	100000	1.1000	58	111010	1.7500
33	100001	1.1250	59	111011	1.7750
34	100010	1.1500	60	111100	1.8000
35	100011	1.1750	61	111101	1.8250
36	100100	1.2000	62	111110	1.8500
37	100101	1.2250	63	111111	1.8750
38	100110	1.2500			

Table 31 provides a list of registers used to configure and operate SW1 and a detailed description on each one of these register is provided in Table 31 through Table 36.

Table 31. SW1 register summary

Register	Address	Output
SW1VOLT	0x2E	SW1 Output voltage set point in normal operation
SW1STBY	0x2F	SW1 Output voltage set point in Standby
SW1OFF	0x30	SW1 Output voltage set point in Sleep
SW1MODE	0x31	SW1 Switching Mode selector register
SW1CONF	0x32	SW1 DVS, Phase, Frequency and ILIM configuration

Table 32. Register SW1VOLT - ADDR 0x2E

Name	Bit #	R/W	Default	Description
SW1	5:0	R/W	0x00	Sets the SW1 output voltage during normal operation mode. See Table 30 for all possible configurations.
UNUSED	7:6	–	0x00	UNUSED

Table 33. Register SW1STBY - ADDR 0x2F

Name	Bit #	R/W	Default	Description
SW1STBY	5:0	R/W	0x00	Sets the SW1 output voltage during Standby mode. See Table 30 for all possible configurations.
UNUSED	7:6	–	0x00	UNUSED

Table 34. Register SW1OFF - ADDR 0x30

Name	Bit #	R/W	Default	Description
SW1OFF	5:0	R/W	0x00	Sets the SW1 output voltage during Sleep mode. See Table 30 for all possible configurations.
UNUSED	7:6	–	0x00	UNUSED

Table 35. Register SW1MODE - ADDR 0x31

Name	Bit #	R/W	Default	Description
SW1MODE	3:0	R/W	0x08	Sets the SW1 switching operation mode. See Table 23 for all possible configurations.
UNUSED	4	–	0x00	UNUSED
SW1OMODE	5	R/W	0x00	Set status of SW1 when in Sleep mode 0 = OFF 1 = PFM
UNUSED	7:6	–	0x00	UNUSED

Table 36. Register SW1CONF - ADDR 0x32

Name	Bit #	R/W	Default	Description
SW1ILIM	0	R/W	0x00	SW1 current limit level selection 0 = High level current limit 1 = Low level current limit
UNUSED	1	R/W	0x00	Unused
SW1FREQ	3:2	R/W	0x00	SW1 switching frequency selector. See Table 29.
SW1PHASE	5:4	R/W	0x00	SW1 Phase clock selection. See Table 27.
SW1DVSSPEED	7:6	R/W	0x00	SW1 DVS speed selection. See Table 26.

6.4.4.7 SW1 external components

Table 37. SW1 external component recommendations

Components	Description	Component
C_{INSW1} (30)	SW1input capacitor	3 x 4.7 µF
C_{IN1HF} (30)	SW1decoupling input capacitor	3 x 0.1 µF
C_{OSW1} (30)	SW1 output capacitor	7 x 22 µF
L_{SW1}	SW1 inductor	0.68 µH, DCR = 10 mΩ, I_{SAT} = 9.0 A
Notes 30. Use X5R or X7R capacitors.		

6.4.4.8 SW1 specifications

Table 38. SW1 electrical characteristics

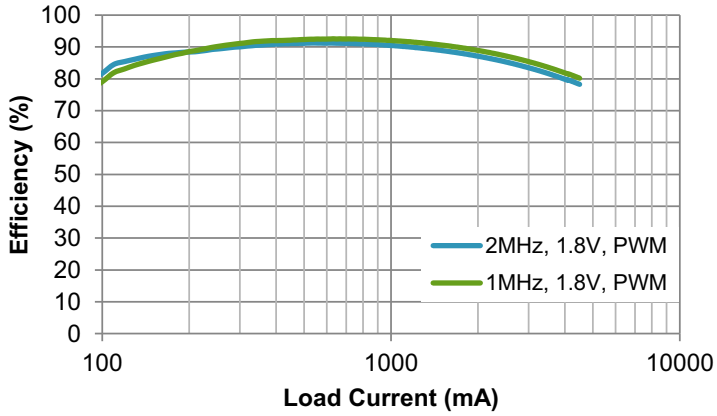
All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = V_{PVIN1} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, f_{SW1} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{PVIN1} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW1						
V_{PVIN1}	Operating Input Voltage	2.8	–	4.5	V	
V_{SW1}	Nominal Output Voltage	–	Table 30	–	V	
V_{SW1ACC}	Output Voltage Accuracy • PWM, APS, 2.8 V < V_{IN} < 4.5 V, 0 < I_{SW1} < 4.5 A 0.625 V ≤ V_{SW1} ≤ 1.450 V 1.475 V ≤ V_{SW1} ≤ 1.875 V • PFM, steady state, 2.8 V < V_{IN} < 4.5 V, 0 < I_{SW1} < 150 mA 0.625 V < V_{SW1} < 0.675 V 0.7 V < V_{SW1} < 0.85 V 0.875 V < V_{SW1} < 1.875 V	 -25 -3.0 -65 -45 -3.0	 – – – – –	 25 3.0 65 45 3.0	 mV % mV mV %	
I_{SW1}	Rated Output Load Current, 2.8 V < V_{IN} < 4.5 V, 0.625 V < V_{SW1} < 1.875 V	–	–	4500	mA	
I_{SW1LIM}	Current Limiter Peak Current Detection • Current through Inductor SW1ILIM = 0 SW1ILIM = 1	 7.1 5.3	 10.5 7.9	 13.7 10.3	 A	
V_{SW1}	Start-up Overshoot I_{SW1} = 0 mA DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN1} = 4.5 V, V_{SW1} = 1.875 V	–	–	66	mV	
t_{ONSW1}	Turn-on Time, Enable to 90% of end value I_{SW1} = 0 mA, DVS clk = 25 mV/4.0 µs, V_{IN} = V_{PVIN1} = 4.5 V, V_{SW1} = 1.875 V	–	–	500	µs	
f_{SW1}	Switching Frequency SW1FREQ[1:0] = 00 SW1FREQ[1:0] = 01 SW1FREQ[1:0] = 10	 – – –	 1.0 2.0 4.0	 – – –	MHz	
η_{SW1}	Efficiency • V_{IN} = 3.6 V, f_{SW1} = 2.0 MHz, L_{SW1} = 1.0 µH PFM, 0.9 V, 1.0 mA PFM, 1.2 V, 50 mA APS, PWM, 1.2 V, 850 mA APS, PWM, 1.2 V, 1275 mA APS, PWM, 1.2 V, 2125 mA APS, PWM, 1.2 V, 4500 mA	 – – – – – –	 77 82 86 84 80 68	 – – – – – –	 %	
ΔV_{SW1}	Output Ripple	–	5.0	–	mV	
V_{SW1LIR}	Line Regulation (APS, PWM)	–	–	20	mV	
V_{SW1LOR}	DC Load Regulation (APS, PWM)	–	–	20	mV	
$V_{SW1LOTR}$	Transient Load Regulation • Transient load = 0 to 2.25 A, di/dt = 100 mA/µs Overshoot Undershoot	 –	 –	 50	mV	

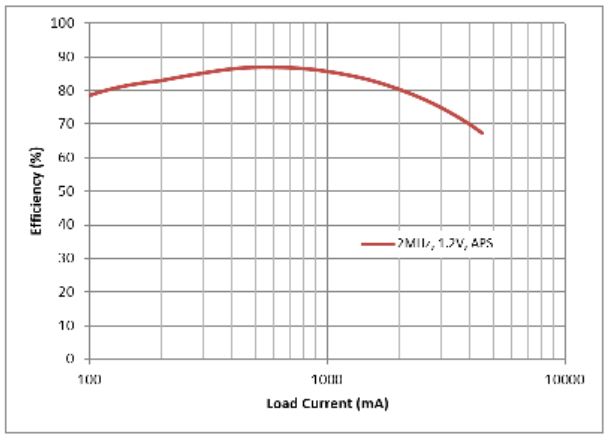
Table 38. SW1 electrical characteristics (continued)

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = V_{PVIN1} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, f_{SW1} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{PVIN1} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, and 25 °C, unless otherwise noted.

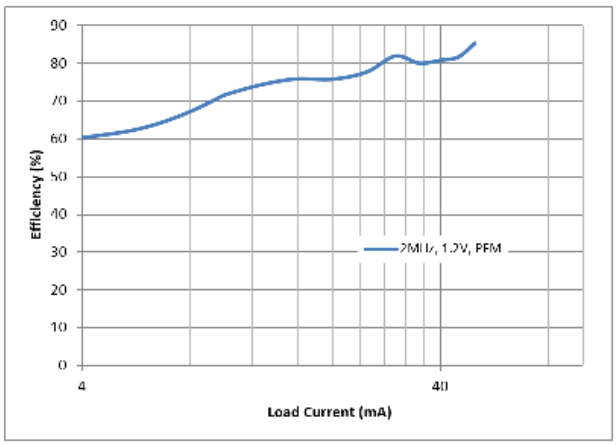
Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW1 (continued)						
I_{SW1Q}	Quiescent Current PFM Mode APS Mode	 – –	 18 145	 – –	µA	
R_{SW1DIS}	Discharge Resistance	–	600	–	Ω	
R_{ONSW1P}	SW1 P-MOSFET $R_{DS(on)}$ V_{PVIN1} = 3.3 V	–	60	77	mΩ	
R_{ONSW1N}	SW1 N-MOSFET $R_{DS(on)}$ V_{PVIN1} = 3.3 V	–	80	101	mΩ	



SW1 Efficiency Waveform: VIN = 3.3 V; VOUT = 1.8 V



SW1 Efficiency Waveform: VIN = 3.6 V; VOUT = 1.2 V



SW1 Efficiency Waveform: VIN = 3.6 V; VOUT = 1.2 V

Figure 13. SW1 efficiency waveforms

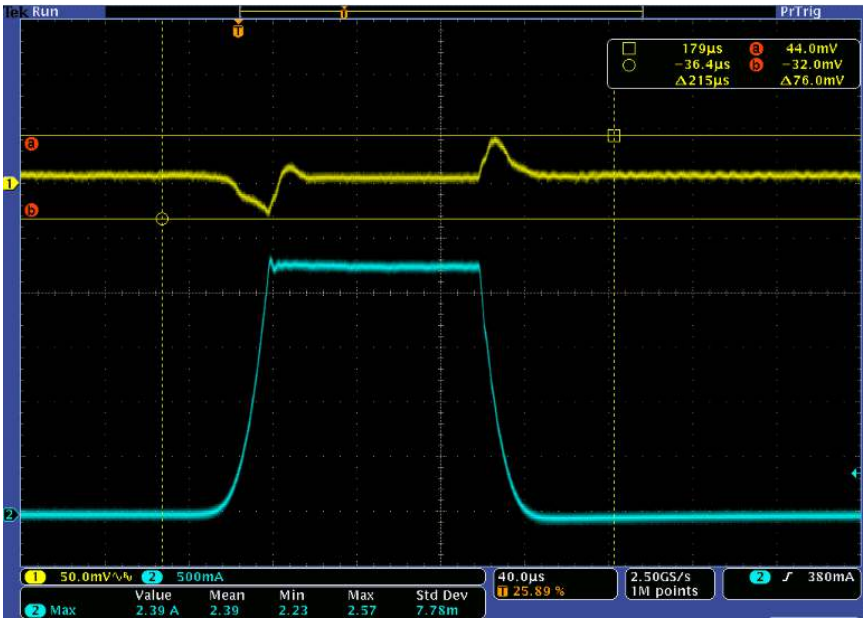


Figure 14. Load transient response – SW1 (APS)

6.4.4.9 SW2

SW2 is a 2.0 A rated buck regulator. Table 23 describes the modes, and Table 24 show the options for the SWxMODE[3:0] bits. Figure 15 shows the block diagram and the external component connections for SW2 regulator.

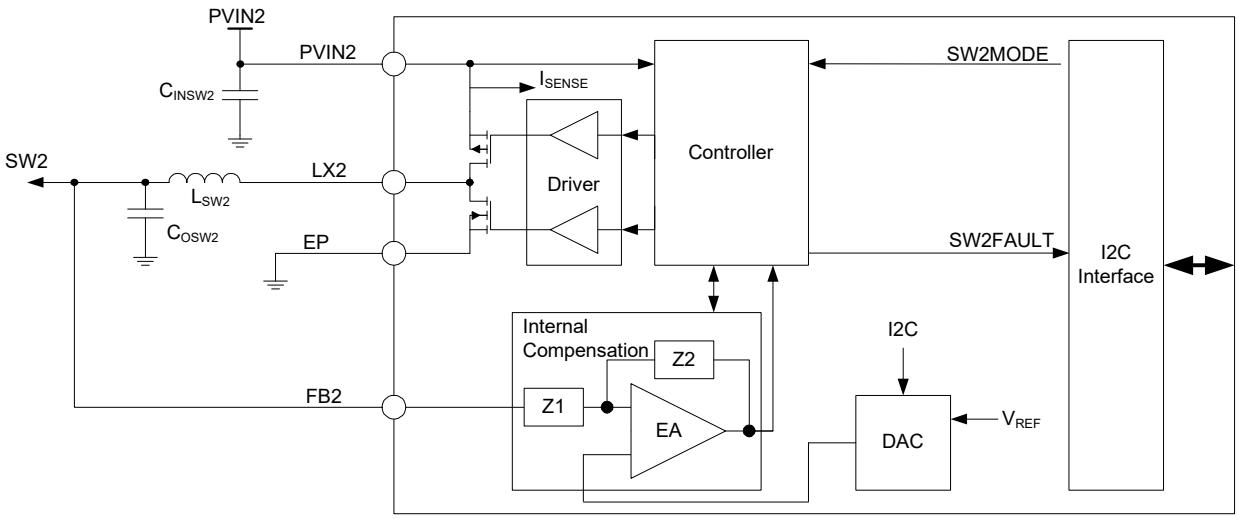


Figure 15. SW2 block diagram

6.4.4.10 SW2 setup and control registers

SW2 output voltage is programmable from 0.625 V to 3.300 V; however, bit SW2[6] in register SW2VOLT is read-only during normal operation. Its value is determined by the default configuration. Therefore, once SW2[6] is set to "0", the output is limited to the lower output voltages from 0.625 V to 1.975 V with 25 mV increments, as determined by bits SW2[5:0]. Likewise, once bit SW2[6] is set to "1", the output voltage is limited to the higher output voltage range from 0.800 V to 3.300 V with 50 mV increments, as determined by bits SW2[5:0].

In order to optimize the performance of the regulator, it is recommended only voltages from 2.000 V to 3.300 V be used in the high range, and the lower range be used for voltages from 0.625 V to 1.975 V.

The output voltage set point is independently programmed for normal, standby, and sleep mode by setting the SW2[5:0], SW2STBY[5:0] and SW2OFF[5:0] bits, respectively. However, the initial state of bit SW2[6] are copied into bits SW2STBY[6], and SW2OFF[6] bits. Therefore, the output voltage range remains the same in all three operating modes. Table 39 shows the output voltage coding valid for SW2.

Table 39. SW2 output voltage configuration

Low output voltage range[31]			High output voltage range		
Set Point	**SW2[6:0]**	**SW2 Output**	**Set Point**	**SW2[6:0]**	**SW2 Output**
0	0000000	Reserved	64	1000000	0.8000
1	0000001	Reserved	65	1000001	0.8500
2	0000010	Reserved	66	1000010	0.9000
3	0000011	Reserved	67	1000011	0.9500
4	0000100	Reserved	68	1000100	1.0000
5	0000101	Reserved	69	1000101	1.0500
6	0000110	Reserved	70	1000110	1.1000
7	0000111	Reserved	71	1000111	1.1500
8	0001000	Reserved	72	1001000	1.2000
9	0001001	0.6250	73	1001001	1.2500
10	0001010	0.6500	74	1001010	1.3000
11	0001011	0.6750	75	1001011	1.3500
12	0001100	0.7000	76	1001100	1.4000
13	0001101	0.7250	77	1001101	1.4500
14	0001110	0.7500	78	1001110	1.5000
15	0001111	0.7750	79	1001111	1.5500
16	0010000	0.8000	80	1010000	1.6000
17	0010001	0.8250	81	1010001	1.6500
18	0010010	0.8500	82	1010010	1.7000
19	0010011	0.8750	83	1010011	1.7500
20	0010100	0.9000	84	1010100	1.8000
21	0010101	0.9250	85	1010101	1.8500
22	0010110	0.9500	86	1010110	1.9000
23	0010111	0.9750	87	1010111	1.9500
24	0011000	1.0000	88	1011000	2.0000
25	0011001	1.0250	89	1011001	2.0500
26	0011010	1.0500	90	1011010	2.1000
27	0011011	1.0750	91	1011011	2.1500
28	0011100	1.1000	92	1011100	2.2000
29	0011101	1.1250	93	1011101	2.2500

Table 39. SW2 output voltage configuration(continued)

30	0011110	1.1500	94	1011110	2.3000
31	0011111	1.1750	95	1011111	2.3500
32	0100000	1.2000	96	1100000	2.4000
33	0100001	1.2250	97	1100001	2.4500
34	0100010	1.2500	98	1100010	2.5000
35	0100011	1.2750	99	1100011	2.5500
36	0100100	1.3000	100	1100100	2.6000
37	0100101	1.3250	101	1100101	2.6500
38	0100110	1.3500	102	1100110	2.7000
39	0100111	1.3750	103	1100111	2.7500
40	0101000	1.4000	104	1101000	2.8000
41	0101001	1.4250	105	1101001	2.8500
42	0101010	1.4500	106	1101010	2.9000
43	0101011	1.4750	107	1101011	2.9500
44	0101100	1.5000	108	1101100	3.0000
45	0101101	1.5250	109	1101101	3.0500
46	0101110	1.5500	110	1101110	3.1000
47	0101111	1.5750	111	1101111	3.1500
48	0110000	1.6000	112	1110000	3.2000
49	0110001	1.6250	113	1110001	3.2500
50	0110010	1.6500	114	1110010	3.3000
51	0110011	1.6750	115	1110011	Reserved
52	0110100	1.7000	116	1110100	Reserved
53	0110101	1.7250	117	1110101	Reserved
54	0110110	1.7500	118	1110110	Reserved
55	0110111	1.7750	119	1110111	Reserved
56	0111000	1.8000	120	1111000	Reserved
57	0111001	1.8250	121	1111001	Reserved
58	0111010	1.8500	122	1111010	Reserved
59	0111011	1.8750	123	1111011	Reserved
60	0111100	1.9000	124	1111100	Reserved
61	0111101	1.9250	125	1111101	Reserved
62	0111110	1.9500	126	1111110	Reserved
63	0111111	1.9750	127	1111111	Reserved

Notes
31. For voltages less than 2.0 V, only use set points 9 to 63.

Setup and control of SW2 is done through I^2C registers listed i n Table 40, and a detailed description of each one of the registers is provided in Tables 41 to Table 45.

Table 40. SW2 register summary

Register	Address	Description
SW2VOLT	0x35	Output voltage set point on normal operation
SW2STBY	0x36	Output voltage set point on Standby
SW2OFF	0x37	Output voltage set point on Sleep
SW2MODE	0x38	Switching Mode selector register
SW2CONF	0x39	DVS, Phase, Frequency, and ILIM configuration

Table 41. Register SW2VOLT - ADDR 0x35

Name	Bit #	R/W	Default	Description
SW2	5:0	R/W	0x00	Sets the SW2 output voltage during normal operation mode. See Table 39 for all possible configurations.
SW2	6	R	0x00	Sets the operating output voltage range for SW2. Set by OTP. See Table 39 for all possible configurations.
UNUSED	7	–	0X00	UNUSED

Table 42. Register SW2STBY - ADDR 0x36

Name	Bit #	R/W	Default	Description
SW2STBY	5:0	R/W	0x00	Sets the SW2 output voltage during Standby mode. See Table 39 for all possible configurations.
SW2STBY	6	R	0x00	Sets the operating output voltage range for SW2 on Standby mode. This bit inherits the value configured on bit SW2[6] by OTP. See Table 39 for all possible configurations.
UNUSED	7	–	0X00	UNUSED

Table 43. Register SW2OFF - ADDR 0x37

Name	Bit #	R/W	Default	Description
SW2OFF	5:0	R/W	0x00	Sets the SW2 output voltage during Sleep mode. See Table 39 for all possible configurations.
SW2OFF	6	R	0x00	Sets the operating output voltage range for SW2 on Sleep mode. This bit inherits the value configured on bit SW2[6] by OTP. See Table 39 for all possible configurations.
UNUSED	7	–	0X00	UNUSED

Table 44. Register SW2MODE - ADDR 0x38

Name	Bit #	R/W	Default	Description
SW2MODE	3:0	R/W	0x08	Sets the SW2 switching operation mode. See Table 23 for all possible configurations.
UNUSED	4	–	0x00	UNUSED
SW2OMODE	5	R/W	0x00	Set status of SW2 when in Sleep mode 0 = OFF 1 = PFM
UNUSED	7:6	–	0x00	UNUSED

Table 45. Register SW2CONF - ADDR 0x39

Name	Bit #	R/W	Default	Description
SW2ILIM	0	R/W	0x00	SW2 current limit level selection 0 = High level current limit 1 = Low level current limit
UNUSED	1	R/W	0x00	Unused
SW2FREQ	3:2	R/W	0x00	SW2 switching frequency selector. See Table 29.
SW2PHASE	5:4	R/W	0x00	SW2 Phase clock selection. See Table 27.
SW2DVSSPEED	7:6	R/W	0x00	SW2 DVS speed selection. See Table 28.

6.4.4.11 SW2 external components

Table 46. SW2 external component recommendations

Components	Description	Values
C_{INSW2} (32)	SW2 Input capacitor	4.7 µF
C_{IN2HF} (32)	SW2 Decoupling input capacitor	0.1 µF
C_{OSW2} (32)	SW2 Output capacitor	3 x 22 µF
L_{SW2}	SW2 Inductor	1.5 µH DCR = 50 mΩ I_{SAT} = 2.6 A

Notes
32. Use X5R or X7R capacitors.

6.4.4.12 SW2 specifications

Table 47. SW2 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = V_{PVIN2} = 3.6 V, I_{SW2} = 100 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{PVIN2} = 3.6 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2						
V_{PVIN2}	Operating Input Voltage	2.8	–	4.5	V	
V_{SW2}	Nominal Output Voltage	–	Table 39	–	V	
V_{SW2ACC}	Output Voltage Accuracy • PWM, APS, 2.8 V < V_{IN} < 4.5 V, 0 < I_{SW2} < 2.0 A 0.625 V < V_{SW2} < 0.85 V 0.875 V < V_{SW2} < 1.975 V 2.0 V < V_{SW2} < 3.3 V • PFM, 2.8 V < V_{IN} < 4.5 V, 0 < I_{SW2} ≤ 50 mA 0.625 V < V_{SW2} < 0.675 V 0.7 V < V_{SW2} < 0.85 V 0.875 V < V_{SW2} < 1.975 V 2.0 V < V_{SW2} < 3.3 V	 -25 -3.0 -6.0 -65 -45 -3.0 -3.0	 – – – – – – –	 25 3.0 6.0 65 45 3.0 3.0	 mV % % mV mV % %	

Table 47. SW2 electrical characteristics (continued)

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = V_{PVIN2} = 3.6 V, I_{SW2} = 100 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{PVIN2} = 3.6 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
I_{SW2}	Rated Output Load Current 2.8 V < V_{IN} < 4.5 V, 0.625 V < V_{SW2} < 3.3 V	–	–	2000	mA	(33)
I_{SW2LIM}	Current Limiter Peak Current Detection • Current through Inductor SW2ILIM = 0 SW2ILIM = 1	 2.8 2.1	 4.0 3.0	 5.2 3.9	A	
V_{SW2OSH}	Start-up Overshoot I_{SW2} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN2} = 4.5 V	–	–	66	mV	
tON_{SW2}	Turn-ON Time, Enable to 90% of end value I_{SW2} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN2} = 4.5 V	–	–	500	µs	
f_{SW2}	Switching Frequency SW2FREQ[1:0] = 00 SW2FREQ[1:0] = 01 SW2FREQ[1:0] = 10	 – – –	 1.0 2.0 4.0	 – – –	MHz	

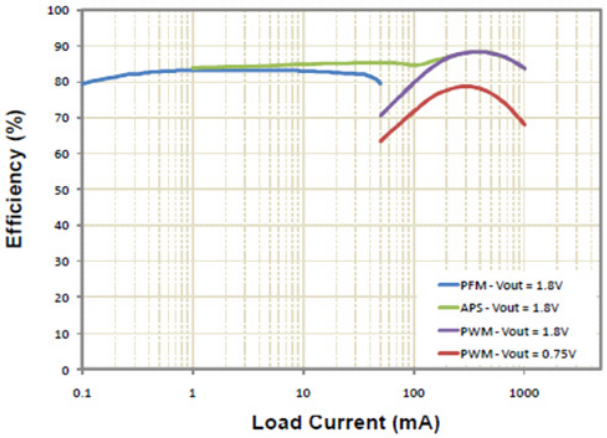
Notes

33. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (VIN_{SW2} - V_{SW2}) = I_{SW2}* (DCR of Inductor +R_{ONSW2P} + PCB trace resistance).

Table 47. SW2 electrical characteristics (continued)

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = V_{PVIN2} = 3.6 V, I_{SW2} = 100 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{PVIN2} = 3.6 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2 (continued)						
η_{SW2}	Efficiency • V_{IN} = 2.8 V, f_{SW2} = 2.0 MHz, L_{SW2} = 1.0 µH APS, PWM, 1.0 V, 1000 mA • V_{IN} = 4.5V, f_{SW2} = 2.0 MHz, L_{SW2} = 1.0 µH PFM, 1.0 V, 50 mA APS, 1.0 V, 1.0 mA APS, 1.0 V, 1000 mA • V_{IN} = 3.6V, f_{SW2} = 2.0 MHz, L_{SW2} = 1.0 µH PFM, 3.15 V, 1.0 mA PFM, 3.15 V, 50 mA APS, PWM, 3.15 V, 400 mA APS, PWM, 3.15 V, 600 mA APS, PWM, 3.15 V, 1000 mA APS, PWM, 3.15 V, 2000 mA	 – – – – – – – – – –	 77 68 68 76 94 95 96 94 92 86	 – – – – – – – – – –	% 	
ΔV_{SW2}	Output Ripple	–	5.0	–	mV	
V_{SW2LIR}	Line Regulation (APS, PWM)	–	–	20	mV	
V_{SW2LOR}	DC Load Regulation (APS, PWM)	–	–	20	mV	
$V_{SW2LOTR}$	Transient Load Regulation • Transient load = 0.0 mA to 0.5 A, di/dt = 100 mA/µs Overshoot Undershoot	 – –	 – –	 50 50	mV	
I_{SW2Q}	Quiescent Current PFM Mode APS Mode (Low output voltage settings) APS Mode (High output voltage settings)	 – – –	 23 145 305	 – – –	µA	
R_{ONSW2P}	SW2 P-MOSFET $R_{DS(on)}$ at V_{IN} = V_{PVIN2} = 3.3 V	–	190	209	mΩ	
R_{ONSW2N}	SW2 N-MOSFET $R_{DS(on)}$ at V_{IN} = V_{PVIN2} = 3.3 V	–	212	255	mΩ	
R_{SW2DIS}	Discharge Resistance	–	600	–	Ω	



SW2 Efficiency Waveform: VIN = 3.6V; VOUT = 1.8V

Figure 16. SW2 efficiency waveforms

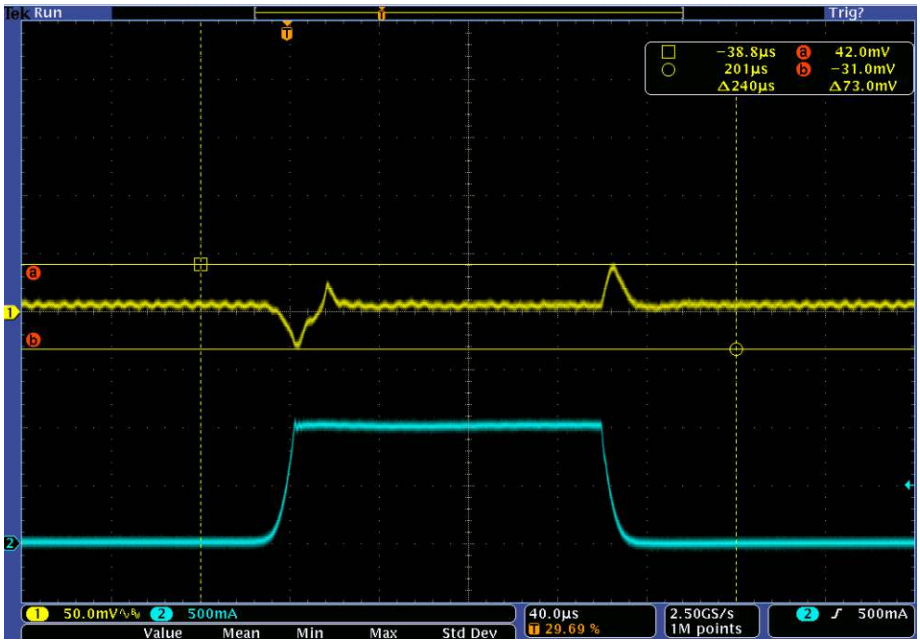


Figure 17. Load transient response – SW2 (PWM)

6.4.4.13 SW3

SW3 is a 2.5 A regulator capable of providing an output from 0.625 V to 3.3 V. Figure 18 shows a high level block diagram of the SW3 regulator.

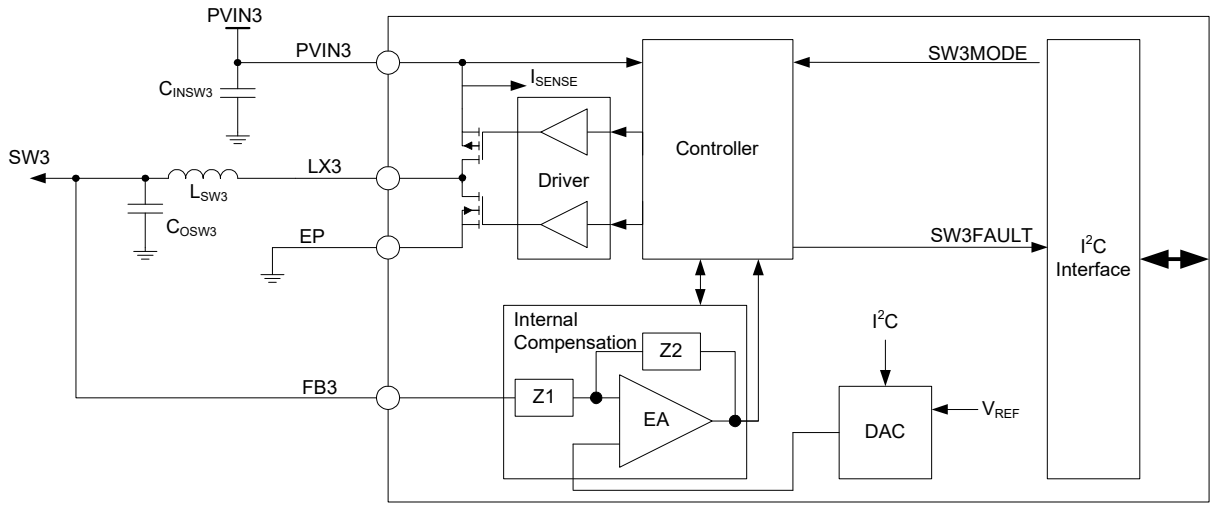


Figure 18. SW3 regulator block diagram

6.4.4.14 SW3 setup and control registers

SW3 output voltage is programmable from 0.625 V to 3.300 V; however, bit SW3 [6] in register SW3VOLT is read-only during normal operation. Its value is determined by the default configuration. Therefore, once SW3 [6] is set to “0”, the output is limited to the lower output voltages from 0.625 V to 1.975 V with 25 mV increments, as determined by bits SW3[5:0]. Likewise, once bit SW3[6] is set to "1", the output voltage is limited to the higher output voltage range from 0.800 V to 3.300 V with 50 mV increments, as determined by bits SW3[5:0].

In order to optimize the performance of the regulator, it is recommended only voltages from 2.00 V to 3.300 V be used in the high range and the lower range be used for voltages from 0.625 V to 1.975 V.

The output voltage set point is independently programmed for normal, standby, and sleep mode by setting the SW3[5:0], SW3STBY[5:0], and SW3OFF[5:0] bits respectively; however, the initial state of the SW3[6] bit is copied into the SW3STBY[6] and SW3OFF[6] bits. Therefore, the output voltage range remains the same on all three operating modes. Table 48 shows the output voltage coding valid for SW3. Table 48 shows the output voltage coding valid for SW3.

Table 48. SW3 output voltage configuration

Low output voltage range[34]			High output voltage range		
Set point	**SW3[6:0]**	**SW3 output**	**Set point**	**SW3[6:0]**	**SW3 output**
0	0000000	Reserved	64	1000000	0.8000
1	0000001	Reserved	65	1000001	0.8500
2	0000010	Reserved	66	1000010	0.9000
3	0000011	Reserved	67	1000011	0.9500
4	0000100	Reserved	68	1000100	1.0000
5	0000101	Reserved	69	1000101	1.0500
6	0000110	Reserved	70	1000110	1.1000
7	0000111	Reserved	71	1000111	1.1500
8	0001000	Reserved	72	1001000	1.2000
9	0001001	0.6250	73	1001001	1.2500
10	0001010	0.6500	74	1001010	1.3000
11	0001011	0.6750	75	1001011	1.3500
12	0001100	0.7000	76	1001100	1.4000
13	0001101	0.7250	77	1001101	1.4500

Table 48. SW3 output voltage configuration (continued)

Low output voltage range[34]			High output voltage range		
Set point	**SW3[6:0]**	**SW3 output**	**Set point**	**SW3[6:0]**	**SW3 output**
14	0001110	0.7500	78	1001110	1.5000
15	0001111	0.7750	79	1001111	1.5500
16	0010000	0.8000	80	1010000	1.6000
17	0010001	0.8250	81	1010001	1.6500
18	0010010	0.8500	82	1010010	1.7000
19	0010011	0.8750	83	1010011	1.7500
20	0010100	0.9000	84	1010100	1.8000
21	0010101	0.9250	85	1010101	1.8500
22	0010110	0.9500	86	1010110	1.9000
23	0010111	0.9750	87	1010111	1.9500
24	0011000	1.0000	88	1011000	2.0000
25	0011001	1.0250	89	1011001	2.0500
26	0011010	1.0500	90	1011010	2.1000
27	0011011	1.0750	91	1011011	2.1500
28	0011100	1.1000	92	1011100	2.2000
29	0011101	1.1250	93	1011101	2.2500
30	0011110	1.1500	94	1011110	2.3000
31	0011111	1.1750	95	1011111	2.3500
32	0100000	1.2000	96	1100000	2.4000
33	0100001	1.2250	97	1100001	2.4500
34	0100010	1.2500	98	1100010	2.5000
35	0100011	1.2750	99	1100011	2.5500
36	0100100	1.3000	100	1100100	2.6000
37	0100101	1.3250	101	1100101	2.6500
38	0100110	1.3500	102	1100110	2.7000
39	0100111	1.3750	103	1100111	2.7500
40	0101000	1.4000	104	1101000	2.8000
41	0101001	1.4250	105	1101001	2.8500
42	0101010	1.4500	106	1101010	2.9000
43	0101011	1.4750	107	1101011	2.9500
44	0101100	1.5000	108	1101100	3.0000
45	0101101	1.5250	109	1101101	3.0500
46	0101110	1.5500	110	1101110	3.1000
47	0101111	1.5750	111	1101111	3.1500
48	0110000	1.6000	112	1110000	3.2000
49	0110001	1.6250	113	1110001	3.2500
50	0110010	1.6500	114	1110010	3.3000
51	0110011	1.6750	115	1110011	Reserved

Table 48. SW3 output voltage configuration (continued)

Low output voltage range[34]			High output voltage range		
Set point	SW3[6:0]	SW3 output	Set point	SW3[6:0]	SW3 output
52	0110100	1.7000	116	1110100	Reserved
53	0110101	1.7250	117	1110101	Reserved
54	0110110	1.7500	118	1110110	Reserved
55	0110111	1.7750	119	1110111	Reserved
56	0111000	1.8000	120	1111000	Reserved
57	0111001	1.8250	121	1111001	Reserved
58	0111010	1.8500	122	1111010	Reserved
59	0111011	1.8750	123	1111011	Reserved
60	0111100	1.9000	124	1111100	Reserved
61	0111101	1.9250	125	1111101	Reserved
62	0111110	1.9500	126	1111110	Reserved
63	0111111	1.9750	127	1111111	Reserved

Notes
34. For voltages less than 2.0 V, only use set points 9 to 63.

Table 49 provides a list of registers used to configure and operate SW3. A detailed description on each of these register is provided on Tables 49 through Table 54.

Table 49. SW3 register summary

Register	Address	Output
SW3VOLT	0x3C	SW3 Output voltage set point on normal operation
SW3STBY	0x3D	SW3 Output voltage set point on Standby
SW3OFF	0x3E	SW3 Output voltage set point on Sleep
SW3MODE	0x3F	SW3 Switching mode selector register
SW3CONF	0x40	SW3 DVS, phase, frequency and ILIM configuration

Table 50. Register SW3VOLT - ADDR 0x3C

Name	Bit #	R/W	Default	Description
SW3	5:0	R/W	0x00	Sets the SW3 output voltage, during normal operation mode. See Table 48 for all possible configurations.
SW3	6	R	0x00	Sets the operating output voltage range for SW3. Set by OTP. See Table 48 for all possible configurations.
UNUSED	7	–	0x00	UNUSED

Table 51. Register SW3STBY - ADDR 0x3D

Name	Bit #	R/W	Default	Description
SW3STBY	5:0	R/W	0x00	Sets the SW3 output voltage, during Standby mode. See Table 48 for all possible configurations.
SW3	6	R	0x00	Sets the operating output voltage range for SW3 on Standby mode. This bit inherits the value configured on bit SW3[6] by OTP. See Table 48 for all possible configurations.
UNUSED	7	–	0x00	UNUSED

Table 52. Register SW3OFF - ADDR 0x3E

Name	Bit #	R/W	Default	Description
SW3OFF	5:0	R/W	0x00	Sets the SW3 output voltage during Sleep mode. See Table 48 for all possible configurations.
SW3	6	R	0x00	Sets the operating output voltage range for SW3 on Sleep mode. This bit inherits the value configured on bit SW3[6] by OTP. See Table 48 for all possible configurations.
UNUSED	7	–	0x00	UNUSED

Table 53. Register SW3MODE - ADDR 0x3F

Name	Bit #	R/W	Default	Description
SW3MODE	3:0	R/W	0x08	Sets the SW3 switching operation mode. See Table 23 for all possible configurations.
UNUSED	4	–	0x00	UNUSED
SW3OMODE	5	R/W	0x00	Set status of SW3 when in Sleep mode. 0 = OFF 1 = PFM
UNUSED	7:6	–	0x00	UNUSED

Table 54. Register SW3CONF - ADDR 0x40

Name	Bit #	R/W	Default	Description
SW3ILIM	0	R/W	0x00	SW3 current limit level selection 0 = High level current limit 1 = Low level current limit
UNUSED	1	R/W	0x00	Unused
SW3FREQ	3:2	R/W	0x00	SW3 switching frequency selector. See Table 29.
SW3PHASE	5:4	R/W	0x00	SW3 Phase clock selection. See Table 27.
SW3DVSSPEED	7:6	R/W	0x00	SW3 DVS speed selection. See Table 28.

6.4.4.15 SW3 external components

Table 55. SW3 external component requirements

Components	Description	SW3
C_{INSW3} (35)	SW3 input capacitor	2 x 4.7 µF
C_{OSW3} (35)	SW3 output capacitor	3 x 22 µF
C_{IN3HF} (35)	SW3 decoupling input capacitor	2 x 0.1 µF
L_{SW3}	SW3 inductor	1.5 µH DCR = 25 mΩ I_{SAT} = 5.0 A

Notes

35. Use X5R or X7R capacitors.

6.4.4.16 SW3 specifications

Table 56. SW3 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = V_{PVIN3} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{PVIN3} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW3						
V_{PVIN3}	Operating Input Voltage	2.8	–	4.5	V	
V_{SW3}	Nominal Output Voltage	-	Table 48	-	V	
V_{SW3ACC}	Output Voltage Accuracy • PWM, APS 2.8 V < V_{IN} < 4.5 V, 0 < I_{SW3} < 2.5 A 0.625 V < V_{SW3} < 0.85 V 0.875 V < V_{SW3} < 1.975 V 2.0 V < V_{SW3} < 3.3 V • PFM, steady state (2.8 V < V_{IN} < 4.5 V, 0 < I_{SW3} < 50 mA) 0.625 V < V_{SW3} < 0.675 V 0.7 V < V_{SW3} < 0.85 V 0.875 V < V_{SW3} < 1.975 V 2.0 V < V_{SW3} < 3.3 V	 -25 -3.0 -6.0 -65 -45 -45 -3.0	 – – – – – – –	 25 3.0 6.0 65 45 45 3.0	 mV % % mV mV mV %	
I_{SW3}	Rated Output Load Current • 2.8 V < V_{IN} < 4.5 V, 0.625 V < V_{SW3} < 3.3 V PWM, APS mode	 –	 –	 2500	mA	(36)
I_{SW3LIM}	Current Limiter Peak Current Detection • Current through inductor SW3ILIM = 0 SW3ILIM = 1	 3.5 2.7	 5.0 3.8	 6.5 4.9	A	
V_{SW3OSH}	Start-up Overshoot I_{SW3} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN3} = 4.5 V	–	–	66	mV	
t_{ONSW3}	Turn-on Time Enable to 90% of end value I_{SW3} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN3} = 4.5 V	–	–	500	µs	
f_{SW3}	Switching Frequency SW3FREQ[1:0] = 00 SW3FREQ[1:0] = 01 SW3FREQ[1:0] = 10	 – – –	 1.0 2.0 4.0	 – – –	MHz	

Notes

36. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{INSW3} - V_{SW3}) = I_{SW3}* (DCR of inductor +$R_{ONSW3xP}$ + PCB trace resistance).

Table 56. SW3 electrical characteristics (continued)

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = V_{PVIN3} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{PVIN3} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW3 (continued)						
η_{SW3}	Efficiency • f_{SW3} = 2.0 MHz, L_{SW3} 1.0 µH PFM, 1.5 V, 1.0 mA PFM, 1.5 V, 50 mA APS, PWM 1.5 V, 500 mA APS, PWM 1.5 V, 750 mA APS, PWM 1.5 V, 1250 mA APS, PWM 1.5 V, 2500 mA	 – – – – – –	 84 85 85 84 80 74	 – – – – – –	%	
ΔV_{SW3}	Output Ripple	–	5.0	–	mV	
V_{SW3LIR}	Line Regulation (APS, PWM)	–	–	20	mV	
V_{SW3LOR}	DC Load Regulation (APS, PWM)	–	–	20	mV	
$V_{SW3LOTR}$	Transient Load Regulation • Transient Load = 0.0 mA to 1.25 A, di/dt = 100 mA/µs Overshoot Undershoot	 – –	 – –	 50 50	mV	
I_{SW3Q}	Quiescent Current PFM Mode APS Mode	 – –	 22 300	 – –	µA	
R_{ONSW3P}	SW3 P-MOSFET R_{DSON} at V_{IN} = V_{PVIN3} = 3.3 V	–	108	123	mΩ	
R_{ONSW3N}	SW3 N-MOSFET R_{DSON} at V_{IN} = V_{PVIN3} = 3.3 V	–	129	163	mΩ	
R_{SW3DIS}	Discharge Resistance	–	600	–	Ω	

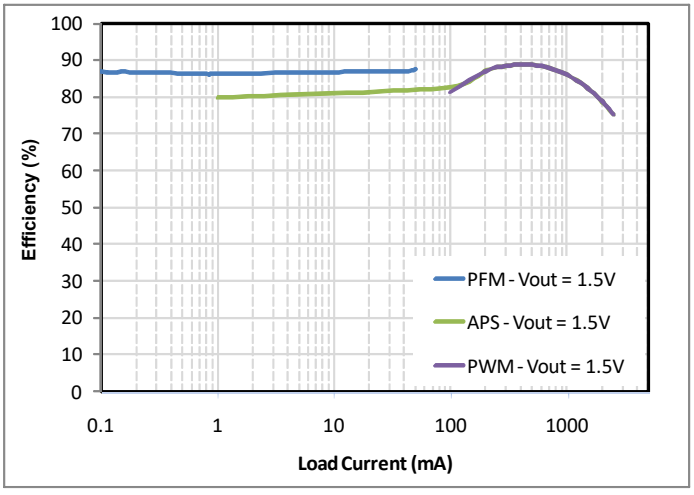


Figure 19. SW3 efficiency waveforms

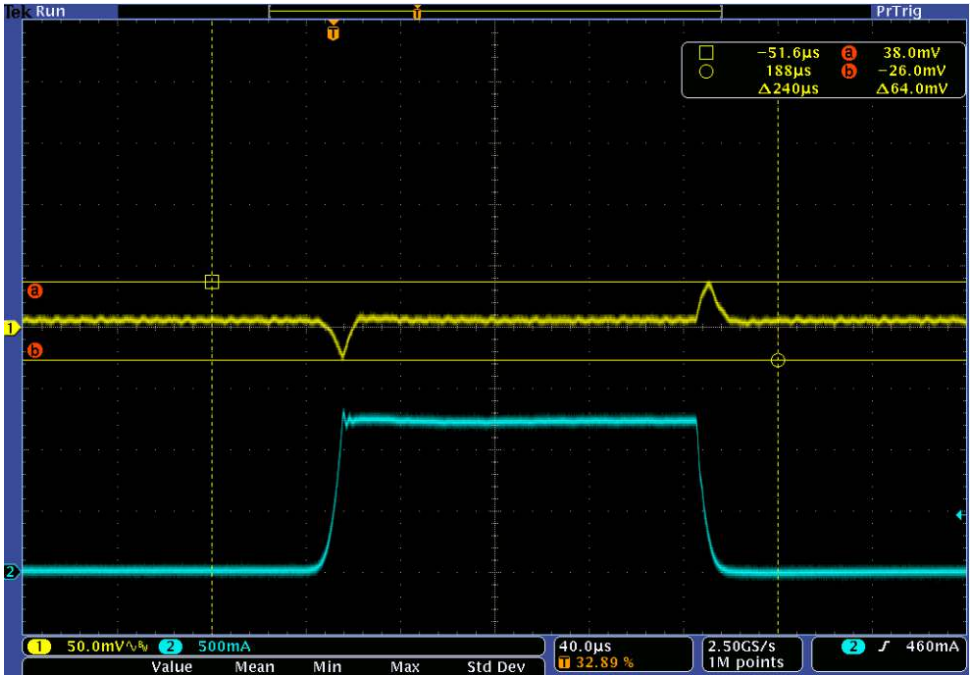


Figure 20. Load transient response – SW3 (PWM)

6.4.4.17 SW4

SW4 operates by default in VTT mode (for the 34VR500V1, V3, V4, V5, V6, V7) and it's not possible to change this configuration and modify the output voltage after the Start-up sequence. SW4 operates in non VTT mode for the 34VR500V2 and it is possible to change the output voltage by the I^2C bus.

SW4 is a 1.0 A rated buck regulator capable of operating in two modes. In Regulator mode, it operates as a normal buck regulator with a programmable output between 0.625 and 1.975 V. It is capable of operating in the three available switching modes: PFM, APS, and PWM, described on Table 23 and configured by the SW4MODE[3:0] bits, as shown in Table 24.

If the system requires DDR memory termination, SW4 can be used in its VTT mode. In the VTT mode, its reference voltage will track the output voltage of SW3, scaled by 0.5. Furthermore, when in VTT mode, only the PWM switching mode is allowed. The minimum output voltage for SW4 in VTT mode is 0.6 V

Figure 21 shows the block diagram and the external component connections for the SW4 regulator.

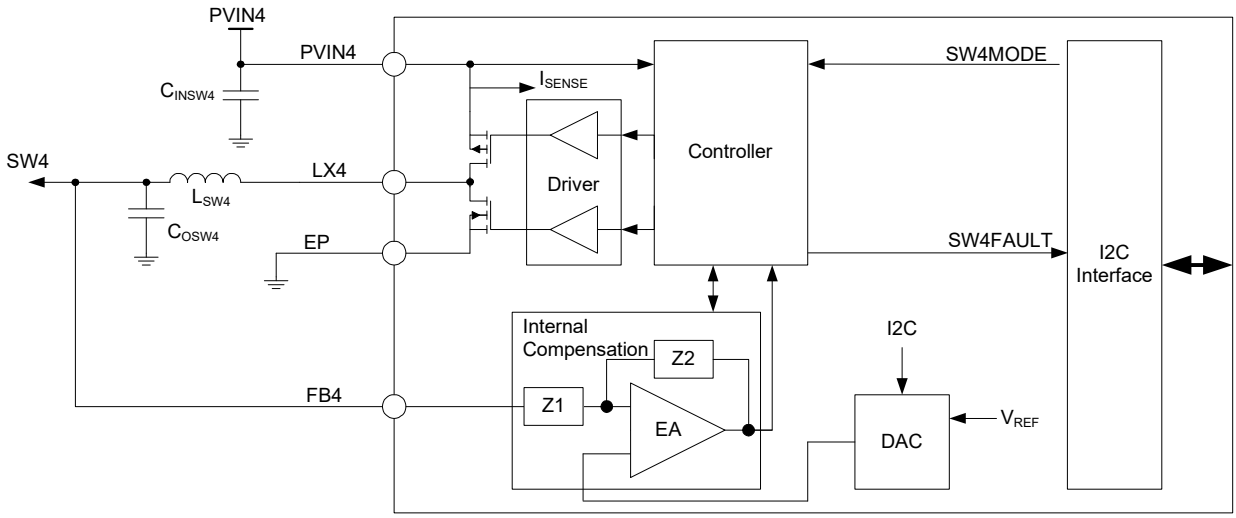


Figure 21. SW4 block diagram

6.4.4.18 SW4 setup and control registers

In Regulator mode, the SW4 output voltage is programmable from 0.625 to 1.975 V.

The output voltage set point is independently programmed for Normal, Standby, and Sleep mode by setting the SW4[5:0], SW4STBY[5:0], and SW4OFF[5:0] bits, respectively. Table 57 shows the output voltage coding valid for SW4.

Table 57. SW4 output voltage configuration

Set Point	SW4[5:0]	SW4 Output	Set Point	SW4[5:0]	SW4 Output
9	001001	0.6250	37	100101	1.3250
10	001010	0.6500	38	100110	1.3500
11	001011	0.6750	39	100111	1.3750
12	001100	0.7000	40	101000	1.4000
13	001101	0.7250	41	101001	1.4250
14	001110	0.7500	42	101010	1.4500
15	001111	0.7750	43	101011	1.4750
16	010000	0.8000	44	101100	1.5000
17	010001	0.8250	45	101101	1.5250
18	010010	0.8500	46	101110	1.5500
19	010011	0.8750	47	101111	1.5750
20	010100	0.9000	48	110000	1.6000
21	010101	0.9250	49	110001	1.6250
22	010110	0.9500	50	110010	1.6500
23	010111	0.9750	51	110011	1.6750
24	011000	1.0000	52	110100	1.7000
25	011001	1.0250	53	110101	1.7250
26	011010	1.0500	54	110110	1.7500
27	011011	1.0750	55	110111	1.7750
28	011100	1.1000	56	111000	1.8000
29	011101	1.1250	57	111001	1.8250
30	011110	1.1500	58	111010	1.8500
31	011111	1.1750	59	111011	1.8750
32	100000	1.2000	60	111100	1.9000
33	100001	1.2250	61	111101	1.9250
34	100010	1.2500	62	111110	1.9500
35	100011	1.2750	63	111111	1.9750
36	100100	1.3000			

Full setup and control of SW4 is done through the I^2C registers listed on Table 58, and a detailed description of each one of the registers is provided in Tables 59 to Table 63.

Table 58. SW4 register summary

Register	Address	Description
SW4VOLT	0x4A	Output voltage set point on normal operation
SW4STBY	0x4B	Output voltage set point on Standby
SW4OFF	0x4C	Output voltage set point on Sleep
SW4MODE	0x4D	Switching mode selector register
SW4CONF	0x4E	DVS, phase, frequency and ILIM configuration

Table 59. Register SW4VOLT - ADDR 0x4A

Name	Bit #	R/W	Default	Description
SW4	5:0	R/W	0x00	Sets the SW4 output voltage during normal operation mode. See Table 57 for all possible configurations.
UNUSED	7	–	0x00	UNUSED

Table 60. Register SW4STBY - ADDR 0x4B

Name	Bit #	R/W	Default	Description
SW4STBY	5:0	R/W	0x00	Sets the SW4 output voltage during Standby mode. See Table 57 for all possible configurations.
UNUSED	7	–	0x00	UNUSED

Table 61. Register SW4OFF - ADDR 0x4C

Name	Bit #	R/W	Default	Description
SW4OFF	5:0	R/W	0x00	Sets the SW4 output voltage during Sleep mode. See Table 57 for all possible configurations.
UNUSED	7	–	0x00	UNUSED

Table 62. Register SW4MODE - ADDR 0x4D

Name	Bit #	R/W	Default	Description
SW4MODE	3:0	R/W	0x08	Sets the SW4 switching operation mode. See Table 23 for all possible configurations.
UNUSED	4	–	0x00	UNUSED
SW4OMODE	5	R/W	0x00	Set status of SW4 when in Sleep mode 0 = OFF 1 = PFM
UNUSED	7:6	–	0x00	UNUSED

Table 63. Register SW4CONF - ADDR 0x4E

Name	Bit #	R/W	Default	Description
SW4ILIM	0	R/W	0x00	SW4 current limit level selection 0 = High level Current limit 1 = Low level Current limit
UNUSED	1	R/W	0x00	Unused
SW4FREQ	3:2	R/W	0x00	SW4 switching frequency selector. See Table 29.
SW4PHASE	5:4	R/W	0x00	SW4 Phase clock selection. See Table 27.
SW4DVSSPEED	7:6	R/W	0x00	SW4 DVS speed selection. See Table 28.

6.4.4.19 SW4 external components

Table 64. SW4 external component recommendations

Components	Description	Values
C_{INSW4} (37)	SW4 Input capacitor	4.7 µF
C_{IN4HF} (37)	SW4 Decoupling input capacitor	0.1 µF
C_{OSW4} (37)	SW4 Output capacitor	3 x 22 µF
L_{SW4}	SW4 Inductor	1.5 µH DCR = 50 mΩ I_{SAT} = 2.6 A
Notes 37. Use X5R or X7R capacitors.		

6.4.4.20 SW4 specifications

Table 65. SW4 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = V_{PVIN4} = 3.6 V, V_{SW4} = 1.8 V, I_{SW4} = 100 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, f_{SW4} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{PVIN4} = 3.6 V, V_{SW4} = 1.8 V, I_{SW4} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW4						
V_{PVIN4}	Operating Input Voltage	2.8	–	4.5	V	
V_{SW4}	Nominal Output Voltage Normal operation VTT Mode	 – –	 Table 57 $V_{SW3}/2$	 – –	 V	
V_{SW4ACC}	Output Voltage Accuracy • PWM, APS, 2.8 V < V_{IN} < 4.5 V, 0 < I_{SW4} < 1.0 A 0.625 V < V_{SW4} < 0.85 V 0.875 V < V_{SW4} < 1.975 V • PFM, steady state, 2.8 V < V_{IN} < 4.5 V, 0 < I_{SW4} < 50 mA 0.625 V < V_{SW4} < 0.675 V 0.7 V < V_{SW4} < 0.85 V 0.875 V < V_{SW4} < 1.975 V • VTT Mode, 2.8 V < V_{IN} < 4.5 V, 0 < I_{SW4} < 1.0 A	 -25 -3.0 -65 -45 -45 -40	 – – – – – –	 25 3.0 65 45 45 40	 mV % mV mV mV mV	
I_{SW4}	Rated Output Load Current 2.8 V < V_{IN} < 4.5 V, 0.625 V < V_{SW4} < 1.975 V	–	–	1000	mA	

Table 65. SW4 electrical characteristics (continued)

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = V_{PVIN4} = 3.6 V, V_{SW4} = 1.8 V, I_{SW4} = 100 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, f_{SW4} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{PVIN4} = 3.6 V, V_{SW4} = 1.8 V, I_{SW4} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW4 (continued)						
I_{SW4LIM}	Current Limiter Peak Current Detection Current through inductor SW4ILIM = 0 SW4ILIM = 1	 1.4 1.0	 2.0 1.5	 3.0 2.4	A	
V_{SW4OSH}	Start-up Overshoot I_{SW4} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN4} = 4.5 V	–	–	66	mV	
tON_{SW4}	Turn-on Time Enable to 90% of end value I_{SW4} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{PVIN4} = 4.5 V	–	–	500	µs	
f_{SW4}	Switching Frequency SW4FREQ[1:0] = 00 SW4FREQ[1:0] = 01 SW4FREQ[1:0] = 10	 – – –	 1.0 2.0 4.0	 – – –	MHz	
η_{SW4}	Efficiency • f_{SW4} = 2.0 MHz, L_{SW4} = 1.0 µH PFM, 1.8 V, 1.0 mA PFM, 1.8 V, 50 mA APS, PWM 1.8 V, 200 mA APS, PWM 1.8 V, 500 mA APS, PWM 1.8 V, 1000 mA PWM 0.75 V, 200 mA PWM 0.75 V, 500 mA PWM 0.75 V, 1000 mA	 – – – – – – – –	 81 78 87 88 83 78 76 66	 – – – – – – – –	%	
ΔV_{SW4}	Output Ripple	–	5.0	–	mV	
V_{SW4LIR}	Line Regulation (APS, PWM)	–	–	20	mV	
V_{SW4LOR}	DC Load Regulation (APS, PWM)	–	–	20	mV	
$V_{SW4LOTR}$	Transient Load Regulation • Transient Load = 0.0 mA to 500 mA, di/dt = 100 mA/µs Overshoot Undershoot	 – –	 – –	 50 50	mV	
I_{SW4Q}	Quiescent Current PFM Mode APS Mode	 – –	 22 145	 – –	µA	
R_{ONSW4P}	SW4 P-MOSFET R_{DSON} at V_{IN} = V_{PVIN4} = 3.3 V	–	236	274	mΩ	
R_{ONSW4N}	SW4 N-MOSFET R_{DSON} at V_{IN} = V_{PVIN4} = 3.3 V	–	293	378	mΩ	
R_{SW4DIS}	Discharge Resistance	–	600	–	Ω	

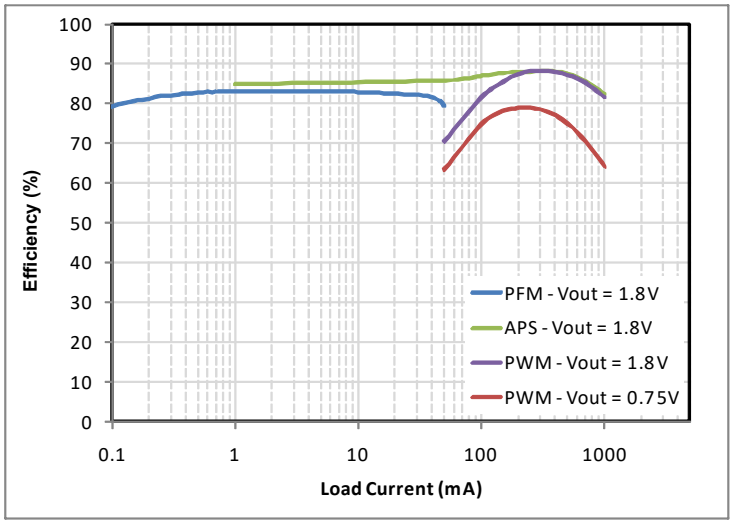


Figure 22. SW4 efficiency waveforms

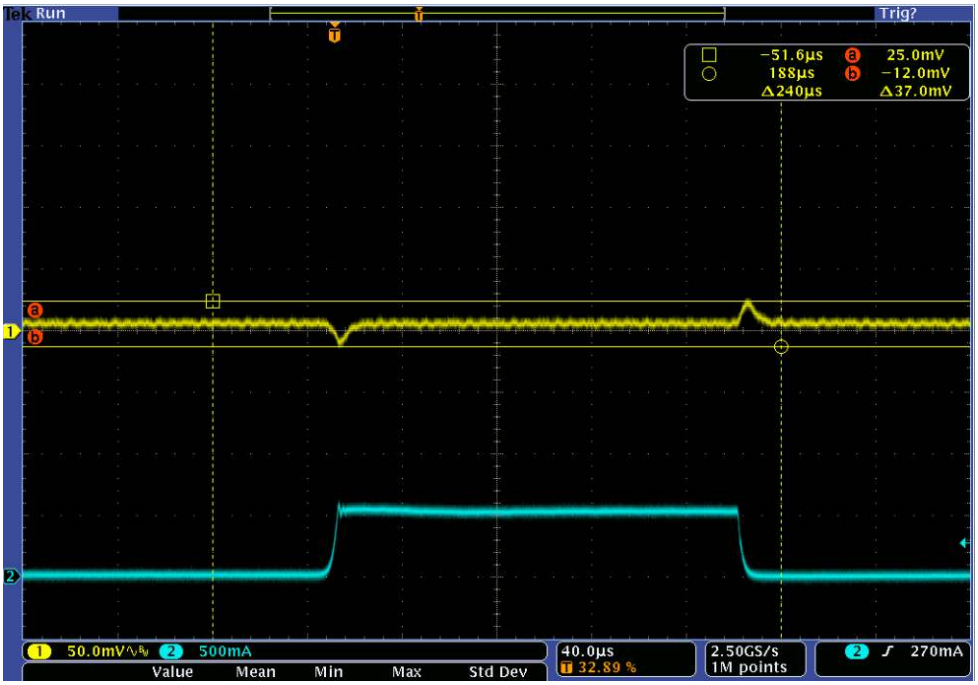


Figure 23. Load transient response – SW4 (PWM)

6.4.5 LDO regulators description

This section describes the LDO regulators provided by the 34VR500. All regulators use the main bandgap as reference. Refer to Bias and references block description section for further information on the internal reference voltages.

A Low Power mode is automatically activated by reducing bias currents when the load current is less than I_Lmax/5. However, the lowest bias currents may be attained by forcing the part into its Low Power mode by setting the LDOxLPWR bit. The use of this bit is only recommended when the load is expected to be less than I_Lmax/50, otherwise performance may be degraded.

When a regulator is disabled, the output will be discharged by an internal pull-down. The pull-down is also activated when PORB is low.

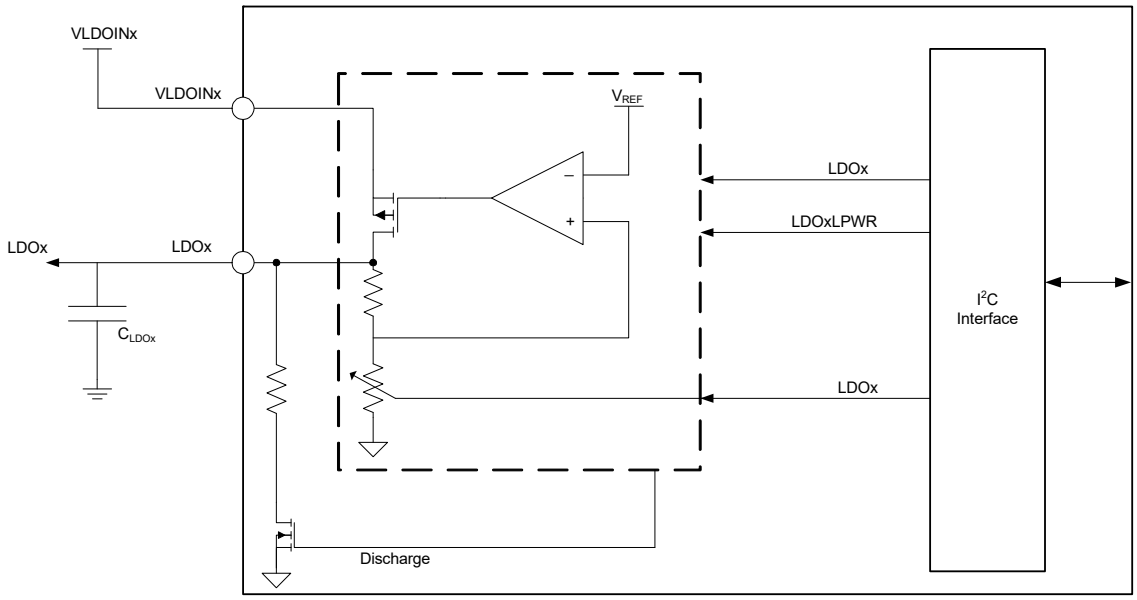
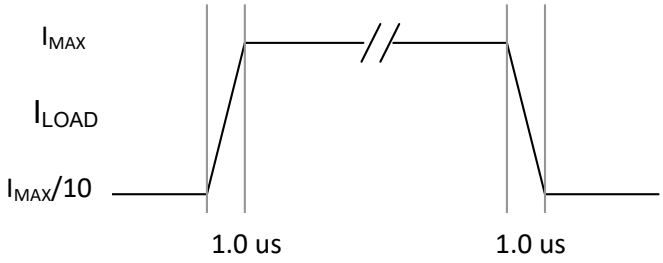


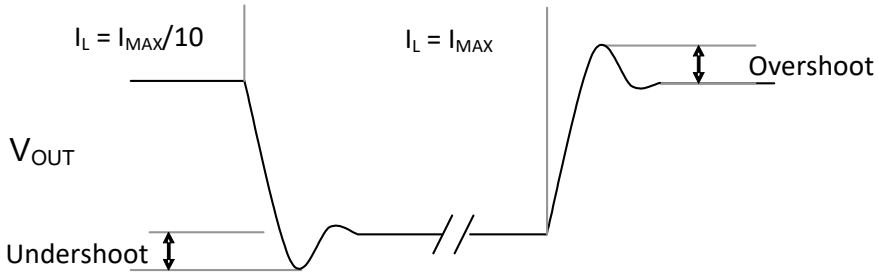
Figure 24. General LDO block diagram

6.4.5.1 Transient response waveforms

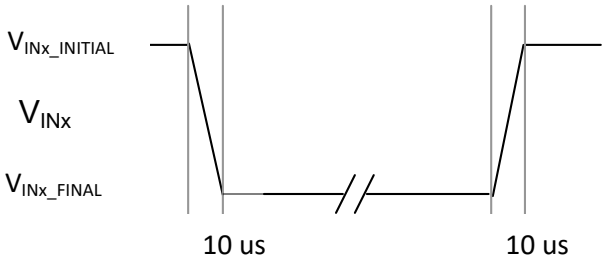
Idealized stimulus and response waveforms for transient line and transient load tests are depicted in Figure 25. Note that the transient line and load response refers to the overshoot, or undershoot only, excluding the DC shift.



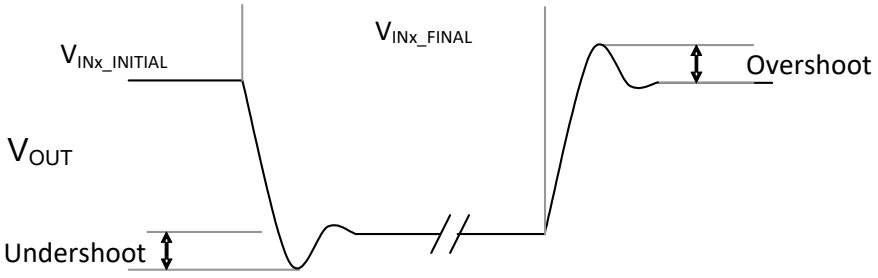
Transient Load Stimulus



V_{OUT} Transient Load Response



Transient Line Stimulus



V_{OUT} Transient Line Response

Figure 25. Transient waveforms

6.4.5.2 Short-circuit protection

All general purpose LDOs have short-circuit protection capability. The Short-circuit Protection (SCP) system includes debounced fault condition detection, regulator shutdown, and processor interrupt generation, to contain failures and minimize the chance of product damage. If a short-circuit condition is detected, the LDO will be disabled by resetting its LDOxEN bit, while at the same time, an interrupt LDOxFAULTI will be generated to flag the fault to the system processor. The LDOxFAULTI interrupt is maskable through the LDOxFAULTM mask bit.

The SCP feature is enabled by setting the REGSCPEN bit. If this bit is not set, the regulators will not automatically be disabled upon a short-circuit detection. However, the current limiter will continue to limit the output current of the regulator. By default, the REGSCPEN is not set; therefore, at start-up none of the regulators will be disabled if an overloaded condition occurs. A fault interrupt, LDOxFAULTI, will be generated in an overload condition regardless of the state of the REGSCPEN bit. See Table 66 for SCP behavior configuration.

Table 66. Short-circuit behavior

REGSCPEN[0]	Short-circuit Behavior
0	Current limit
1	Shutdown

6.4.5.3 LDO regulator control

Each LDO is fully controlled through its respective LDOxCTL register. This register enables the user to set the LDO output voltage according to Table 67 for LDO1 and uses the voltage set point on Table 68 for LDO2 through LDO5.

Table 67. LDO1 output voltage configuration

Set point	LDO1[3:0]	LDO1 output (V)
0	0000	0.800
1	0001	0.850
2	0010	0.900
3	0011	0.950
4	0100	1.000
5	0101	1.050
6	0110	1.100
7	0111	1.150
8	1000	1.200
9	1001	1.250
10	1010	1.300
11	1011	1.350
12	1100	1.400
13	1101	1.450
14	1110	1.500
15	1111	1.550

Table 68. LDO2/3/4/5 output voltage configuration

Set point	LDOx[3:0]	LDOx output (V)
0	0000	1.80
1	0001	1.90
2	0010	2.00
3	0011	2.10
4	0100	2.20
5	0101	2.30
6	0110	2.40
7	0111	2.50
8	1000	2.60
9	1001	2.70
10	1010	2.80
11	1011	2.90
12	1100	3.00
13	1101	3.10
14	1110	3.20
15	1111	3.30

Besides the output voltage configuration, the LDOs can be enabled or disabled at anytime during normal mode operation, as well as programmed to stay “ON” or be disabled when the PMIC enters Standby mode. Each regulator has associated I^2C bits for this. Table 69 presents a summary of all valid combinations of the control bits on LDOxCTL register and the expected behavior of the LDO output.

Table 69. LDO control

LDOxEN	LDOxLPWR	LDOxSTBY	STANDBY[38]	LDOxOUT
0	X	X	X	Off
1	0	0	X	On
1	1	0	X	Low Power
1	X	1	0	On
1	0	1	1	Off
1	1	1	1	Low Power

Notes

38. STANDBY refers to a Standby event as described earlier.

For more detail information, Table 70 through Table 74 provide a description of all registers necessary to operate all five general purpose LDO regulators.

Table 70. Register LDO1CTL - ADDR 0x6D

Name	Bit #	R/W	Default	Description
LDO1	3:0	R/W	0x80	Sets LDO1 output voltage. See Table 67 for all possible configurations.
LDO1EN	4	–	0x00	Enables or Disables LDO1 output 0 = OFF 1 = ON
LDO1STBY	5	R/W	0x00	Set LDO1 output state when in Standby. Refer to Table 69.
LDO1LPWR	6	R/W	0x00	Enable Low Power Mode for LDO1. Refer to Table 69.
UNUSED	7	–	0x00	UNUSED

Table 71. Register LDO2CTL - ADDR 0x6E

Name	Bit #	R/W	Default	Description
LDO2	3:0	R/W	0x80	Sets LDO2 output voltage. See Table 68 for all possible configurations.
LDO2EN	4	–	0x00	Enables or Disables LDO2 output 0 = OFF 1 = ON
LDO2STBY	5	R/W	0x00	Set LDO2 output state when in Standby. Refer to Table 69.
LDO2LPWR	6	R/W	0x00	Enable Low Power Mode for LDO2. Refer to Table 69.
UNUSED	7	–	0x00	UNUSED

Table 72. Register LDO3CTL - ADDR 0x6F

Name	Bit #	R/W	Default	Description
LDO3	3:0	R/W	0x80	Sets LDO3 output voltage. See Table 68 for all possible configurations.
LDO3EN	4	–	0x00	Enables or Disables LDO3 output 0 = OFF 1 = ON
LDO3STBY	5	R/W	0x00	Set LDO3 output state when in Standby. Refer to Table 69.
LDO3LPWR	6	R/W	0x00	Enable Low Power Mode for LDO3. Refer to Table 69.
UNUSED	7	–	0x00	UNUSED

Table 73. Register LDO4CTL - ADDR 0x70

Name	Bit #	R/W	Default	Description
LDO4	3:0	R/W	0x80	Sets LDO4 output voltage. See Table 68 for all possible configurations.
LDO4EN	4	–	0x00	Enables or Disables LDO4 output 0 = OFF 1 = ON
LDO4STBY	5	R/W	0x00	Set LDO4 output state when in Standby. Refer to Table 69.
LDO4LPWR	6	R/W	0x00	Enable Low Power Mode for LDO4. Refer to Table 69.
UNUSED	7	–	0x00	UNUSED

Table 74. Register LDO5CTL - ADDR 0x71

Name	Bit #	R/W	Default	Description
LDO5	3:0	R/W	0x80	Sets LDO5 output voltage. See Table 68 for all possible configurations.
LDO5EN	4	–	0x00	Enables or Disables LDO5 output 0 = OFF 1 = ON
LDO5STBY	5	R/W	0x00	Set LDO5 output state when in Standby. Refer to Table 69.
LDO5LPWR	6	R/W	0x00	Enable Low Power Mode for LDO5. Refer to Table 69.
UNUSED	7	–	0x00	UNUSED

6.4.5.4 External components

Table 75 lists the typical component values for the general purpose LDO regulators.

Table 75. LDO external components

Regulator	Output capacitor (μF)[39]
LDO1	4.7
LDO2	2.2
LDO3	4.7
LDO4	2.2
LDO5	2.2

Notes
39. Use X5R/X7R ceramic capacitors.

6.4.5.5 LDO specifications

6.4.5.5.1 LDO1

Table 76. LDO1 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, V_{LDOIN1} = 3.0 V, VLDO1[3:0] = 1111, I_{LDO1} = 10 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDOIN1} = 3.0 V, LDO1[3:0] = 1111, I_{LDO1} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO1						
V_{LDOIN1}	Operating Input Voltage	1.75	–	3.40	V	
$LDO1_{NOM}$	Nominal Output Voltage	–	Table 67	–	V	
I_{LDO1}	Operating Load Current	0.0	–	250	mA	
LDO1 active mode - DC						
$V_{LDO1TOL}$	Output Voltage Tolerance 1.75 V <V_{LDOIN1} < 3.4 V, 0.0 mA < I_{LDO1} < 250 mA LDO1[3:0] = 0000 to 1111	-3.0	–	3.0	%	
$V_{LDO1LOR}$	Load Regulation (V_{LDO1} at I_{LDO1} = 250 mA) - (V_{LDO1} at I_{LDO2} = 0.0 mA) For any 1.75 V <V_{LDOIN1} < 3.4 V	–	0.05	–	mV/mA	
$V_{LDO1LIR}$	Line Regulation (V_{LDO1} at V_{LDOIN1} = 3.4 V) - (V_{LDO1} at V_{LDOIN1} = 1.75 V) For any 0.0 mA < I_{LDO1} < 250 mA	–	0.50	–	mV/V	

Table 76. LDO1 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, V_{LDOIN1} = 3.0 V, VLDO1[3:0] = 1111, I_{LDO1} = 10 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDOIN1} = 3.0 V, LDO1[3:0] = 1111, I_{LDO1} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO1 active mode - DC (continued)						
$I_{LDO1LIM}$	Current Limit I_{LDO1} when LDO1 is forced to $LDO1_{NOM}$/2	305	417	510	mA	
$I_{LDO1OCP}$	Overcurrent Protection Threshold I_{LDO1} required to cause the SCP function to disable LDO when REGSCPEN = 1	290	–	500	mA	
I_{LDO1Q}	Quiescent Current No load, Change in I_{VIN} and $I_{VLDOIN1}$ When LDO1 enabled	–	16	–	µA	
LDO1 AC and transient						
$PSRR_{LDO1}$	PSRR • I_{LDO1} = 187.5 mA, 20 Hz to 20 kHz LDO1[3:0] = 0000 - 1101 LDO1[3:0] = 1110, 1111	 50 37	 60 45	 – –	dB	(40)
$NOISE_{LDO1}$	Output Noise Density • V_{LDOIN1} = 1.75 V, I_{LDO1} = 187.5 mA 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz	 – – –	 -108 -118 -124	 -100 -108 -112	dBV/√Hz	
$SLWR_{LDO1}$	Turn-On Slew Rate • 10% to 90% of end value • 1.75 V ≤ V_{LDOIN1} ≤ 3.4 V, I_{LDO1} = 0.0 mA LDO1[3:0] = 0000 to 0111 LDO1[3:0] = 1000 to 1111	 – –	 – –	 12.5 16.5	mV/µs	
t_{ONLDO1}	Turn-On Time Enable to 90% of end value, V_{LDOIN1} = 1.75 V, 3.4 V I_{LDO1} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO1}$	Turn-Off Time Disable to 10% of initial value, V_{LDOIN1} = 1.75 V I_{LDO1} = 0.0 mA	–	–	10	ms	
$LDO1_{OSHT}$	Start-up Overshoot V_{LDOIN1} = 1.75 V, 3.4 V, I_{LDO1} = 0.0 mA	–	1.0	2.0	%	
$V_{LDO1LOTR}$	Transient Load Response V_{LDOIN1} = 1.75 V, 3.4 V I_{LDO1} = 25 to 250 mA in 1.0 µs Peak of overshoot or undershoot of LDO1 with respect to final value Refer to Figure 25	–	–	3.0	%	
$V_{LDO1LITR}$	Transient Line Response I_{LDO1} = 187.5 mA $V_{LDOIN1INITIAL}$ = 1.75 V to V_{LDOIN1} = 2.25 V for LDO1[3:0] = 0000 to 1101 $V_{LDOIN1INITIAL}$ = V_{LDO1}+0.3 V to $V_{LDOIN1FINAL}$ = V_{LDO1}+0.8 V for LDO1[3:0] = 1110, 1111 Refer to Figure 25	–	5.0	8.0	mV	

Notes

40. The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test.

6.4.5.5.2 LDO2

Table 77. LDO2 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, $V_{LDOIN23}$ = 3.6 V, VLDO2[3:0] = 1111, I_{LDO2} = 10 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN23}$ = 3.6 V, LDO2[3:0] = 1111, I_{LDO2} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO2						
$V_{LDOIN23}$	Operating Input Voltage 1.8 V ≤ $LDO2_{NOM}$ ≤ 2.5 V 2.6 V ≤ $LDO2_{NOM}$ ≤ 3.3 V	2.8 $LDO2_{NOM}$+ 0.250	– –	3.6 3.6	V	(41)
$LDO2_{NOM}$	Nominal Output Voltage	–	Table 68	–	V	
I_{LDO2}	Operating Load Current	0.0	–	100	mA	
LDO2 DC						
$V_{LDO2TOL}$	Output Voltage Tolerance $V_{LDOIN23MIN}$ < $V_{LDOIN23}$ < 3.6 V 0.0 mA < I_{LDO2} < 100 mA LDO2[3:0] = 0000 to 1111	-3.0	–	3.0	%	
$V_{LDO2LOR}$	Load Regulation (V_{LDO2} at I_{LDO2} = 100 mA) - (V_{LDO2} at I_{LDO2} = 0.0 mA) For any $V_{LDOIN23MIN}$ < $V_{LDOIN23}$ < 3.6 V	–	0.07	–	mV/mA	
$V_{LDO2LIR}$	Line Regulation (V_{LDO2} at $V_{LDOIN23}$ = 3.6 V) - (V_{LDO2} at $V_{LDOIN23MIN}$) For any 0.0 mA < I_{LDO2} < 100 mA	–	0.8	–	mV/V	
$I_{LDO2LIM}$	Current Limit I_{LDO2} when LDO2 is forced to $LDO2_{NOM}$/2	127	167	200	mA	
$I_{LDO2OCP}$	Overcurrent Protection Threshold I_{LDO2} required to cause the SCP function to disable LDO when REGSCPEN = 1	120	–	200	mA	
I_{LDO2Q}	Quiescent Current No load, Change in I_{VIN} and $I_{VLDOIN23}$ When LDO2 enabled	–	13	–	µA	
LDO2 AC and transient						
$PSRR_{LDO2}$	PSRR • I_{LDO2} = 75 mA, 20 Hz to 20 kHz LDO2[3:0] = 0000 - 1110, $V_{LDOIN23}$ = $V_{LDOIN23MIN}$ + 100 mV LDO2[3:0] = 0000 - 1000, $V_{LDOIN23}$ = $LDO2_{NOM}$ + 1.0 V	 35 55	 40 60	 – –	dB	(42)
$NOISE_{LDO2}$	Output Noise Density • $V_{LDOIN23}$ = $V_{LDOIN23MIN}$, I_{LDO2} = 75 mA 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
$SLWR_{LDO2}$	Turn-On Slew Rate • 10% to 90% of end value • $V_{LDOIN23MIN}$ ≤ $V_{LDOIN23}$ ≤ 3.6 V, I_{LDO2} = 0.0 mA LDO2[3:0] = 0000 to 0011 LDO2[3:0] = 0100 to 0111 LDO2[3:0] = 1000 to 1011 LDO2[3:0] = 1100 to 1111	 – – – –	 – – – –	 22.0 26.5 30.5 34.5	mV/µs	

Table 77. LDO2 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, $V_{LDOIN23}$ = 3.6 V, VLDO2[3:0] = 1111, I_{LDO2} = 10 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN23}$ = 3.6 V, LDO2[3:0] = 1111, I_{LDO2} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO2 AC and transient (continued)						
t_{ONLDO2}	Turn-On Time Enable to 90% of end value, $V_{LDOIN23}$ = $V_{LDOIN23MIN}$, 3.6 V I_{LDO2} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO2}$	Turn-Off Time Disable to 10% of initial value, $V_{LDOIN23}$ = $V_{LDOIN23MIN}$ I_{LDO2} = 0.0 mA	–	–	10	ms	
$LDO2_{OSHT}$	Start-up Overshoot $V_{LDOIN23}$ = $V_{LDOIN23MIN}$, 3.6 V, I_{LDO2} = 0.0 mA	–	1.0	2.0	%	
$V_{LDO2LOTR}$	Transient Load Response $V_{LDOIN23}$ = $V_{LDOIN23MIN}$, 3.6 V I_{LDO2} = 10 to 100 mA in 1.0µs Peak of overshoot or undershoot of LDO2 with respect to final value. Refer to Figure 25	–	–	3.0	%	
$V_{LDO2LITR}$	Transient Line Response I_{LDO2} = 75 mA $V_{LDOIN23INITIAL}$ = 2.8 V to $V_{LDOIN23FINAL}$ = 3.3 V for LDO2[3:0] = 0000 to 0111 $V_{LDOIN23INITIAL}$ = V_{LDO2}+0.3 V to $V_{LDOIN23FINAL}$ = V_{LDO2}+0.8 V for LDO2[3:0] = 1000 to 1010 $V_{LDOIN23INITIAL}$ = V_{LDO2}+0.25 V to $V_{LDOIN23FINAL}$ = 3.6 V for LDO2[3:0] = 1011 to 1111 Refer to Figure 25	–	5.0	8.0	mV	

Notes

41. When the LDO Output voltage is set above 2.6 V, the minimum allowed input voltage needs to be at least the output voltage plus 0.25 V, for proper regulation due to the dropout voltage generated through the internal LDO transistor.
42. The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. $V_{LDOIN23MIN}$ refers to the minimum allowed input voltage for a particular output voltage.

6.4.5.5.3 LDO3

Table 78. LDO3 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, $V_{LDOIN23}$ = 3.6 V, LDO3[3:0] = 1111, I_{LDO3} = 10 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN23}$ = 3.6 V, LDO3[3:0] = 1111, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO3						
$V_{LDOIN23}$	Operating Input Voltage 1.8 V ≤ $LDO3_{NOM}$ ≤ 2.5 V 2.6 V ≤ $LDO3_{NOM}$ ≤ 3.3 V	2.8 $LDO3_{NOM}$+ 0.250	– –	3.6 3.6	V	(43)
$LDO3_{NOM}$	Nominal Output Voltage	–	Table 68	–	V	
I_{LDO3}	Operating Load Current	0.0	–	350	mA	
LDO3 DC						
$V_{LDO3TOL}$	Output Voltage Tolerance $V_{LDOIN23MIN}$ < $V_{LDOIN23}$ < 3.6 V 0.0 mA < I_{LDO3} < 350 mA LDO3[3:0] = 0000 to 1111	-3.0	–	3.0	%	
$V_{LDO3LOR}$	Load Regulation (V_{LDO3} at I_{LDO3} = 350 mA) - (V_{LDO3} at I_{LDO3} = 0.0 mA) For any $V_{LDOIN23MIN}$ < $V_{LDOIN23}$ < 3.6 V	–	0.07	–	mV/mA	
$V_{LDO3LIR}$	Line Regulation (V_{LDO3} at 3.6 V) - (V_{LDO3} at $V_{LDOIN23MIN}$) For any 0.0 mA < I_{LDO3} < 350 mA	–	0.80	–	mV/V	
$I_{LDO3LIM}$	Current Limit I_{LDO3} when LDO3 is forced to $LDO3_{NOM}$/2	435	584.5	700	mA	
$I_{LDO3OCP}$	Overcurrent Protection Threshold I_{LDO3} required to cause the SCP function to disable LDO when REGSCPEN = 1	420	–	700	mA	
I_{LDO3Q}	Quiescent Current No load, Change in I_{VIN} and $I_{VLDOIN23}$ When LDO3 enabled	–	13	–	µA	
LDO3 AC and transient						
$PSRR_{LDO3}$	PSRR • I_{LDO3} = 262.5 mA, 20 Hz to 20 kHz LDO3[3:0] = 0000 - 1110, $V_{LDOIN23}$ = $V_{LDOIN23MIN}$ + 100 mV LDO3[3:0] = 0000 - 1000, $V_{LDOIN23}$ = $LDO3_{NOM}$ + 1.0 V	 35 55	 40 60	 – –	dB	(44)
$NOISE_{LDO3}$	Output Noise Density • $V_{LDOIN23}$ = $V_{LDOIN23MIN}$, I_{LDO3} = 262.5 mA 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
$SLWR_{LDO3}$	Turn-On Slew Rate • 10% to 90% of end value • $V_{LDOIN23MIN}$ ≤ $V_{LDOIN23}$ ≤ 3.6 V, I_{LDO3} = 0.0 mA LDO3[3:0] = 0000 to 0011 LDO3[3:0] = 0100 to 0111 LDO3[3:0] = 1000 to 1011 LDO3[3:0] = 1100 to 1111	 – – – –	 – – – –	 22.0 26.5 30.5 34.5	mV/µs	

Table 78. LDO3 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, $V_{LDOIN23}$ = 3.6 V, LDO3[3:0] = 1111, I_{LDO3} = 10 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN23}$ = 3.6 V, LDO3[3:0] = 1111, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO3 AC and transient (continued)						
tON_{LDO3}	Turn-On Time Enable to 90% of end value, $V_{LDOIN23}$ = $V_{LDOIN23MIN}$, 3.6 V I_{LDO3} = 0.0 mA	60	–	500	µs	
$tOFF_{LDO3}$	Turn-Off Time Disable to 10% of initial value, $V_{LDOIN23}$ = $V_{LDOIN23MIN}$ I_{LDO3} = 0.0 mA	–	–	10	ms	
$LDO3_{OSHT}$	Start-up Overshoot $V_{LDOIN23}$ = $V_{LDOIN23MIN}$, 3.6 V, I_{LDO3} = 0.0 mA	–	1.0	2.0	%	
$V_{LDO3LOTR}$	Transient Load Response $V_{LDOIN23}$ = $V_{LDOIN23MIN}$, 3.6 V I_{LDO3} = 35 to 350 mA in 1.0 µs Peak of overshoot or undershoot of LDO3 with respect to final value. Refer to Figure 25	–	–	3.0	%	
$V_{LDO3LITR}$	Transient Line Response I_{LDO3} = 262.5 mA $V_{LDOIN23INITIAL}$ = 2.8 V to $V_{LDOIN23FINAL}$ = 3.3 V for LDO3[3:0] = 0000 to 0111 $V_{LDOIN23INITIAL}$ = V_{LDO3}+0.3 V to $V_{LDOIN23FINAL}$ = V_{LDO3}+0.8 V for LDO3[3:0] = 1000 to 1010 $V_{LDOIN23INITIAL}$ = V_{LDO3}+0.25 V to $V_{LDOIN23FINAL}$ = 3.6 V for LDO3[3:0] = 1011 to 1111 Refer to Figure 25	–	5.0	8.0	mV	

Notes

43. When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
44. The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. $V_{LDOIN23MIN}$ refers to the minimum allowed input voltage for a particular output voltage.

6.4.5.5.4 LDO4

Table 79. LDO4 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, $V_{LDOIN45}$ = 3.6 V, LDO4[3:0] = 1111, I_{LDO4} = 10 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN45}$ = 3.6 V, LDO4[3:0] = 1111, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO4						
$V_{LDOIN45}$	Operating Input Voltage 1.8 V ≤ $LDO4_{NOM}$ ≤ 2.5 V 2.6 V ≤ $LDO4_{NOM}$ ≤ 3.3 V	2.8 $LDO4_{NOM}$+ 0.250	– –	4.5 4.5	V	(45)
$LDO4_{NOM}$	Nominal Output Voltage	–	Table 68	–	V	
I_{LDO4}	Operating Load Current	0.0	–	100	mA	
LDO4 active mode – DC						
$V_{LDO4TOL}$	Output Voltage Tolerance $V_{LDOIN45MIN}$ < $V_{LDOIN45}$ < 4.5 V 0.0 mA < I_{LDO4} < 100 mA, LDO4[3:0] = 0000 to 1111	-3.0	–	3.0	%	
$V_{LDO4LOR}$	Load Regulation (V_{LDO4} at I_{LDO4} = 100 mA) - (V_{LDO4} at I_{LDO4} = 0.0 mA) For any $V_{LDOIN45MIN}$ < $V_{LDOIN45}$ < 4.5 mV	–	0.10	–	mV/mA	
$V_{LDO4LIR}$	Line Regulation (V_{LDO4} at $V_{LDOIN45}$ = 4.5 V) - (V_{LDO4} at $V_{LDOIN45MIN}$) For any 0.0 mA < I_{LDO4} < 100 mA	–	0.50	–	mV/V	
$I_{LDO4LIM}$	Current Limit I_{LDO4} when LDO4 is forced to $LDO4_{NOM}$/2	122	167	200	mA	
$I_{LDO4OCP}$	Overcurrent Protection threshold I_{LDO4} required to cause the SCP function to disable LDO when REGSCPEN = 1	120	–	200	mA	
I_{LDO4Q}	Quiescent Current No load, Change in I_{VIN} and $I_{VLDOIN45}$ When LDO4 enabled	–	13	–	µA	
LDO4 AC and transient						
$PSRR_{LDO4}$	PSRR • I_{LDO4} = 75 mA, 20 Hz to 20 kHz LDO4[3:0] = 0000 - 1111, $V_{LDOIN45}$ = $V_{LDOIN45MIN}$ + 100 mV LDO4[3:0] = 0000 - 1111, $V_{LDOIN45}$ = $LDO4_{NOM}$ + 1.0 V	 35 52	 40 60	 – –	dB	(46)
$NOISE_{LDO4}$	Output Noise Density • $V_{LDOIN45}$ = $V_{LDOIN45MIN}$, I_{LDO4} = 75 mA 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
$SLWR_{LDO4}$	Turn-On Slew Rate • 10% to 90% of end value • $V_{LDOIN45MIN}$ ≤ $V_{LDOIN45}$ ≤ 4.5 mV, I_{LDO4} = 0.0 mA LDO4[3:0] = 0000 to 0011 LDO4[3:0] = 0100 to 0111 LDO4[3:0] = 1000 to 1011 LDO4[3:0] = 1100 to 1111	 – – – –	 – – – –	 22.0 26.5 30.5 34.5	mV/µs	

Table 79. LDO4 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, $V_{LDOIN45}$ = 3.6 V, LDO4[3:0] = 1111, I_{LDO4} = 10 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN45}$ = 3.6 V, LDO4[3:0] = 1111, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO4 active mode – DC (continued)						
tON_{LDO4}	Turn-On Time Enable to 90% of end value, $V_{LDOIN45}$ = $V_{LDOIN45MIN}$, 4.5 V I_{LDO4} = 0.0 mA	60	–	500	µs	
$tOFF_{LDO4}$	Turn-Off Time Disable to 10% of initial value, $V_{LDOIN45}$ = $V_{LDOIN45MIN}$ I_{LDO4} = 0.0 mA	–	–	10	ms	
$LDO4_{OSHT}$	Start-Up Overshoot $V_{LDOIN45}$ = $V_{LDOIN45MIN}$, 4.5 V, I_{LDO4} = 0.0 mA	–	1.0	2.0	%	
$V_{LDO4LOTR}$	Transient Load Response $V_{LDOIN45}$ = $V_{LDOIN45MIN}$, 4.5 V I_{LDO4} = 10 to 100 mA in 1.0 µs Peak of overshoot or undershoot of LDO4 with respect to final value. Refer to Figure 25	–	–	3.0	%	
$V_{LDO4LITR}$	Transient Line Response I_{LDO4} = 75 mA $V_{LDOIN45INITIAL}$ = 2.8 V to $V_{LDOIN45FINAL}$ = 3.3 V for LDO4[3:0] = 0000 to 0111 $V_{LDOIN45INITIAL}$ = V_{LDO4}+0.3 V to $V_{LDOIN45FINAL}$ = V_{LDO4}+0.8 V for LDO4[3:0] = 1000 to 1111 Refer to Figure 25	-	5.0	8.0	mV	

Notes

45. When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
46. The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. $V_{LDOIN45MIN}$ refers to the minimum allowed input voltage for a particular output voltage.

6.4.5.5.5 LDO5

Table 80. LDO5 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, $V_{LDOIN45}$ = 3.6 V, LDO5[3:0] = 1111, I_{LDO5} = 10 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN45}$ = 3.6 V, LDO5[3:0] = 1111, I_{LDO5} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO5						
$V_{LDOIN45}$	Operating Input Voltage 1.8 V ≤ $LDO5_{NOM}$ ≤ 2.5 V 2.6 V ≤ $LDO5_{NOM}$ ≤ 3.3 V	2.8 $LDO5_{NOM}$+ 0.250	– –	4.5 4.5	V	(47)
$LDO5_{NOM}$	Nominal Output Voltage	–	Table 68	–	V	
I_{LDO5}	Operating Load Current	0.0	–	200	mA	
LDO5 DC						
$V_{LDO5TOL}$	Output Voltage Tolerance $V_{LDOIN45MIN}$ < $V_{LDOIN45}$ < 4.5 V, 0.0 mA < I_{LDO5} < 200 mA LDO5[3:0] = 0000 to 1111	-3.0	–	3.0	%	
$V_{LDO5LOR}$	Load Regulation (V_{LDO5} at I_{LDO5} = 200 mA) - (V_{LDO5} at I_{LDO5} = 0.0 mA) For any $V_{LDOIN45MIN}$ < $V_{LDOIN45}$ < 4.5 V	–	0.10	–	mV/mA	
$V_{LDO5LIR}$	Line Regulation (V_{LDO5} at $V_{LDOIN45}$ = 4.5 V) - (V_{LDO5} at $V_{LDOIN45MIN}$) For any 0.0 mA < I_{LDO5} < 200 mA	–	0.50	–	mV/V	
$I_{LDO5LIM}$	Current Limit I_{LDO5} when LDO5 is forced to $LDO5_{NOM}$/2	232	333	475	mA	
$I_{LDO5OCP}$	Over Current Protection Threshold I_{LDO5} required to cause the SCP function to disable LDO when REGSCPEN = 1	220	–	475	mA	
I_{LDO5Q}	Quiescent Current No load, Change in I_{VIN} and $I_{VLDOIN45}$, When LDO5 enabled	–	13	–	µA	
LDO5 AC and transient						
$PSRR_{LDO5}$	PSRR • I_{LDO5} = 150 mA, 20 Hz to 20 kHz LDO5[3:0] = 0000 - 1111, $V_{LDOIN45}$ = $V_{LDOIN45MIN}$ + 100 mV LDO5[3:0] = 0000 - 1111, $V_{LDOIN45}$ = $LDO5_{NOM}$ + 1.0 V	 35 52	 40 60	 – –	dB	(48)
$NOISE_{LDO5}$	Output Noise Density • $V_{LDOIN45}$ = $V_{LDOIN45MIN}$, I_{LDO5} = 150 mA 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
$SLWR_{LDO5}$	Turn-On Slew Rate • 10% to 90% of end value • $V_{LDOIN45MIN}$ ≤ $V_{LDOIN45}$ ≤ 4.5 V, I_{LDO5} = 0.0 mA LDO5[3:0] = 0000 to 0011 LDO5[3:0] = 0100 to 0111 LDO5[3:0] = 1000 to 1011 LDO5[3:0] = 1100 to 1111	 – – – –	 – – – –	 22.0 26.5 30.5 34.5	mV/µs	

Table 80. LDO5 electrical characteristics

All parameters are specified at T_A = -40 to 105 °C (See Table 3), V_{IN} = 3.6 V, $V_{LDOIN45}$ = 3.6 V, LDO5[3:0] = 1111, I_{LDO5} = 10 mA, V_{VBIAS} = 1.0 V ±4.0%, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDOIN45}$ = 3.6 V, LDO5[3:0] = 1111, I_{LDO5} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
LDO5 AC and transient (continued)						
t_{ONLDO5}	Turn-On Time Enable to 90% of end value, $V_{LDOIN45}$ = $V_{LDOIN45MIN}$, 4.5 V I_{LDO5} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO5}$	Turn-Off Time Disable to 10% of initial value, $V_{LDOIN45}$ = $V_{LDOIN45MIN}$ I_{LDO5} = 0.0 mA	–	–	10	ms	
$LDO5_{OSHT}$	Start-Up Overshoot $V_{LDOIN45}$ = $V_{LDOIN45MIN}$, 4.5 V, I_{LDO5} = 0 mA	–	1.0	2.0	%	
$V_{LDO5LOTR}$	Transient Load Response $V_{LDOIN45}$ = $V_{LDOIN45MIN}$, 4.5 V I_{LDO5} = 20 to 200 mA in 1.0 µs Peak of overshoot or undershoot of LDO5 with respect to final value. Refer to Figure 25	–	–	3.0	%	
$V_{LDO5LITR}$	Transient Line Response I_{LDO5} = 150 mA $V_{LDOIN45INITIAL}$ = 2.8 V to $V_{LDOIN45FINAL}$ = 3.3 V for LDO5[3:0] = 0000 to 0111 $V_{LDOIN45INITIAL}$ = V_{LDO5}+0.3 V to $V_{LDOIN45FINAL}$ = V_{LDO5}+0.8 V for LDO5[3:0] = 1000 to 1111 Refer to Figure 25	–	5.0	8.0	mV	

Notes

47. When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
48. The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. $V_{LDOIN45}$ refers to the minimum allowed input voltage for a particular output voltage.

6.5 Control interface I²C block description

The 34VR500 contains an I²C interface port which allows access by a processor, or any I²C master, to the register set. Via these registers, the resources of the IC can be controlled. The registers also provide status information about how the IC is operating.

The SCL and SDA lines should be routed away from noisy signals and planes to minimize noise pick up. To prevent reflections in the SCL and SDA traces from creating false pulses, the rise and fall times of the SCL and SDA signals must be greater than 20 ns. This can be accomplished by reducing the drive strength of the I²C master via software. It is recommended to use a drive strength of 80 Ω or higher to increase the edge times. Alternatively, this can be accomplished by using small capacitors from SCL and SDA to ground. For example, use 5.1 pF capacitors from SCL and SDA to ground for bus pull-up resistors of 4.8 kΩ.

6.5.1 I²C device ID

I²C interface protocol requires a device ID for addressing the target IC on a multi-device bus. The I²C address is set to 0x08.

6.5.2 I²C operation

The I²C mode of the interface is implemented generally following the Fast mode definition which supports up to 400 kbits/s operation (exceptions to the standard are noted to be 7-bit only addressing and no support for General Call addressing.)

The I²C interface is configured as "Slave".

Timing diagrams, electrical specifications, and further details can be found in the I²C specification, which is available for download at:

http://www.nxp.com/documents/user_manual/UM10204.pdf

I²C read operations are performed in byte increments separated by an ACK. Read operations begin with the MSB and each byte is sent out unless a STOP command or NACK is received prior to completion.

The 34VR500 only supports single-byte I²C transactions for read and write. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device responds to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NACK is received, the host should terminate the current transaction and retry the transaction.

The 34VR500 uses the "repeated start" operation for reads, as shown in Figure 27.

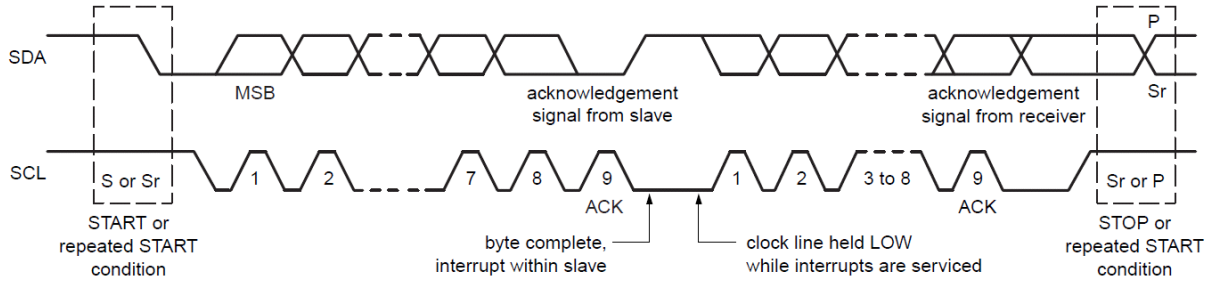


Figure 26. Data transfer on the I²C bus

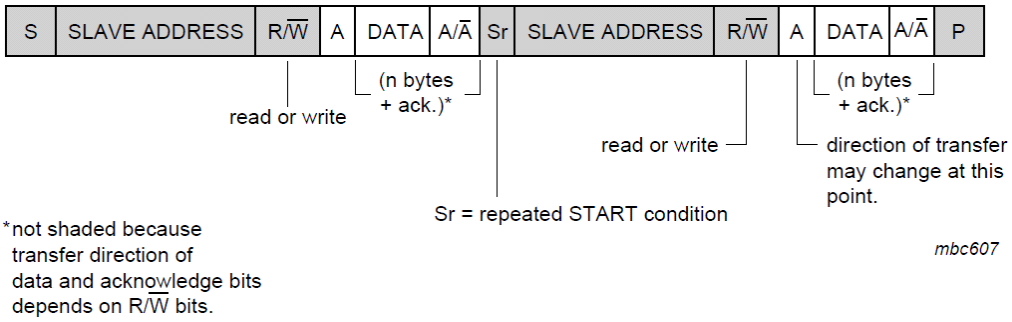


Figure 27. Read operation

6.5.3 Interrupt handling

The system is informed about important events based on interrupts. Unmasked interrupt events are signaled to the processor by driving the INTB pin low.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain set until cleared. Each interrupt can be cleared by writing a “1” to the appropriate bit in the Interrupt Status register; this will also cause the INTB pin to go high. If there are multiple interrupt bits set the INTB pin will remain low until all are either masked or cleared. If a new interrupt occurs while the processor clears an existing interrupt bit, the INTB pin will remain low.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the INTB pin will not go low. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the INTB pin will go low after unmasking.

The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable. Interrupts generated by external events are debounced; therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the INT summary Table 81. Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

6.5.4 Interrupt bit summary

Table 81 summarizes all interrupt, mask, and sense bits associated with INTB control. For more detailed behavioral descriptions, refer to the related chapters.

Table 81. Interrupt, mask and sense bits

Interrupt	Mask	Sense	Purpose	Trigger	Debounce time (ms)
LOWVINI	LOWVINM	LOWVINS	Low Input Voltage Detect Sense is 1 if below 2.80 V threshold	H to L	3.9[49]
ENI	ENM	ENS	Enable on button event	H to L	31.25[49]
			Sense is 1 if EN is high	L to H	31.25
THERM110	THERM110M	THERM110S	Thermal 110 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM120	THERM120M	THERM120S	Thermal 120 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM125	THERM125M	THERM125S	Thermal 125 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM130	THERM130M	THERM130S	Thermal 130 °C threshold Sense is 1 if above threshold	Dual	3.9
SW1FAULTI	SW1FAULTM	SW1FAULTS	Regulator 1 overcurrent limit Sense is 1 if above current limit	L to H	8.0
SW2FAULTI	SW2FAULTM	SW2FAULTS	Regulator 2 overcurrent limit Sense is 1 if above current limit	L to H	8.0
SW3FAULTI	SW3FAULTM	SW3FAULTS	Regulator 3 overcurrent limit Sense is 1 if above current limit	L to H	8.0
SW4FAULTI	SW4FAULTM	SW4FAULTS	Regulator 4 overcurrent limit Sense is 1 if above current limit	L to H	8.0
LDO1FAULTI	LDO1FAULTM	LDO1FAULTS	LDO1 overcurrent limit Sense is 1 if above current limit	L to H	8.0
LDO2FAULTI	LDO2FAULTM	LDO2FAULTS	LDO2 overcurrent limit Sense is 1 if above current limit	L to H	8.0
LDO3FAULTI	LDO3FAULTM	LDO3FAULTS	LDO3 overcurrent limit Sense is 1 if above current limit	L to H	8.0
LDO4FAULTI	LDO4FAULTM	LDO4FAULTS	LDO4 overcurrent limit Sense is 1 if above current limit	L to H	8.0
LDO5FAULTI	LDO5FAULTM	LDO5FAULTS	LDO5 overcurrent limit Sense is 1 if above current limit	L to H	8.0

Notes
49. Debounce timing for the falling edge can be extended with ENDBNC[1:0].

A full description of all interrupt, mask, and sense registers is provided in Tables 82 to 90.

Table 82. Register INTSTAT0 - ADDR 0x05

Name	Bit #	R/W	Default	Description
ENI	0	R/W1C	0	Power on interrupt bit
LOWVINI	1	R/W1C	0	Low-voltage interrupt bit
THERM110I	2	R/W1C	0	110 °C Thermal interrupt bit
THERM120I	3	R/W1C	0	120 °C Thermal interrupt bit
THERM125I	4	R/W1C	0	125 °C Thermal interrupt bit
THERM130I	5	R/W1C	0	130 °C Thermal interrupt bit

Table 83. Register INTMASK0 - ADDR 0x06

Name	Bit #	R/W	Default	Description
ENM	0	R/W1C	1	Power on interrupt mask bit
LOWVINM	1	R/W1C	1	Low-voltage interrupt mask bit
THERM110M	2	R/W1C	1	110 °C Thermal interrupt mask bit
THERM120M	3	R/W1C	1	120 °C Thermal interrupt mask bit
THERM125M	4	R/W1C	1	125 °C Thermal interrupt mask bit
THERM130M	5	R/W1C	1	130 °C Thermal interrupt mask bit

Table 84. Register INTSENSE0 - ADDR 0x07

Name	Bit #	R/W	Default	Description
ENS	0	R	0	Enable on sense bit 0 = EN low 1 = EN high
LOWVINS	1	R	0	Low voltage sense bit 0 = VIN > 2.8 V 1 = VIN ≤ 2.8 V
THERM110S	2	R	0	110 °C Thermal sense bit 0 = Below threshold 1 = Above threshold
THERM120S	3	R	0	120 °C Thermal sense bit 0 = Below threshold 1 = Above threshold
THERM125S	4	R	0	125 °C Thermal sense bit 0 = Below threshold 1 = Above threshold
THERM130S	5	R	0	130 °C Thermal sense bit 0 = Below threshold 1 = Above threshold

Table 85. Register INTSTAT1 - ADDR 0x08

Name	Bit #	R/W	Default	Description
SW1FAULTI	2:0	R/W1C	0	SW1 Overcurrent interrupt bit
SW2FAULTI	3	R/W1C	0	SW2 Overcurrent interrupt bit
SW3FAULTI	5:4	R/W1C	0	SW3 Overcurrent interrupt bit
SW4FAULTI	6	R/W1C	0	SW4 Overcurrent interrupt bit

Table 86. Register INTMASK1 - ADDR 0x09

Name	Bit #	R/W	Default	Description
SW1FAULTM	2:0	R/W	1	SW1 Overcurrent interrupt mask bit
SW2FAULTM	3	R/W	1	SW2 Overcurrent interrupt mask bit
SW3FAULTM	5:4	R/W	1	SW3 Overcurrent interrupt mask bit
SW4FAULTM	6	R/W	1	SW4 Overcurrent interrupt mask bit

Table 87. Register INTSENSE1 - ADDR 0x0A

Name	Bit #	R/W	Default	Description
SW1FAULTS	2:0	R	0	SW1 Overcurrent sense bit 0 = Normal operation 1 = Above current limit
SW2FAULTS	3	R	0	SW2 Overcurrent sense bit 0 = Normal operation 1 = Above current limit
SW3FAULTS	5:4	R	0	SW3 Overcurrent sense bit 0 = Normal operation 1 = Above current limit
SW4FAULTS	6	R	0	SW4 Overcurrent sense bit 0 = Normal operation 1 = Above current limit

Table 88. Register INTSTAT4 - ADDR 0x11

Name	Bit #	R/W	Default	Description
LDO1FAULTI	1	R/W1C	0	LDO1 Overcurrent interrupt bit
LDO2FAULTI	2	R/W1C	0	LDO2 Overcurrent interrupt bit
LDO3FAULTI	3	R/W1C	0	LDO3 Overcurrent interrupt bit
LDO4FAULTI	4	R/W1C	0	LDO4 Overcurrent interrupt bit
LDO5FAULTI	5	R/W1C	0	LDO5 Overcurrent interrupt bit

Table 89. Register INTMASK4 - ADDR 0x12

Name	Bit #	R/W	Default	Description
LDO1FAULTM	1	R/W	1	LDO1 Overcurrent interrupt mask bit
LDO2FAULTM	2	R/W	1	LDO2 Overcurrent interrupt mask bit
LDO3FAULTM	3	R/W	1	LDO3 Overcurrent interrupt mask bit
LDO4FAULTM	4	R/W	1	LDO4 Overcurrent interrupt mask bit
LDO5FAULTM	5	R/W	1	LDO5 Overcurrent interrupt mask bit

Table 90. Register INTSENSE4 - ADDR 0x13

Name	Bit #	R/W	Default	Description
LDO1FAULTS	1	R	0	LDO1 Overcurrent sense bit 0 = Normal operation 1 = Above current limit
LDO2FAULTS	2	R	0	LDO2 Overcurrent sense bit 0 = Normal operation 1 = Above current limit
LDO3FAULTS	3	R	0	LDO3 Overcurrent sense bit 0 = Normal operation 1 = Above current limit
LDO4FAULTS	4	R	0	LDO4 Overcurrent sense bit 0 = Normal operation 1 = Above current limit
LDO5FAULTS	5	R	0	LDO5 Overcurrent sense bit 0 = Normal operation 1 = Above current limit

6.5.5 Specific registers

6.5.5.1 IC and version identification

The IC and other version details can be read via identification bits. These are hard-wired on chip and described in Tables 91 to 93.

Table 91. Register DEVICEID - ADDR 0x00

Name	Bit #	R/W	Default	Description
DEVICEID	3:0	R	0x00	Die version. 0100 = 34VR500

Table 92. Register SILICON REV- ADDR 0x03

Name	Bit #	R/W	Default	Description
METAL_LAYER_REV	3:0	R	0x00	Represents the metal mask revision Pass 0.0 = 0000 . . Pass 0.15 = 1111
FULL_LAYER_REV	7:4	R	0x01	Represents the full mask revision Pass 1.0 = 0001 . . Pass 15.0 = 1111

Table 93. Register FABID - ADDR 0x04

Name	Bit #	R/W	Default	Description
FIN	1:0	R	0x00	Allows for characterizing different options within the same reticule
FAB	3:2	R	0x00	Represents the wafer manufacturing facility

6.5.6 Register bitmap

The register map is comprised of thirty-two pages, and its address and data fields are each eight bits wide. Only the first two pages can be accessed. On each page, registers 0 to 0x7F are referred to as *'functional'*, and registers 0x80 to 0xFF as *'extended'*. On each page, the functional registers are the same, but the extended registers are different. To access the Functional page from one of the extended pages, no write to the page register is necessary.

Registers that are missing in the sequence are reserved; reading from them will return a value 0x00, and writing to them will have no effect.

The contents of all registers are given in the tables defined in this chapter; each table is structure as follows:

Name: Name of the bit.

Bit #: The bit location in the register (7-0)

R/W: Read / Write access and control

- R is read-only access
- R/W is read and write access
- RW1C is read and write access with write 1 to clear

Reset: Reset signals are color coded based on the following legend.

Bits reset by VCOREDIG_PORB
Bits reset by EN or loaded default
Bits reset by DIGRESETB
Bits reset by PORB
Bits reset by VCOREDIG_PORB
Bits reset by POR or OFFB

Default: The value after reset, as noted in the Default column of the memory map.

- Fixed defaults are explicitly declared as 0 or 1.
- “X” corresponds to Read / Write bits that are initialized at start-up. Bits are subsequently I^2C modifiable, when their reset has been released. “X” may also refer to bits that may have other dependencies. For example, some bits may depend on the version of the IC, or a value from an analog block, for instance the sense bits for the interrupts.

6.5.6.1 Register map

Table 94. Functional page

				BITS[7:0]							
Add	**Register name**	**R/W**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00	DeviceID	R	8'b0001_0000	–	–	–	–	DEVICE ID [3:0]			
				0	0	0	1	0	1	0	0
03	SILICONREVID	R	8'b0001_0000	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
				0	0	0	1	0	0	0	0
04	FABID	R	8'b0000_0000	–	–	–	–	FAB[1:0]		FIN[1:0]	
				0	0	0	0	0	0	0	0
05	INTSTAT0	RW1C	8'b0000_0000	–	–	THERM130I	THERM125I	THERM120I	THERM110I	LOWVINI	ENI
				0	0	0	0	0	0	0	0
06	INTMASK0	R/W	8'b0011_1111	–	–	THERM130M	THERM125M	THERM120M	THERM110M	LOWVINM	ENM
				0	0	1	1	1	1	1	1
07	INTSENSE0	R	8'b00xx_xxxx	RSVD	RSVD	THERM130S	THERM125S	THERM120S	THERM110S	LOWVINS	ENS
				0	0	x	x	x	x	x	x

Table 94. Functional page (continued)

				BITS[7:0]							
Add	**Register name**	**R/W**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
08	INTSTAT1	RW1C	8'b0000_0000	–	SW4FAULTI	SW3FAULTI		SW2FAULTI		SW1FAULTI	
				0	0	0	0	0	0	0	0
09	INTMASK1	R/W	8'b0111_1111	–	SW4FAULTM	SW3FAULTM		SW2FAULTM		SW1FAULTM	
				0	1	1	1	1	1	1	1
0A	INTSENSE1	R	8'b0xxx_xxxx	–	SW4FAULTS	SW3FAULTS		SW2FAULTS		SW1FAULTS	
				0	x	x	x	x	x	x	x
11	INTSTAT4	RW1C	8'b0000_0000	–	–	LDO5FAULTI	LDO4FAULTI	LDO3FAULTI	LDO2FAULTI	LDO1FAULTI	–
				0	0	0	0	0	0	0	0
12	INTMASK4	R/W	8'b0011_1111	–	–	LDO5 FAULTM	LDO4 FAULTM	LDO3 FAULTM	LDO2 FAULTM	LDO1 FAULTM	–
				0	0	1	1	1	1	1	1
13	INTSENSE4	R	8'b00xx_xxxx	–	–	LDO5 FAULTS	LDO4 FAULTS	LDO3 FAULTS	LDO2 FAULTS	LDO1 FAULTS	–
				0	0	x	x	x	x	x	x
1B	PWRCTL	R/W	8'b0001_0000	REGSCPEN	STANDBYINV	STBYDLY[1:0]		ENDBNC[1:0]		ENRSTEN	RESTARTEN
				0	0	0	1	0	0	0	0
2E	SW1VOLT	R/W	8'b00xx_xxxx	–	–	SW1[5:0]					
				0	0	x	x	x	x	x	x
2F	SW1STBY	R/W	8'b00xx_xxxx	–	–	SW1STBY[5:0]					
				0	0	x	x	x	x	x	x
30	SW1OFF	R/W	8'b00xx_xxxx	–	–	SW1OFF[5:0]					
				0	0	x	x	x	x	x	x
31	SW1MODE	R/W	8'b0000_1000	–	–	SW1OMODE	–	SW1MODE[3:0]			
				0	0	0	0	1	0	0	0
32	SW1CONF	R/W	8'bxx00_xx00	SW1DVSSPEED[1:0]		SW1PHASE[1:0]		SW1FREQ[1:0]		–	SW1ILIM
				x	x	0	0	x	x	0	0
35	SW2VOLT	R/W	8'b0xxx_xxxx	–	SW2[6:0]						
				0	x	x	x	x	x	x	x
36	SW2STBY	R/W	8'b0xxx_xxxx	–	SW2STBY[6:0]						
				0	x	x	x	x	x	x	x
37	SW2OFF	R/W	8'b0xxx_xxxx	–	SW2OFF[6:0]						
				0	x	x	x	x	x	x	x
38	SW2MODE	R/W	8'b0000_1000	–	–	SW2OMODE	–	SW2MODE[3:0]			
				0	0	0	0	1	0	0	0
39	SW2CONF	R/W	8'bxx01_xx00	SW2DVSSPEED[1:0]		SW2PHASE[1:0]		SW2FREQ[1:0]		–	SW2ILIM
				x	x	0	1	x	x	0	0

Table 94. Functional page (continued)

				BITS[7:0]							
Add	**Register name**	**R/W**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
3C	SW3AVOLT	R/W	8'b0xxx_xxxx	–	SW3[6:0]						
				0	x	x	x	x	x	x	x
3D	SW3ASTBY	R/W	8'b0xxx_xxxx	–	SW3STBY[6:0]						
				0	x	x	x	x	x	x	x
3E	SW3AOFF	R/W	8'b0xxx_xxxx	–	SW3OFF[6:0]						
				0	x	x	x	x	x	x	x
3F	SW3MODE	R/W	8'b0000_1000			SW3OMODE	–	SW3MODE[3:0]			
				0	0	0	0	1	0	0	0
40	SW3CONF	R/W	8'bxx10_xx00	SW3DVSSPEED[1:0]		SW3PHASE[1:0]		SW3FREQ[1:0]		–	SW3ILIM
				x	x	1	0	x	x	0	0
4A	SW4VOLT	R/W	8'b0xxx_xxxx	–	–	SW4[5:0]					
				0	0	x	x	x	x	x	x
4B	SW4STBY	R/W	8'b0xxx_xxxx	–	–	SW4STBY[5:0]					
				0	0	x	x	x	x	x	x
4C	SW4OFF	R/W	8'b0xxx_xxxx	–	–	SW4OFF[5:0]					
				0	0	x	x	x	x	x	x
4D	SW4MODE	R/W	8'b0000_1000	–	–	SW4OMODE	–	SW4MODE[3:0]			
				0	0	0	0	1	0	0	0
4E	SW4CONF	R/W	8'bxx11_xx00	SW4DVSSPEED[1:0]		SW4PHASE[1:0]		SW4FREQ[1:0]		–	SW4ILIM
				x	x	1	1	x	x	0	0
6A	REFOUTCRTRL	R/W	8'b000x_0000	–	–	–	REFOUTEN	–	–	–	–
				0	0	0	x	0	0	0	0
6D	LDO1CTL	R/W	8'b000x_xxxx	–	LDO1LPWR	LDO1STBY	LDO1EN	LDO1[3:0]			
				0	0	0	x	x	x	x	x
6E	LDO2CTL	R/W	8'b000x_xxxx	–	LDO2LPWR	LDO2STBY	LDO2EN	LDO2[3:0]			
				0	0	0	x	x	x	x	x
6F	LDO3CTL	R/W	8'b000x_xxxx	–	LDO3LPWR	LDO3STBY	LDO3EN	LDO3[3:0]			
				0	0	0	x	x	x	x	x
70	LDO4CTL	R/W	8'b000x_xxxx	–	LDO4LPWR	LDO4STBY	LDO4EN	LDO4[3:0]			
				0	0	0	x	x	x	x	x
71	LDO5CTL	R/W	8'b000x_xxxx	–	LDO5LPWR	LDO5STBY	LDO5EN	LDO5[3:0]			
				0	0	0	x	x	x	x	x
7F	Page Register	R/W	8'b0000_0000	–	–	–	PAGE[4:0]				
				0	0	0	x	x	x	x	x

Table 95. Extended page 1: internal RAM

Address	Register name	TYPE	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
A8	SW1 VOLT	R/W	8'b00xx_xxxx	–	–	SW1_VOLT[5:0]					
				0	0	x	x	x	x	x	x
A9	SW1 SEQ	R/W	8'b000x_xxxx	–			SW1_SEQ[4:0]				
				0	0	0	x	x	x	x	x
AA	SW1 CONFIG	R/W	8'b0000_00xx	–	–	–	–	–	–	SW1_FREQ[1:0]	
				0	0	0	0	0	0	x	x
AC	SW2 VOLT	R/W	8'b0xxx_xxxx	–	SW2_VOLT[6:0]						
				0	x	x	x	x	x	x	x
AD	SW2 SEQ	R/W	8'b000x_xxxx	–	–		SW2_SEQ[4:0]				
				0	0	0	x	x	x	x	x
AE	SW2 CONFIG	R/W	8'b0000_00xx	–	–	–	–	–	–	SW2_FREQ[1:0]	
				0	0	0	0	0	0	x	x
B0	SW3 VOLT	R/W	8'b0xxx_xxxx	–	SW3A_VOLT[6:0]						
				0	x	x	x	x	x	x	x
B1	SW3 SEQ	R/W	8'b000x_xxxx	–	–		SW3_SEQ[4:0]				
				0	0	0	x	x	x	x	x
B2	SW3 CONFIG	R/W	8'b0000_xxxx	–	–	–	–	SW3_CONFIG[1:0]		SW3_FREQ[1:0]	
				0	0	0	0	x	x	x	x
B8	SW4 VOLT	R/W	8'b00xx_xxxx	–	–	SW4_VOLT[5:0]					
				0	0	x	x	x	x	x	x
B9	SW4 SEQ	R/W	8'b000x_xxxx	–	–	–	SW4_SEQ[4:0]				
				0	0	0	x	x	x	x	x
BA	SW4 CONFIG	R/W	8'b000x_xxxx	–	–	–	VTT	–	–	SW4_FREQ[1:0]	
				0	0	0	x	x	x	x	x
C4	REFOUT SEQ	R/W	8'b000x_x0xx	–	–	–	REFOUT_SEQ[4:0]				
				0	0	0	x	x	0	x	x
CC	LDO1 VOLT	R/W	8'b0000_xxxx	–	–	–	–	LDO1_VOLT[3:0]			
				0	0	0	0	x	x	x	x
CD	LDO1 SEQ	R/W	8'b000x_xxxx	–	–	–	LDO1_SEQ[4:0]				
				0	0	0	x	x	x	x	x
D0	LDO2 VOLT	R/W	8'b0000_xxxx	–	–	–	–	LDO2_VOLT[3:0]			
				0	0	0	0	x	x	x	x

Table 95. Extended page 1: internal RAM (continued)

Address	Register name	TYPE	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
D1	LDO2 SEQ	R/W	8'b000x_xxxx	–	–	–	LDO2_SEQ[4:0]				
				0	0	0	x	x	x	x	x
D4	LDO3 VOLT	R/W	8'b0000_xxxx	–	–	–	–	LDO3_VOLT[3:0]			
				0	0	0	0	x	x	x	x
D5	LDO3 SEQ	R/W	8'b000x_xxxx	–	–	–	LDO3_SEQ[4:0]				
				0	0	0	x	x	x	x	x
D8	LDO4 VOLT	R/W	8'b0000_xxxx	–	–	–	–	LDO4_VOLT[3:0]			
				0	0	0	0	x	x	x	x
D9	LDO4 SEQ	R/W	8'b000x_xxxx	–	–	–	LDO4_SEQ[4:0]				
				0	0	0	x	x	x	x	x
DC	LDO5 VOLT	R/W	8'b0000_xxxx	–	–	–	–	LDO5_VOLT[3:0]			
				0	0	0	0	x	x	x	x
DD	LDO5 SEQ	R/W	8'b000x_xxxx	–	–	–	LDO5_SEQ[4:0]				
				0	0	0	x	x	x	x	x
E0	PU CONFIG1	R/W	8'b000x_xxxx	–	–	–	PWRON_CFG1	SWDVS_CLK1[1:0]		SEQ_CLK_SPEED1[1:0]	
				0	0	0	x	x	x	x	x
E4	TBB_POR	R/W	8'b0000_00x0	TBB_POR	RSVD	–	–	–	–	RSVD	–
				0	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
E8	PWRGD EN	R/W/M	8'b0000_000x	–	–	–	–	–	–	–	PG_EN
				0	0	0	0	0	0	x	0

7 Typical applications

7.1 Introduction

Figure 28 provides a typical application diagram of the 34VR500 PMIC together with its functional components. For details on component references and additional components such as filters, refer to the individual sections.

7.1.1 Application diagram

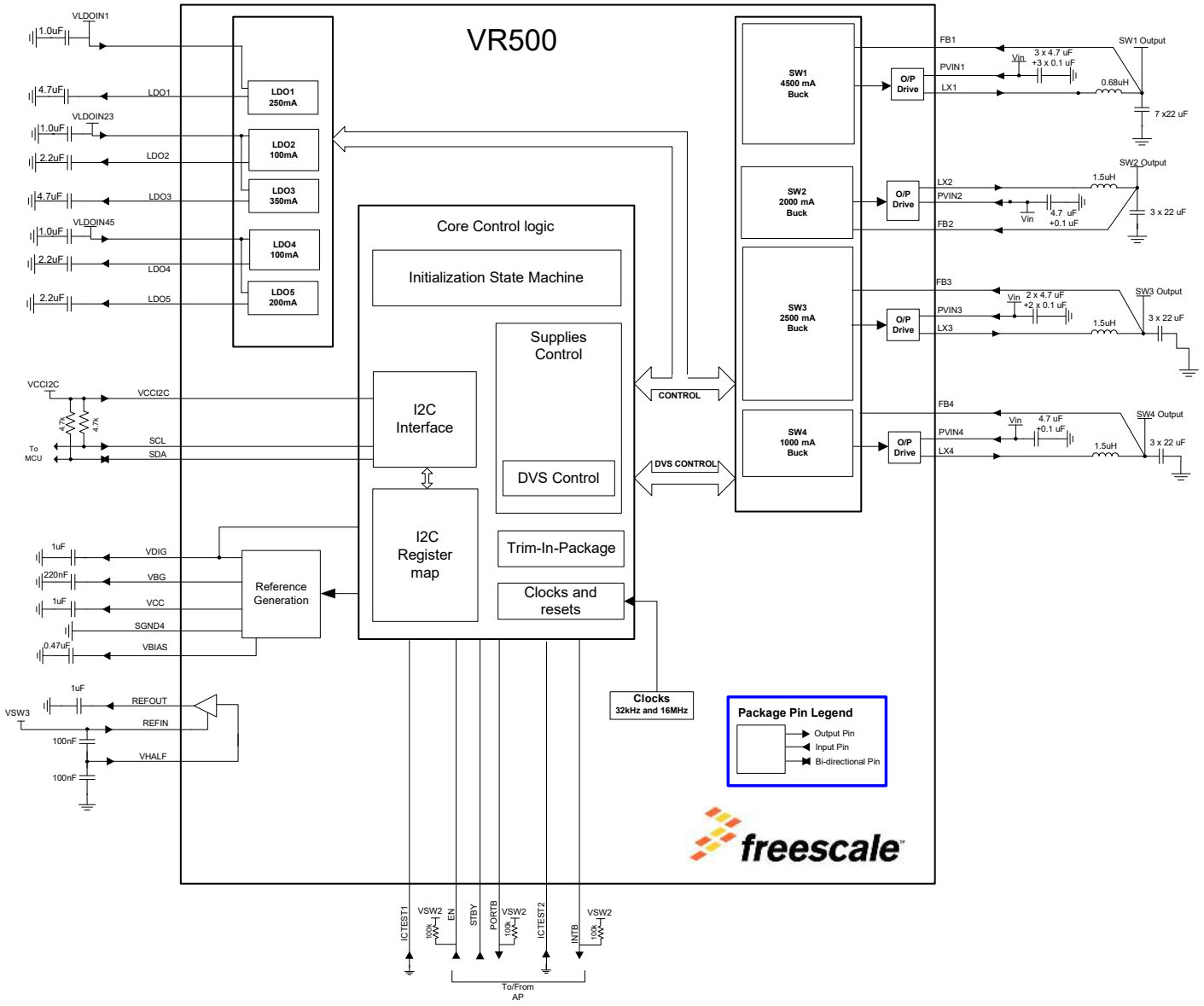


Figure 28. Typical application schematic

7.1.2 Application instructions

Table 96 provides a complete list of the recommended components on a full featured system using the 34VR500 device. Critical components such as inductors, transistors, and diodes are provided with a recommended part number, but equivalent components may be used.

7.2 Bill of materials

Table 96. Bill of materials (50)

Item	Qty	Schematic label	Value	Description	Part number	Manufacturer	Component/pin	Assy opt
Freescale components								
1	1			Power management IC	34VR500	Freescale		
BUCK, SW1 - (0.625-1.875 V), 4.5 A								
2	1		0.60 µH	4 x 4 x 2.1 I_{SAT} = 10.4 A for 30% drop, DCR_{MAX} = 10.45 mΩ	XAL4020-601ME	Coilcraft	Output Inductor	
3	6		22 µF	10 V X5R 0805	LMK212BJ226MG-T	Taiyo Yuden	Output capacitance	
4	3		4.7 µF	10 V X5R 0603	LMK107BJ475KA-T	Taiyo Yuden	Input capacitance	
5	3		0.1 µF	10 V X5R 0402	C0402C104K8PAC	Kemet	Input capacitance	
BUCK, SW2 - (0.625-3.3 V), 2.0 A								
6	1		1.5 µH	3.9 x 3.9 x 1.1 I_{SAT} = 2.6 A for 10% drop, DCR_{MAX} = 70 mΩ	LPS4012-152MR	Coilcraft	Output Inductor	
7	2		22 µF	10 V X5R 0805	LMK212BJ226MG-T	Taiyo Yuden	Output capacitance	
8	1		4.7 µF	10 V X5R 0603	LMK107BJ475KA-T	Taiyo Yuden	Input capacitance	
9	1		0.1 µF	10 V X5R 0402	C0402C104K8PAC	Kemet	Input capacitance	
BUCK, SW3 - (0.625-3.3 V), 2.5 A								
10	1		1.5 µH	4 x 4 x 2.1 I_{SAT} = 7.0 A for 10% drop, DCR_{MAX} = 21.45 mΩ	XFL4020-152ME	Coilcraft	Output Inductor	
11	–		1.5 µH	4.3 x 4.3 x 1.4 I_{SAT} = 2.9 A for 10% drop, DCR_{MAX} = 78 mΩ	LPS4014_152ML	Coilcraft	Output Inductor (Alternate)	
12	–		1.0 µH	4 x 4 x 1.2 I_{SAT} = 6.2 A, DCR = 37 mΩ	FDSD0412-H-1R0M	Toko	Output inductor (Alternate)	
13	4		22 µF	10 V X5R 0805	LMK212BJ226MG-T	Taiyo Yuden	Output capacitance	
14	2		4.7 µF	10 V X5R 0603	LMK107BJ475KA-T	Taiyo Yuden	Input capacitance	
15	1		0.1 µF	10 V X5R 0402	C0402C104K8PAC	Kemet	Input capacitance	

Table 96. Bill of materials [50] (continued)

Item	Qty	Schematic label	Value	Description	Part number	Manufacturer	Component/pin	Assy opt
BUCK, SW4 - (0.625-1.975 V), 1.0 A								
16	1		1.5 µH	3.9 x 3.9 x 1.1 I_{SAT} = 2.6 A for 10% drop, DCR_{MAX} = 70 mΩ	LPS4012-152MR	Coilcraft	Output Inductor	
17	2		22 µF	10 V X5R 0805	LMK212BJ226MG-T	Taiyo Yuden	Output capacitance	
18	1		4.7 µF	10 V X5R 0603	LMK107BJ475KA-T	Taiyo Yuden	Input capacitance	
19	1		0.1 µF	10 V X5R 0402	C0402C104K8PAC	Kemet	Input capacitance	
LDO, LDO1 - (0.80-1.55), 250 mA								
20	1		4.7 µF	6.3 V X5R 0402	C0402X5R6R3-	Venkel	Output capacitance	
LDO, LDO2 - (1.80-3.30), 100 mA								
21	1		2.2 µF	6.3 V X5R 0402	C0402C225M9PACTU	Kemet	Output capacitance	
LDO, LDO3 - (1.80-3.30), 350 mA								
22	1		4.7 µF	6.3 V X5R 0402	C0402X5R6R3-	Venkel	Output capacitance	
LDO, LDO4 - (1.80-3.30), 100 mA								
23	1		2.2 µF	6.3 V X5R 0402	C0402C225M9PACTU	Kemet	Output capacitance	
LDO, LDO5 - (1.80-3.30), 200 mA								
24	1		2.2 µF	6.3 V X5R 0402	C0402C225M9PACTU	Kemet	Output capacitance	
Reference, REFOUT - (0.60-0.90V), 10 mA								
25	1		1.0 µF	10 V X5R 0402	CC0402KRX5R6BB105	Yageo America	Output capacitance	
26	2		0.1 µF	10 V X5R 0402	C0402C104K8PAC	Kemet	VHALF, REFIN	
Internal references, VDIG, VBG, VCC								
27	1		1.0 µF	10 V X5R 0402	CC0402KRX5R6BB105	Yageo America	VDIG	
28	1		1.0 µF	10 V X5R 0402	CC0402KRX5R6BB105	Yageo America	VCC	
29	1		0.22 µF	10 V X5R 0402	GRM155R61A224KE1	Murata	VBG	
Miscellaneous								
30	1		0.1 µF	10 V X5R 0402	CD402C104K8PAC	Kemet	VCCI2C	
31	1		1.0 µF	10 V X5R 0402	CC0402KRX5R6BB105	Yageo America	VIN	
32	1		100 kΩ	1/16 W 0402	RK73H1ETTP1003F	KOA SPEER	EN	
33	1		100 kΩ	1/16 W 0402	RK73H1ETTP1003F	KOA SPEER	PORB	
34	1		100 kΩ	1/16 W 0402	RK73H1ETTP1003F	KOA SPEER	STBY	
35	1		100 kΩ	1/16 W 0402	RK73H1ETTP1003F	KOA SPEER	INTB	

Notes

50. Freescale does not assume liability, endorse, or warrant components from external manufacturers are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
51. Do not populate
52. **Critical components.** For critical components, it is vital to use the manufacturer listed.

7.3 34VR500 layout guidelines

7.3.1 General board recommendations

1. It is recommended to use an eight layer board stack-up arranged as follows:
   - High current signal
   - GND
   - Signal
   - Power
   - Power
   - Signal
   - GND
   - High current signal
2. Allocate TOP and BOTTOM PCB Layers for POWER ROUTING (high current signals), copper-pour the unused area.
3. Use internal layers sandwiched between two GND planes for the SIGNAL routing.

7.3.2 Component placement

It is desirable to keep all component related to the power stage as close to the PMIC as possible, specially decoupling input and output capacitors.

7.3.3 General routing requirements

1. Some recommended things to keep in mind for manufacturability:
   - Via in pads require a 4.5 mil minimum annular ring. Pad must be 9.0 mils larger than the hole
   - Maximum copper thickness for lines less than 5.0 mils wide is 0.6 oz copper
   - Minimum allowed spacing between line and hole pad is 3.5 mils
   - Minimum allowed spacing between line and line is 3.0 mils
2. Care must be taken with FBx pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high power signals, like the ones on the PVINx, SWx, and LXx pins. They could be also shielded.
3. Shield feedback traces of the regulators and keep them as short as possible (trace them on the bottom so the ground and power planes shield these traces).
4. Avoid coupling traces between important signal/low noise supplies (like VBG, VCC, VDIG) from any switching node (i.e. LX1, LX2, LX3, and LX4).
5. Make sure that all components related to a specific block are referenced to the corresponding ground.

7.3.4 Parallel routing requirements

1. I^2C signal routing
   - CLK is the fastest signal of the system, so it must be given special care.
   - To avoid contamination of these delicate signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the whole signal trace length.

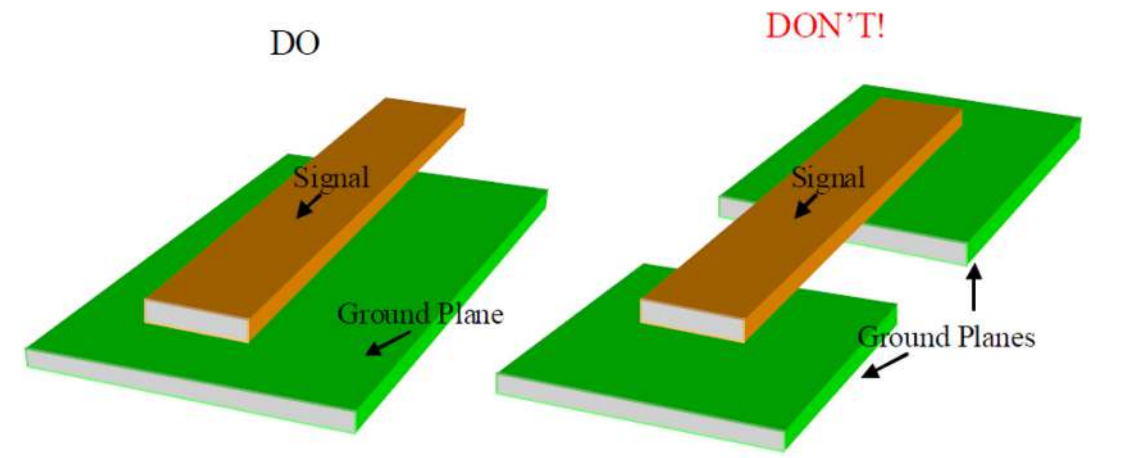


Figure 29. Recommended shielding for critical signals

   - These signals can be placed on an outer layer of the board to reduce their capacitance with respect to the ground plane.
   - Care must be taken with these signals not to contaminate analog signals, as they are high frequency signals. Another good practice is to trace them perpendicularly on different layers, so there is a minimum area of proximity between signals.

7.3.5 Switching regulator layout recommendations

1. Per design, the switching regulators in 34VR500 are designed to operate with only one input bulk capacitor. However, it is recommended to add a high frequency filter input capacitor (CIN_hf), to filter out any noise at the regulator input. This capacitor should be in the range of 100 nF and should be placed right next to or under the IC, closest to the IC pins.
2. Make high-current ripple traces low-inductance (short, high W/L ratio).
3. Make high-current traces wide or copper islands.

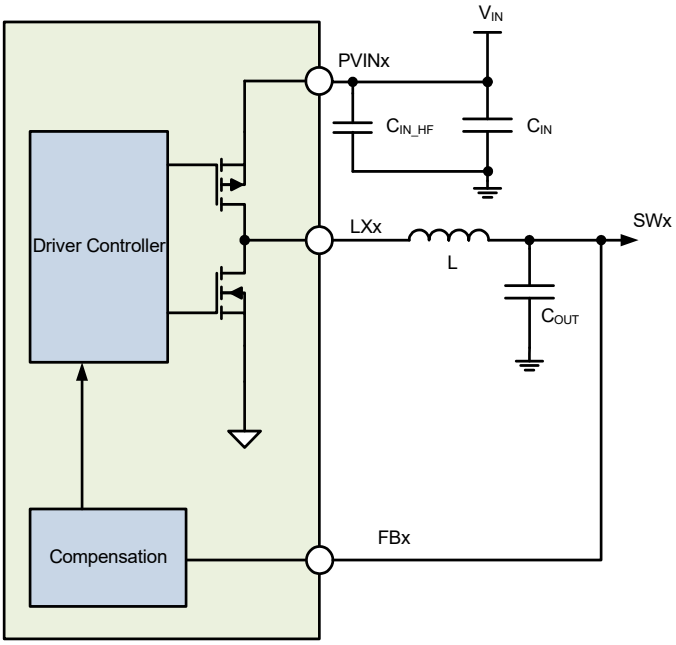


Figure 30. Generic buck regulator architecture

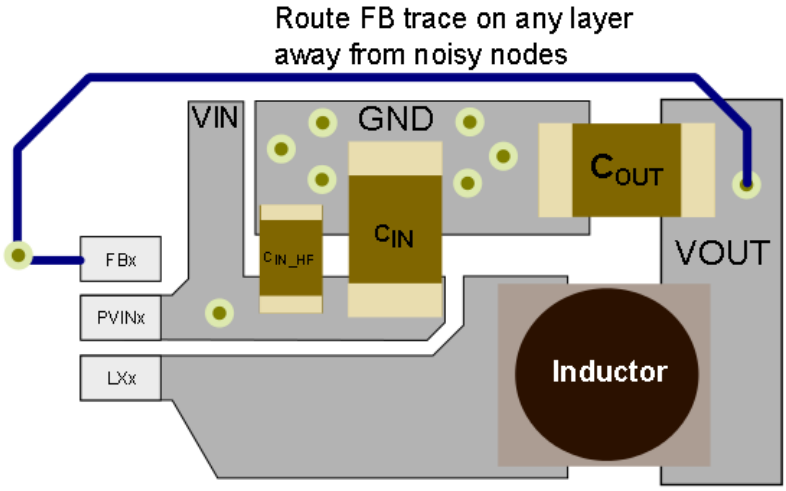


Figure 31. Layout example for buck regulators

7.4 Thermal information

7.4.1 Rating data

The thermal rating data of the packages has been simulated with the results listed in Table 4.

Junction to Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol $R_{\theta JA}$ or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. $R_{\theta JMA}$ or θJMA (Theta-JMA) will be used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, Theta-JA, will continue to be commonly used.

The JEDEC standards can be consulted at http://www.jedec.org.

7.4.2 Estimation of junction temperature

An estimation of the chip junction temperature T_J can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

with:

T_A = Ambient temperature for the package in °C

$R_{\theta JA}$ = Junction to ambient thermal resistance in °C/W

P_D = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board $R_{\theta JA}$ and the value obtained on a four layer board $R_{\theta JMA}$. Actual application PCBs show a performance close to the simulated four layer board value although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

At a known board temperature, the junction temperature T_J is estimated using the following equation

$T_J = T_B + (R_{\theta JB} \times P_D)$ with

T_B = Board temperature at the package perimeter in °C

$R_{\theta JB}$ = Junction to board thermal resistance in °C/W

P_D = Power dissipation in the package in W

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made.

See Functional block requirements and behaviors for more details on thermal management.

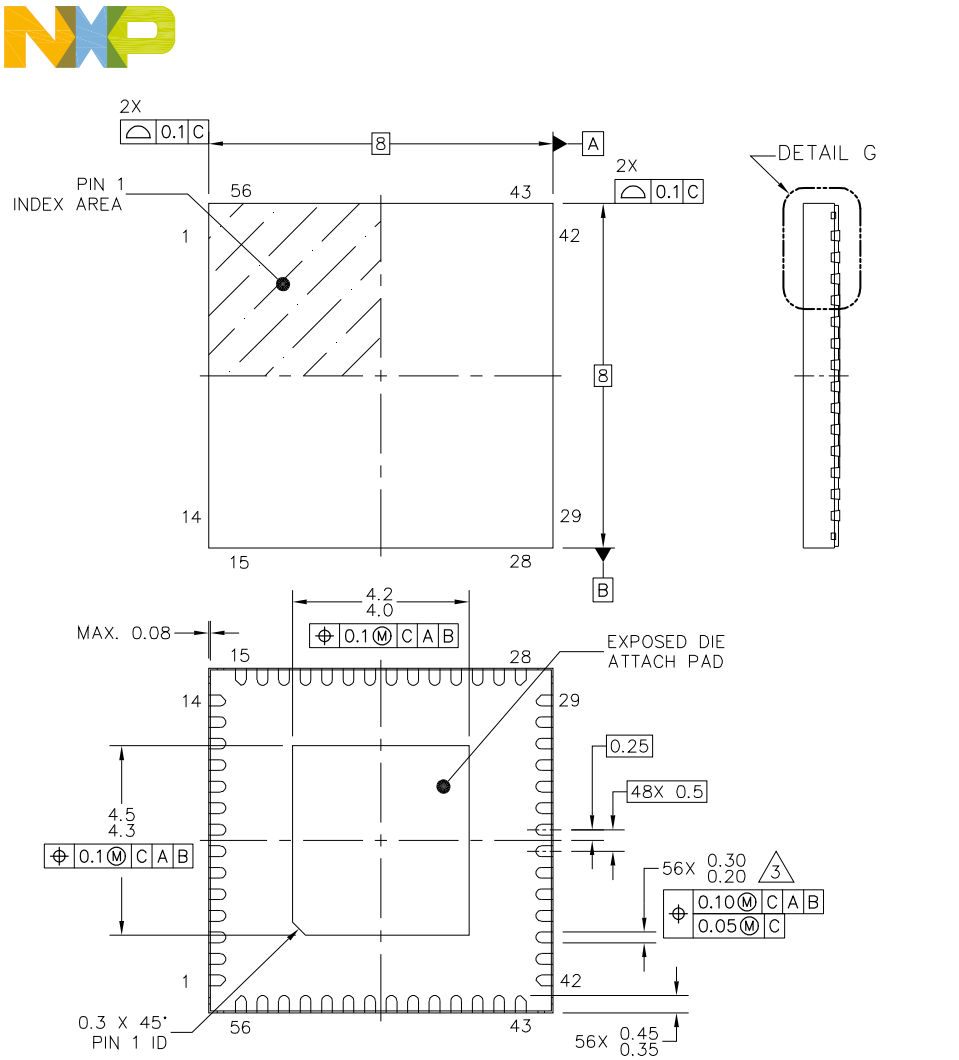
8 Packaging

8.1 Packaging dimensions

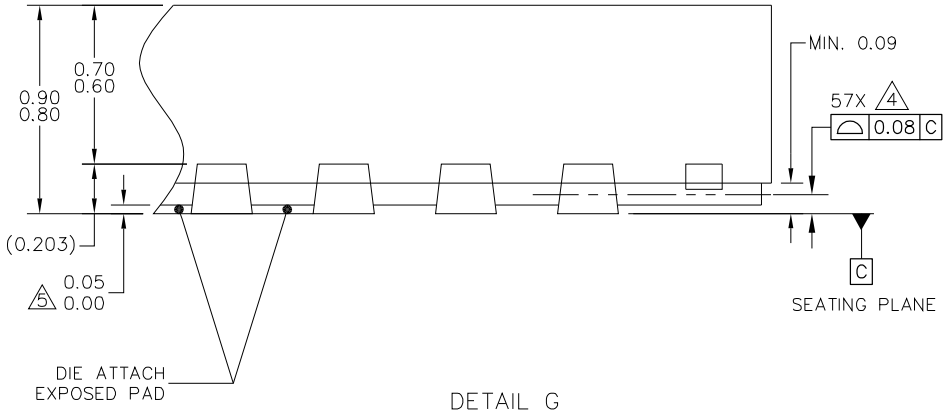
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number. See the Thermal characteristics section for specific thermal characteristics for each package.

Table 97. Package drawing information

Package	Suffix	Package outline drawing number
56 QFN 8x8 mm - 0.5 mm pitch. WF-Type (wettable flank)	ES	98ASA00589D



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: QFN, THERMALLY ENHANCED 8 X 8 X 0.85, 0.5 PITCH, 56 TERMINAL	DOCUMENT NO: 98ASA00589D	REV: C
	STANDARD: NON-JEDEC	
	SOT684-18	19 APR 2016



DETAIL G
VIEW ROTATED 90° CW

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TITLE: QFN, THERMALLY ENHANCED 8 X 8 X 0.85, 0.5 PITCH, 56 TERMINAL	DOCUMENT NO: 98ASA00589D	REV: C
	STANDARD: NON-JEDEC	
	SOT684-18	19 APR 2016

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–2009.
3. THIS DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DIMENSION APPLIES ONLY FOR TERMINALS.

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TITLE: QFN, THERMALLY ENHANCED 8 X 8 X 0.85, 0.5 PITCH, 56 TERMINAL	DOCUMENT NO: 98ASA00589D	REV: C
	STANDARD: NON–JEDEC	
	SOT684–18	19 APR 2016

9 Revision history

Revision	Date	Description of changes
1.0	5/2014	• Initial release
2.0	8/2014	• SW2, SW3, and SW4 voltage range modification • Table 6.1.2 added to explain how to change the start sequence. • Table 95 added • Added PC34VR500V2ES to the Orderable part Table 1 • Update the 98A number • Added Bill of Materials
3.0	1/2015	• Updated Table 1 (corrected a typo) • Updated values for V_{SW2ACC} in Table 47 • Updated values for V_{SW3ACC} in Table 56 • Updated values for V_{SW4ACC} in Table 65 • Updated package outline (changed 98ASA00379D to 98ASA00589D) • Added optimized value for the buck regulator external components
4.0	7/2015	• Added MC34VR500V3ES, MC34VR500V4ES, MC34VR500V5ES to the Orderable Part Variations Table • Added SW1, SW2, SW3, SW4 transient load plots • Added SW1, SW2 efficiency plots • Updated Control interface I2C block description, I2C device ID, and I2C operation sections • Updated SW2 rated current to 2.0 A
5.0	1/2017	• Updated document to NXP form and style • Added MC34VR500V6ES, MC34VR500V7ES, and MC34VR500V8ES to Table 1 • Updated Table 8 and added the new part numbers to 5.1 Features, page 12, and 6.4.4.17 SW4, page 49 • Updated Figure 16

6.0	1/2018	• Updated voltage values under “Four independent outputs” for SW2 and SW3 from “0.625 V to 1.975 V” to “0.625V to 3.3V” in Section 5.1
		• Updated Figure 4 in Section 5.2, to reflect revised voltage values for SW2 and SW3
		• Updated voltage values for SW2 and SW3 in Table 21 from “0.625 - 1.975” to “0.625 - 1.975 / 0.8 - 3.3”
		• Updated Step size values for SW2 and SW3 from “25” to “25 / 50” in Table 21
		• Updated SW2 and SW3 voltage from “1.975 V” to “3.3” V in Figure 10
		• Updated Section 6.4.4.10 and Table 39
		• Updated Table 41, Table 42 and Table 43, adding two rows to the bottom of each table
		• Updated Table 47, as follows:
		  • Added high voltage range values “2.0 V < V_{SW2} < 3.3 V”, “-6.0” and “6.0” in the first bullet of Parameter, Min and Max columns for V_{SW2ACC}
		  • Added high voltage range values “2.0 V < V_{SW2} < 3.3 V”, “-3.0” and “3.0” in the second bullet of Parameter, Min and Max columns for V_{SW2ACC}
		  • Updated the parameter value for V_{SW2} from “2.8 V < V_{IN} < 4.5 V, 0.625 V < V_{SW2} < 1.975 V” to “2.8 V < V_{IN} < 4.5 V, 0.625 V < V_{SW2} < 3.3 V”
		  • Added third bullet under Parameter along with associated Typ values for η_{SW2}
		• Updated Section 6.4.4.13, revising “1.975 V” to “3.3 V”
		• Updated the first paragraph of Section 6.4.4.14 and the content of Table 48
		• Updated Table 50, Table 51 and Table 52, adding two rows to the bottom of each table
		• Updated Table 56 as follows:
		  • Added high voltage range values “2.0 V < V_{SW3} < 3.3 V”, “-6.0” and “6.0” in the first bullet of Parameter, Min and Max columns for V_{SW3ACC}
		  • Added high voltage range values “2.0 V < V_{SW2} < 3.3 V”, “-3.0” and “3.0” in the second bullet of Parameter, Min and Max columns for V_{SW3ACC}
		  • Updated the parameter value for V_{SW3} from “2.8 V < V_{IN} < 4.5 V, 0.625 V < V_{SW3} < 1.975 V” to “2.8 V < V_{IN} < 4.5 V, 0.625 V < V_{SW3} < 3.3 V”
		  • Removed “single/dual phase” from “PWM, APS mode single/dual phase”
		  • Removed “PWN, APS mode independent (per phase)” from the parameter value for I_{SW3} and removed the associated Max value
		  • Removed “x” after “SW3” in the note at the bottom of the table.
		• Updated Table 94 as follows:
		  • Remove the values for Bit 6 for addresses 35, 36, 37, 3C, 3D, 3E, AC and B0
		• Updated bold text before item 6 for SW2 and bold text before item 7 for SW3 from “(0.625-1.975 V)” to “(0.625-3.3 V)” in Table 96.

Revision	Date	Description of changes
7.0	5/2018	• Added MC34VR500V9ES to Table 1 • Added 34VR500V9 to “Four independent outputs” for SW4 in Section 5.1 Features, page 12 • Updated Table 8
8.0	8/2018	• Added MC34VR500VAES to Table 1 • Added configuration for 34VR500VA to Table 8
9.0	1/2019	• Added MC34VR500VBES to Table 1 • Added configuration for 34VR500VB to Table 8
10	3/2020	• Changed document status from Advance Information to Technical Data • Updated Features list on page 1 as per CIN 202003004I (deleted “Auto qualified AEC Q100 grade 2”)

11	4/2020	• Updated start-up configuration for 34VR500VB in Table 8
		  • LDO3_SEQ - replaced 3 by 2
		  • SW2_VOLT - replaced 1.8 V by 0.9 V
		  • SW3_VOLT - replaced 0.9 V by 1.8 V

12	3/2021	• Updated as per CIN 202103010I
		  • Added MC34VR500VCES to Table 1
		  • Added configuration for 34VR500VC to Table 8

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