19-5801; Rev 1; 12/11

Low-Current SPI/3-Wire RTCs

General Description

The DS1343/DS1344 low-current real-time clocks (RTCs) are timekeeping devices that provide an extremely low standby current, permitting longer life from a backup supply source. The devices also support high-ESR crystals, broadening the pool of usable crystals for the devices. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

Address and data are transferred serially through an SPI or 3-wire interface. Two programmable time-of-day alarms are provided. Each alarm can generate an interrupt on a combination of seconds, minutes, hours, and day. Don't-care states can be inserted into one or more fields if it is desired for them to be ignored for the alarm condition. The time-of-day alarms can be programmed to assert two different interrupt outputs, or they can be combined to assert one common interrupt output. Both interrupt outputs operate when the device is powered by either V_{CC} or V_{BAT}.

The devices are available in a lead-free/RoHS-compliant, 20-pin TSSOP or 14-pin TDFN package, and support a -40°C to +85°C extended industrial temperature range.

Applications

Medical

Handheld Devices

Telematics

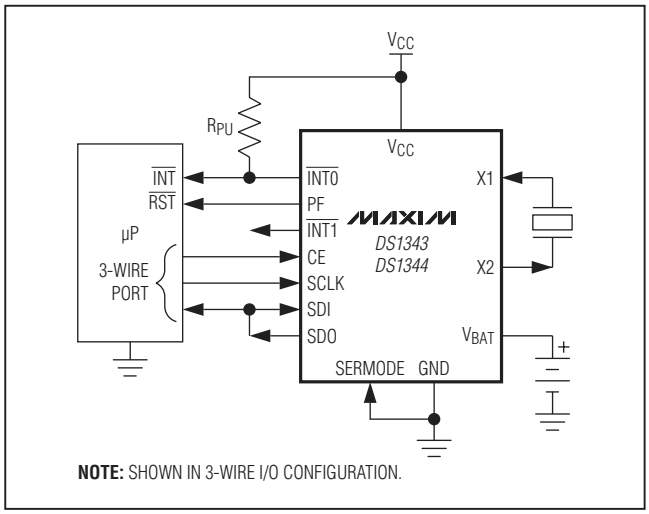
Embedded Timestamping

***Ordering Information* appears at end of data sheet.**

Features

- **Low Timekeeping Current of 250nA (typ)**
- **Compatible with Crystal ESR Up to 100kΩ**
- **Versions Available to Support Either 6pF or 12.5pF Crystals**
- **RTC Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap Year Compensation Valid Through 2099**
- **Power-Fail and Switch Circuitry**
- **Three Operating Voltages**
  - **1.8V ±5%**
  - **3.0V±10%**
  - **3.3V ±10%**
- **Trickle-Charge Capability**
- **Maintain Time Down to 1.15V (typ)**
- **Support Motorola SPI Modes 1 and 3, or Standard 3-Wire Interface**
- **Burst Mode for Reading/Writing Successive Addresses in Clock/RAM**
- **96-Byte Battery-Backed NV RAM for Data Storage**
- **Two Time-of-Day Alarms with Two Interrupt Outputs**
- **Industrial Temperature Range**
- **20-Pin TSSOP or 14-Pin TDFN Package**
- **Underwriters Laboratories (UL) Recognized**

Typical Operating Circuit



NOTE: SHOWN IN 3-WIRE I/O CONFIGURATION.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} or V_{BAT} Relative to Ground ..... -0.3V to +6.0V
Voltage Range on Any Nonpower Pin Relative to Ground ..... -0.3V to (V_{CC} + 0.3V)
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature Maximum ..... +150°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +260°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 91°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 20°C/W

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 54°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	DS134_-18	1.71	1.8	5.5	V
		DS134_-3	2.7	3.0	5.5	
		DS134_-33	3.0	3.3	5.5	
Minimum Timekeeping Voltage	$V_{BAT}T_{MIN}$	T_A = +25°C		1.15	1.3	V
Backup Voltage	V_{BAT}		1.3		5.5	V
Logic 1 Input	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Logic 0 Input	V_{IL}		-0.3		0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = $V_{CC(MIN)}$ to +5.5V, V_{BAT} = +1.3V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Active Current		I_{CCA}	-3 or -33: f_{SCLK} = 4MHz (Note 4)			600	µA
Power-Supply Standby Current (Note 5)		I_{CCS}	-33: V_{CC} = 3.63V			120	µA
			V_{CC} = $V_{CC(MAX)}$			160	
Backup Leakage Current		I_{BATLKG}	V_{CC} > V_{PF}	-100	+25	+100	nA
Backup Current (Oscillator Off)		I_{BAT}	T_A = +25°C, V_{CC} = 0V, $\overline{EOSC}$ = 1			100	nA
Backup Current (Note 6)	DS1343	I_{BAT1}	V_{BAT} = 3V		250		nA
			V_{BAT} = $V_{BAT(MAX)}$			500	
	DS1344		V_{BAT} = 3V		350		
			V_{BAT} = $V_{BAT(MAX)}$			600	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = $V_{CC(MIN)}$ to +5.5V, V_{BAT} = +1.3V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Backup Current (Note 7)	DS1343	I_{BAT2}	V_{BAT} = 3V		300		nA
			V_{BAT} = $V_{BAT(MAX)}$			600	
	DS1344		V_{BAT} = 3V		400		
			V_{BAT} = $V_{BAT(MAX)}$			700	
Input Leakage (CE, SERMODE, SCLK, SDI)		I_I	V_{IN} = 0V to V_{CC}	-0.1		+0.1	µA
Output Leakage ($\overline{INT0}$, $\overline{INT1}$, $\overline{PF}$, SDO)		I_O	CE = V_{IL}, no alarms	-0.1		+0.1	µA
Output Logic 1 ($\overline{PF}$, SDO)		I_{OH}	-3 or -33: V_{OH} = 2.4V	-1			mA
Output Logic 0, V_{OL} = 0.4V ($\overline{INT0}$, $\overline{INT1}$, $\overline{PF}$, SDO)		I_{OL}	$V_{CC} \geq V_{CC(MIN)}$	3.0			mA
			$V_{BAT} \geq 1.3V \geq V_{CC}$ + 0.2V (Note 8)	250			µA
Power-Fail Trip Point		V_{PF}	-18	1.51	1.6	1.71	V
			-3	2.45	2.6	2.70	
			-33	2.70	2.88	3.0	
Switchover Voltage		V_{SW}	V_{BAT} > V_{PF}	V_{PF}			V
			V_{BAT} < V_{PF}	V_{BAT} > V_{CC}			
Trickle-Charger Resistors		R1		1			kΩ
		R2		2			
		R3		4			

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}	-18	DC		1	MHz
		-3 or -33	DC		4	
Data to SCLK Setup	t_{DC}		30			ns
SCLK to Data Hold	t_{CDH}		30			ns
SCLK to Data Delay	t_{CDD}	-18			160	ns
		-3 or -33			80	
SCLK Low Time	t_{CL}	-18	400			ns
		-3 or -33	110			
SCLK High Time	t_{CH}	-18	400			ns
		-3 or -33	110			
SCLK Rise and Fall	t_R, t_F				200	ns
CE to SCLK Setup	t_{CC}		400			ns
SCLK to CE Hold	t_{CCH}		100			ns
CE Inactive Time	t_{CWH}	-18	500			ns
		-3 or -33	400			
CE to Output High-Z	t_{CDZ}				40	ns
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 9)		25	100	ms

POWER-UP/DOWN CHARACTERISTICS

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{REC}			20	40	ms
V_{CC} Fall Time (V_{PF} to 0V)	t_{VCCF}		150			µs
V_{CC} Rise Time (0V to V_{PF})	t_{VCCR}		0			µs

CAPACITANCE

(T_A = +25°C, unless otherwise noted.)

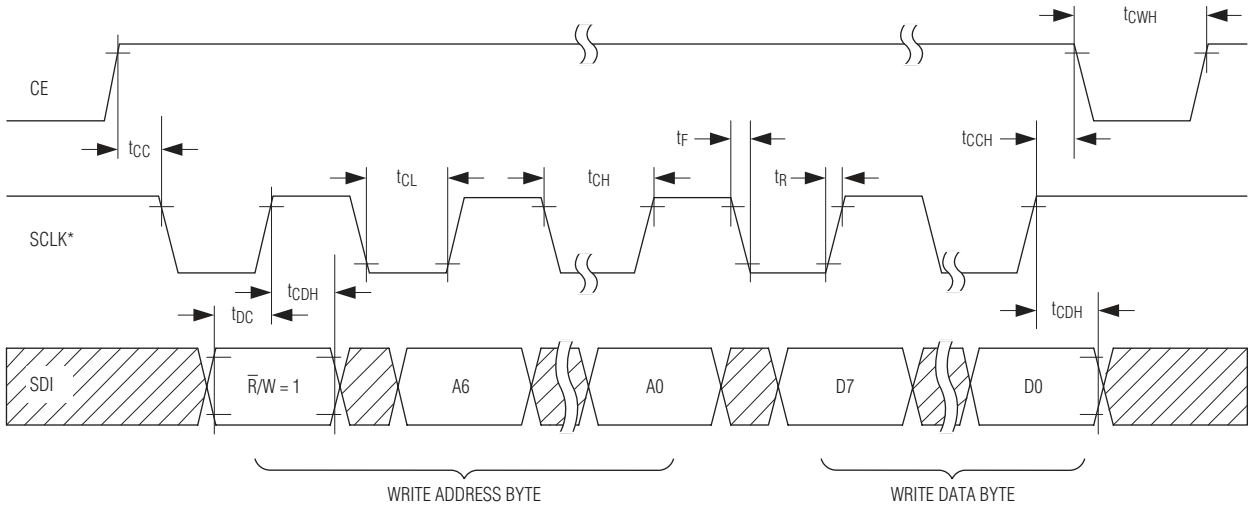
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	(Note 10)		10		pF
Output Capacitance	C_O	(Note 10)		15		pF

CRYSTAL PARAMETERS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O			32.768		kHz
Series Resistance	ESR				100	kΩ
Load Capacitance	C_L	DS1343		6		pF
		DS1344		12.5		

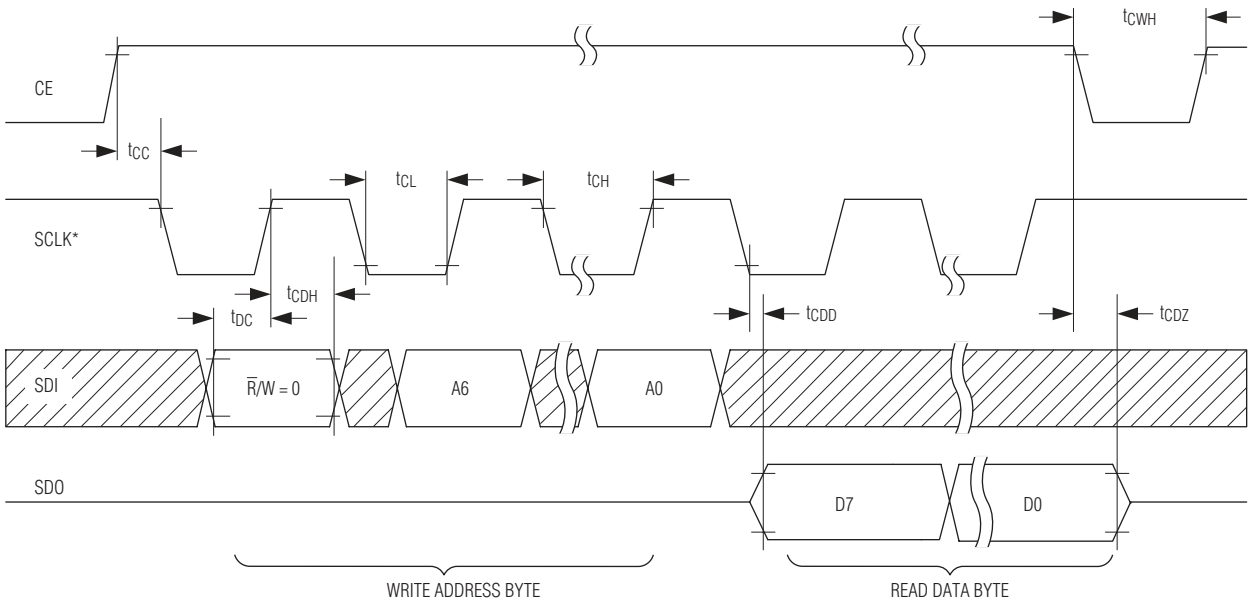
Note 2: Voltage referenced to ground.
Note 3: Limits at T_A = -40°C are guaranteed by design and not production tested.
Note 4: CE = V_{CC}, V_{SCLK} = V_{CC} to GND, I_{OUT} = 0mA, trickle charger disabled.
Note 5: CE = GND, I_{OUT} = 0mA, $\overline{EOSC}$ = EGFIL = DOSF = 0, trickle charger disabled.
Note 6: V_{CC} = 0V, EGFIL = 0, DOSF = 1.
Note 7: V_{CC} = 0V, EGFIL = 1, DOSF = 0.
Note 8: Applies to $\overline{INT0}$ and $\overline{INT1}$.
Note 9: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set.
Note 10: Guaranteed by design; not 100% production tested.

SPI Write Timing



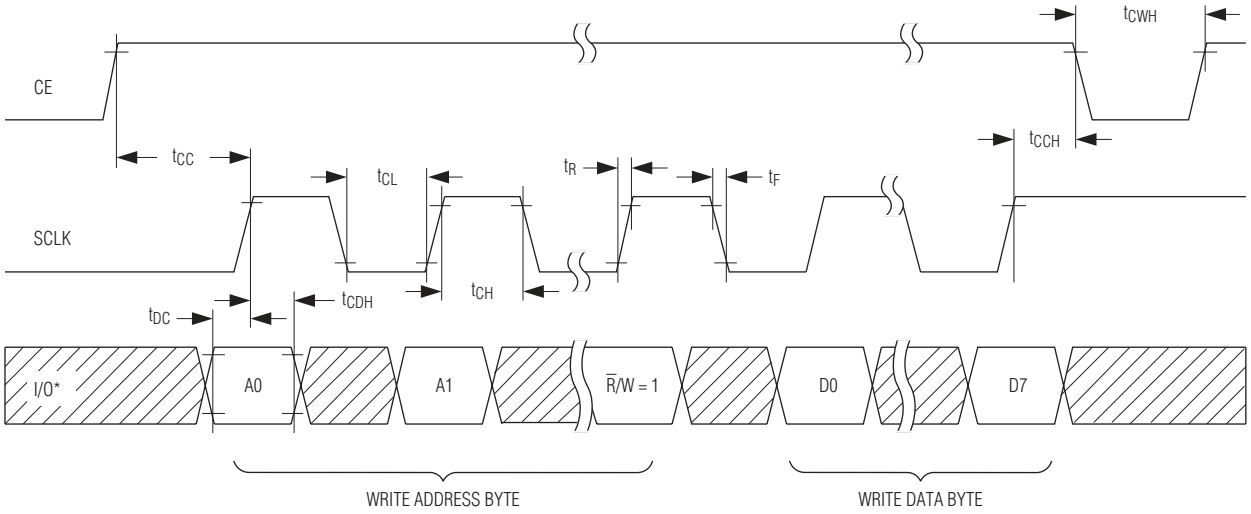
*SCLK CAN BE EITHER POLARITY. TIMING SHOWN FOR CPOL = 1.
SERMODE = V_{CC}.

SPI Read Timing



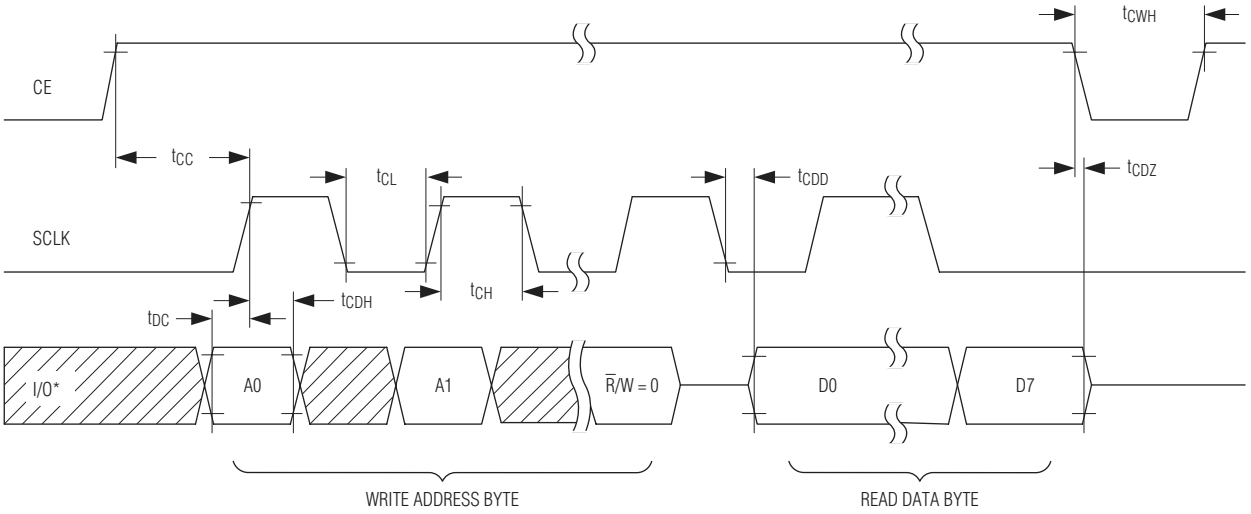
*SCLK CAN BE EITHER POLARITY. TIMING SHOWN FOR CPOL = 1.
SERMODE = V_{CC}.

3-Wire Write Timing



*I/O IS SDI AND SDO CONNECTED TOGETHER.
SERMODE = GND.

3-Wire Read Timing

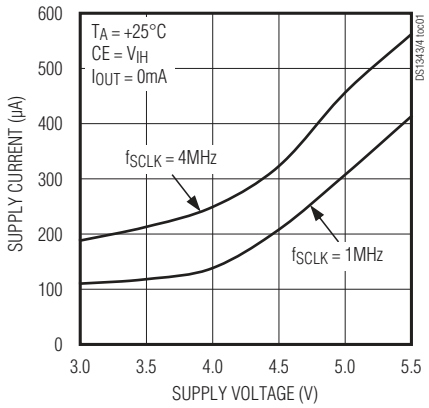


*I/O IS SDI AND SDO CONNECTED TOGETHER.
SERMODE = GND.

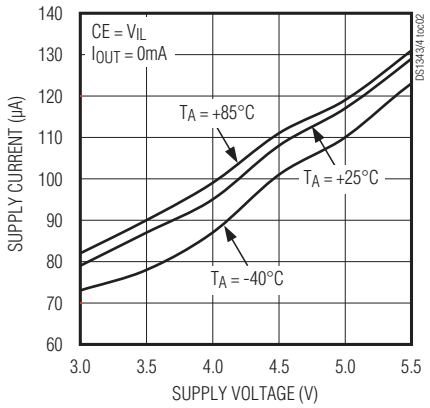
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

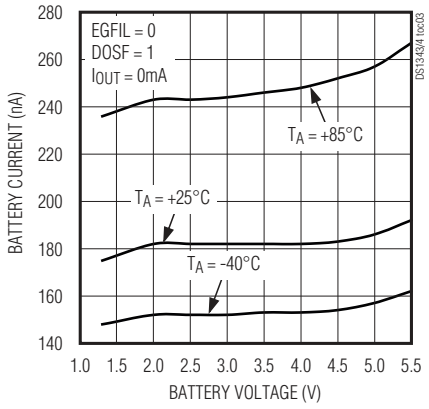
POWER-SUPPLY CURRENT vs. POWER-SUPPLY VOLTAGE



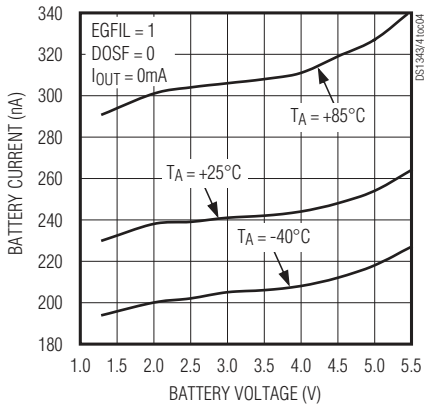
POWER-SUPPLY CURRENT vs. POWER-SUPPLY VOLTAGE



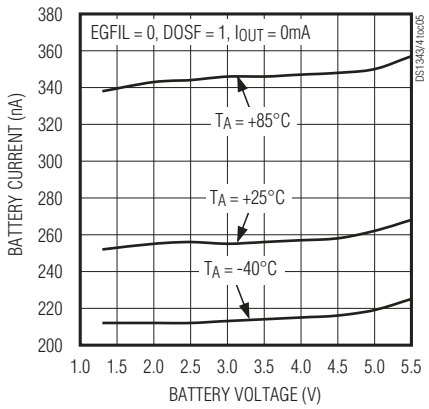
DS1343 BATTERY CURRENT1 vs. BATTERY VOLTAGE



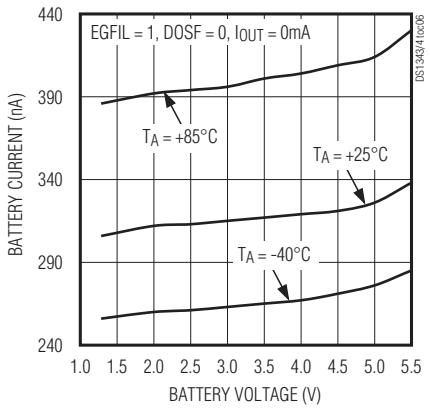
DS1343 BATTERY CURRENT2 vs. BATTERY VOLTAGE



DS1344 BATTERY CURRENT1 vs. BATTERY VOLTAGE

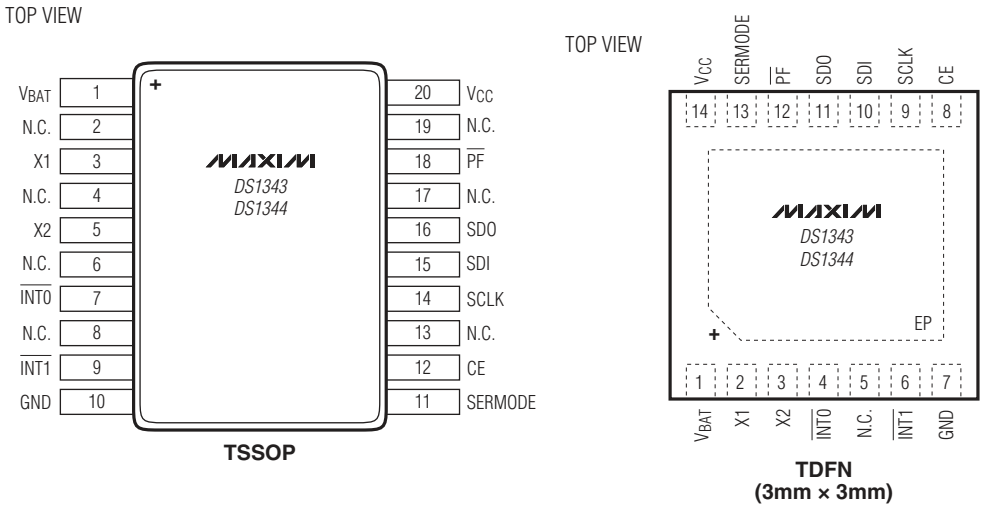


DS1344 BATTERY CURRENT2 vs. BATTERY VOLTAGE



Low-Current SPI/3-Wire RTCs

Pin Configurations



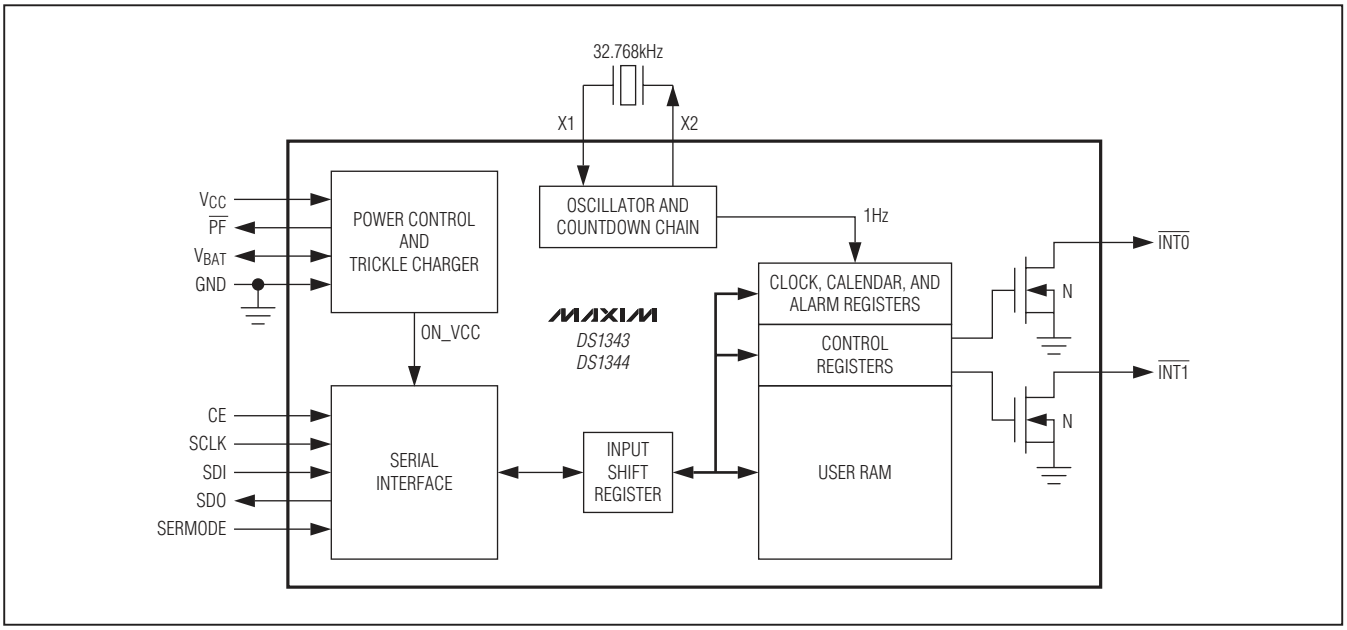
Pin Descriptions

PIN		NAME	FUNCTION
TSSOP	TDFN-EP		
1	1	V_{BAT}	Battery Input for Standard +3V Lithium Cell or Other Energy Source. UL recognized to ensure against reverse charging current when used in conjunction with a primary lithium battery.
2, 4, 6, 8, 13, 17, 19	5	N.C.	No Connection. N.C. pins can be connected to GND to reduce noise around the crystal inputs.
3	2	X1	Connections for Standard 32.768kHz Quartz Crystal (see the *Crystal Characteristics* table). The devices can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator and the X2 pin is left unconnected.
5	3	X2	
7	4	$\overline{INT0}$	Active-Low Interrupt 0 Output. $\overline{INT0}$ is an active-low output that can be used as an interrupt output to a processor. $\overline{INT0}$ can be programmed to be asserted by only Alarm 0, or can be programmed to be asserted by either Alarm 0 or Alarm 1. $\overline{INT0}$ remains low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. $\overline{INT0}$ operates when the component is powered by V_{CC} or V_{BAT}. $\overline{INT0}$ is an open-drain output and requires an external pullup resistor.
9	6	$\overline{INT1}$	Active-Low Interrupt 1 Output. $\overline{INT1}$ is an active-low output that can be used either as an interrupt output to a processor or a 32kHz square-wave output. $\overline{INT1}$ can be programmed to be asserted by Alarm 1 only. $\overline{INT1}$ remains low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. $\overline{INT1}$ operates when the component is powered by V_{CC} or V_{BAT}. $\overline{INT1}$ is an open-drain output and requires an external pullup resistor.

Pin Descriptions (continued)

PIN		NAME	FUNCTION
TSSOP	TDFN-EP		
10	7	GND	Ground
11	13	SERMODE	Serial-Interface Mode Input. When connected to GND, standard 3-wire communication is selected. When connected to V_{CC}, SPI communication is selected.
12	8	CE	Chip Enable. The chip-enable signal must be asserted high during a read or a write for either 3-wire or SPI communications.
14	9	SCLK	Serial-Clock Input. SCLK is used to synchronize data movement on the serial interface for either 3-wire or SPI communications.
15	10	SDI	Serial-Data Input. When SPI communication is selected, SDI is the serial-data input for the SPI bus. When 3-wire communication is selected, this pin must be connected to SDO (SDI and SDO function as a single I/O pin when connected together).
16	11	SDO	Serial-Data Output. When SPI communication is selected, SDO is the serial-data output for the SPI bus. When 3-wire communication is selected, this pin must be connected to SDI (SDI and SDO function as a single I/O pin when connected together).
18	12	$\overline{PF}$	Active-Low Power-Fail Output. The $\overline{PF}$ pin is used to indicate loss of the primary power supply (V_{CC}). When V_{CC} is less than V_{PF}, the $\overline{PF}$ pin is driven low.
20	14	V_{CC}	Power-Supply Input
—	—	EP	Exposed Pad (TDFN Only). Connect to GND or leave unconnected.

Functional Diagram



Detailed Description

The DS1343/DS1344 low-current real-time clocks (RTCs) are timekeeping devices that consume an extremely low timekeeping current and also support high-ESR crystals, broadening the pool of usable crystals for the device.

The devices provide a full binary-coded decimal (BCD) clock calendar that is accessed by a simple serial interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year through 2099. The clock operates in either a 24-hour or 12-hour format with an $\overline{AM}$/PM indicator. In addition, 96 bytes of NV RAM are provided for data storage. The devices maintain the time and date, provided that the oscillator is enabled, as long as at least one supply is at a valid level.

Both devices provide two programmable time-of-day alarms. Each alarm can generate an interrupt on a programmable combination of seconds, minutes, hours, and day. Don't-care states can be inserted into one or more fields if it is desired for them to be ignored for the alarm condition. The time-of day alarms can be programmed to assert two different interrupt outputs or to assert one common interrupt output. Both interrupt outputs operate when the device is powered by V_{CC} or V_{BAT}.

The devices support a direct interface to SPI serial-data ports or standard 3-wire interface. A straight-forward address and data format is implemented in which data transfers can occur one byte at a time or in multiple-byte burst mode.

The devices have a built-in temperature-compensated power-sense circuit that detects power failures and automatically switches to the backup supply. The V_{BAT} pin can be configured to provide trickle charging of a rechargeable voltage source, with selectable charging resistance and diode-voltage drops.

I/O and Power-Switching Operation

The devices operate as slave devices on a 3-wire or SPI serial bus. Access is obtained by selecting the part by the CE pin and clocking data into/out of the part using the SCLK and SDI/SDO pins. Multiple byte transfers are supported within one CE high period; see the *Serial Peripheral Interface (SPI)* section for more information. The devices are fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access, and the device power is switched from V_{CC} to V_{BAT}.

If V_{PF} is less than the voltage on the backup supply, the device power is switched from V_{CC} to the backup supply when V_{CC} drops below V_{PF}. If V_{PF} is greater than the backup supply, the device power is switched from V_{CC} to the backup supply when V_{CC} drops below the backup supply. The registers are maintained from the backup supply source until V_{CC} is returned to nominal levels. The *Functional Diagram* illustrates the main elements.

Freshness Seal Mode

When a battery is first attached to the device, the device does not immediately provide battery-backup power to the RTC or internal circuitry. After V_{CC} exceeds V_{PF}, the devices leave the freshness seal mode and provide battery-backup power whenever V_{CC} subsequently falls below V_{BAT}. This mode allows attachment of the battery during product manufacturing, but no battery capacity is consumed until after the system has been activated for the first time. As a result, minimum battery energy is used during storage and shipping.

Oscillator Circuit

The devices use an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. The DS1343 includes integrated capacitive loading for a 6pF C_L crystal, and the DS1344 includes integrated capacitive loading for a 12.5pF C_L crystal. See the *Crystal Parameters* table for the external crystal parameters. The *Functional Diagram* shows a simplified schematic of the oscillator circuit. The startup time is usually less than one second when using a crystal with the specified characteristics.

Clock Accuracy

When running from the internal oscillator, the accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 1 shows a typical PCB layout for isolation of the crystal and oscillator from noise. Refer to Application Note 58: *Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

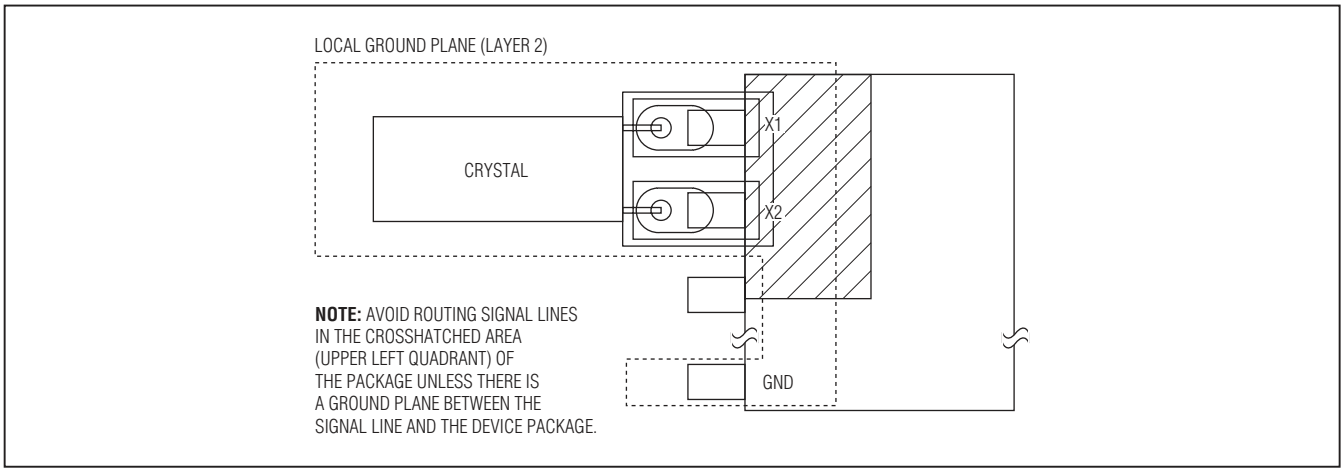


Figure 1. Layout Example

Register Map

Table 1 shows the devices' register map. During a multibyte RTC access, if the address pointer reaches the end of the register space (1Fh), it wraps around to location 00h. During a multibyte RAM access, if the address pointer reaches the end of the register space (7Fh), it wraps around to location 20h. On either the rising edge of CE or an RTC address pointer wrap around, the current time is transferred to a secondary set of registers. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

Clock and Calendar (00h–06h)

The time and calendar information is obtained by reading the appropriate register bytes. Table 1 shows the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the BCD format. The Day register increments at midnight and rolls over from 7 to 1. Values that correspond to the day-of-week are user defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

The devices can be run in either 12-hour or 24-hour mode. Bit 6 of the Hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit, with a content of 1 being PM. In the 24-hour mode, bit 5 is the 20-hour field. Changing the 12/$\overline{24}$ mode-select bit requires that the Hours data subsequently be reentered, including the Alarm register (if used). The Century bit (bit 7 of Month) is toggled when the Years register rolls over from 99 to 00. On a power-on reset (POR), the time and date are set to 00:00:00 01/01/00 (hh:mm:ss DD/MM/YY), and the Day register is set to 01.

Alarms (07h–0Eh)

The devices contains two time-of-day/date alarms. Alarm 0 can be set by writing to registers 07h–0Ah. Alarm 1 can be set by writing to registers 0Bh–0Eh. The alarms can be programmed to activate the $\overline{INT0}$ or $\overline{INT1}$ outputs on an alarm match condition (see Table 2). Bit 7 of each of the time of day/date alarm registers are mask bits. When all the mask bits for each alarm are 0, an alarm only occurs when the values in the timekeeping registers 00h–06h match the values stored in the alarm registers. The alarms can also be programmed to repeat every second, minute, hour, or day. Configurations not listed in the table result in illogical operation. POR values are undefined.

When the RTC register values match alarm register settings, the corresponding alarm flag bit (IRQF0 or IRQF1) is set to 1 in the Status register. If the corresponding alarm interrupt enable bit (A0IE or A1IE) is also set to 1 in the Control register, the alarm condition activates the output(s) defined by the INTCN bit. Upon an active alarm, clearing the associated IRQF[1:0] bit deasserts the selected interrupt output while leaving the alarm enabled for the next occurrence of a match. Alternatively, clearing the A_IE bit deasserts the output and inhibits further output activations.

The alarm flags are always active, fully independent of the A_IE bit states. All alarm registers should be written to logic zero to disable the alarm matching.

Table 1. Register Map

ADDRESS	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	FUNCTION	RANGE
00h	0	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Minutes			Minutes				Minutes	00–59
02h	0	12/$\overline{24}$	$\overline{AM}$/PM 20 Hours	10 Hours	Hour				Hours	1–12 + $\overline{AM}$/PM 00–23
03h	0	0	0	0	0	Day			Day	1–7
04h	0	0	10 Date		Date				Date	01–31
05h	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06h	10 Year				Year				Year	00–99
07h	A0M1	10 Seconds			Seconds				Alarm 0 Seconds	00–59
08h	A0M2	10 Minutes			Minutes				Alarm 0 Minutes	00–59
09h	A0M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hours	10 Hours	Hour				Alarm 0 Hours	1–12 + $\overline{AM}$/PM 00–23
0Ah	A0M4	0	0	0	Day				Alarm 0 Day	1–7
0Bh	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
0Ch	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
0Dh	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hours	10 Hours	Hour				Alarm 1 Hours	1–12 + $\overline{AM}$/PM 00–23
0Eh	A1M4	0	0	0	Day				Alarm 1 Day	1–7
0Fh	$\overline{EOSC}$	X	DOSF	EGFIL	SQW	INTCN	A1IE	A0IE	Control	—
10h	OSF	0	0	0	0	0	IRQF1	IRQF0	Status	—
11h	TCS3	TCS2	TCS1	TCS0	DS1	DS0	RS1	RS0	Trickle Charger	—
12h–1Fh	Reserved								Reserved	—
20h–7Fh	User RAM								User RAM	00h–FFh

Note: *Bits listed as 0 always read back as 0 and cannot be written to 1.*

Table 2. Alarm Mask Bits

ALARM REGISTER MASK BITS (BIT 7)				ALARM RATE
A_M4	A_M3	A_M2	A_M1	
1	1	1	1	Alarm once a second
1	1	1	0	Alarm when seconds match
1	1	0	0	Alarm when minutes and seconds match
1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	Alarm when day, hours, minutes, and seconds match

Control Register (0Fh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{EOSC}$	X	DOSF	EGFIL	SQW	INTCN	A1IE	A0IE
1	0	0	0	0	0	0	0

BIT 7	**$\overline{EOSC}$:** Enable oscillator. During battery backup, when $\overline{EOSC}$ is set to 0, the oscillator is enabled during backup operation. When set to 1, the oscillator is stopped when the device is powered by the backup supply. This bit is set to logic 1 on the initial application of power.
BIT 6	Not used.
BIT 5	**DOSF:** Disable oscillator stop flag. When the DOSF bit is set to 1, sensing of the oscillator conditions that would set the OSF bit are disabled. OSF remains at 0 regardless of what happens to the oscillator. This bit is cleared (0) on the initial application of power.
BIT 4	**EGFIL:** Enable glitch filter. When the EGFIL bit is 1, the 5µs glitch filter at the output of crystal oscillator is enabled. The glitch filter is disabled when this bit is 0. This bit is cleared (0) on the initial application of power.
BIT 3	**SQW:** Enable square wave. When the SQW bit is set to 1, a 32kHz square wave is output on the $\overline{INT1}$ output. This bit is cleared (0) on the initial application of power.
BIT 2	**INTCN:** Interrupt control. This bit controls the relationship between the two time-of-day alarms and the two interrupt output pins. When the INTCN bit is 1, a match between the timekeeping registers and the Alarm 0 registers activates the $\overline{INT0}$ output (provided A0IE = 1), and a match between the timekeeping registers and the Alarm 1 registers activates the $\overline{INT1}$ output (provided A1IE = 1). When the INTCN bit is 0, a match between the timekeeping registers and either the Alarm 0 registers or Alarm 1 registers activates the $\overline{INT0}$ output (provided A0IE = A1IE = 1). The $\overline{INT1}$ output has no function when INTCN = 0. The INTCN bit is cleared (0) on the initial application of power.
BIT 1	**A1IE:** Alarm 1 interrupt enable. When A1IE is set to 0, the Alarm 1 interrupt function is disabled. When A1IE is 1, the Alarm 1 interrupt function is enabled and is routed to either $\overline{INT0}$ (if INTCN = 0) or $\overline{INT1}$ (if INTCN = 1). Regardless of the state of A1IE, a match between the timekeeping registers and the Alarm 1 registers (0Bh–0Eh) sets the interrupt request 1 flag bit (IRQF1). The A1IE bit is cleared (0) when power is first applied.
BIT 0	**A0IE:** Alarm 0 interrupt enable. When A0IE is set to 0, the Alarm 0 interrupt function is disabled. When A0IE is 1, the Alarm 0 interrupt function is enabled and is routed to $\overline{INT0}$. Regardless of the state of A0IE, a match between the timekeeping registers and the Alarm 0 registers (07h–0Ah) sets the interrupt register 0 flag bit (IRQF0). The A0IE bit is cleared (0) when power is first applied.

Status Register (10h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OSF	0	0	0	0	0	IRQF1	IRQF0
1	0	0	0	0	0	0	0

BIT 7	**OSF:** Oscillator stop flag. If the OSF bit is 1, the oscillator either has stopped or was stopped for some period and could be used to judge the validity of the clock and calendar data. This bit is edge triggered and is set to 1 when the internal circuitry senses the oscillator has transitioned from a normal run state to a stop condition. This bit remains at logic 1 until written to logic 0. Attempting to write OSF to 1 leaves the value unchanged. The following are examples of conditions that can cause the OSF bit to be set: 1) The first time power is applied. 2) The voltage present on V_{CC} is insufficient to support oscillation. 3) The $\overline{EOSC}$ bit is a logic one during battery backup. 4) External influences on the crystal (i.e., noise, leakage, etc.).
BIT 1	**IRQF1:** Interrupt request 1 flag. A logic 1 in the IRQF1 bit indicates that the time matched the Alarm 1 registers. This flag can be used to generate an interrupt on either $\overline{INT0}$ or $\overline{INT1}$ depending on the status of the INTCN bit in the Control register. If the INTCN bit is 0 and IRQF1 is 1 (and the A1IE bit is also 1), $\overline{INT0}$ goes low. If the INTCN bit is 1 and IRQF1 is 1 (and the A1IE bit is also 1), $\overline{INT1}$ goes low. IRQF1 is cleared when the address pointer is set to any of the Alarm 1 registers during an I/O transaction. The IRQF1 bit can also be cleared by writing it to 0. This bit can only be written to 0. Attempting to write the IRQF1 bit to 1 leaves the value unchanged.
BIT 0	**IRQF0:** Interrupt request 0 flag. A logic 1 in the IRQF0 bit indicates that the time matched the Alarm 0 registers. If the A0IE bit is also 1, $\overline{INT0}$ goes low. IRQF0 is cleared when the address pointer is set to any of the Alarm 0 registers during an I/O transaction. The IRQF0 bit can also be cleared by writing it to 0. This bit can only be written to 0. Attempting to write the IRQF0 bit to 1 leaves the value unchanged.

Trickle Charger Register (11h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TCS3	TCS2	TCS1	TCS0	DS1	DS0	RS1	RS0
0	0	0	0	0	0	0	0

Register 11h controls the devices' trickle-charge characteristics. The simplified schematic of Figure 2 shows the basic components of the trickle charger. The trickle-charge select (TCS[3:0]) bits (bits 7:4) control the selection of the trickle charger. To prevent accidental enabling, only a pattern of 1010 enables the trickle charger; all other patterns disable the trickle charger. On the initial application of power, the devices power up with the trickle charger disabled. The diode-select (DS[1:0]) bits (bits 3:2) select whether or not a diode is connected between V_{CC} and V_{BAT}. The resistor-select (RS[1:0]) bits (bits 1:0) select the resistor that is connected between V_{CC} and V_{BAT}. The RS and DS bits select the resistor and diodes, as shown in Table 3. The user determines diode and resistor selection according to the maximum current desired for secondary battery or super cap charging. The maximum charging current can be calculated using the equation that follows.

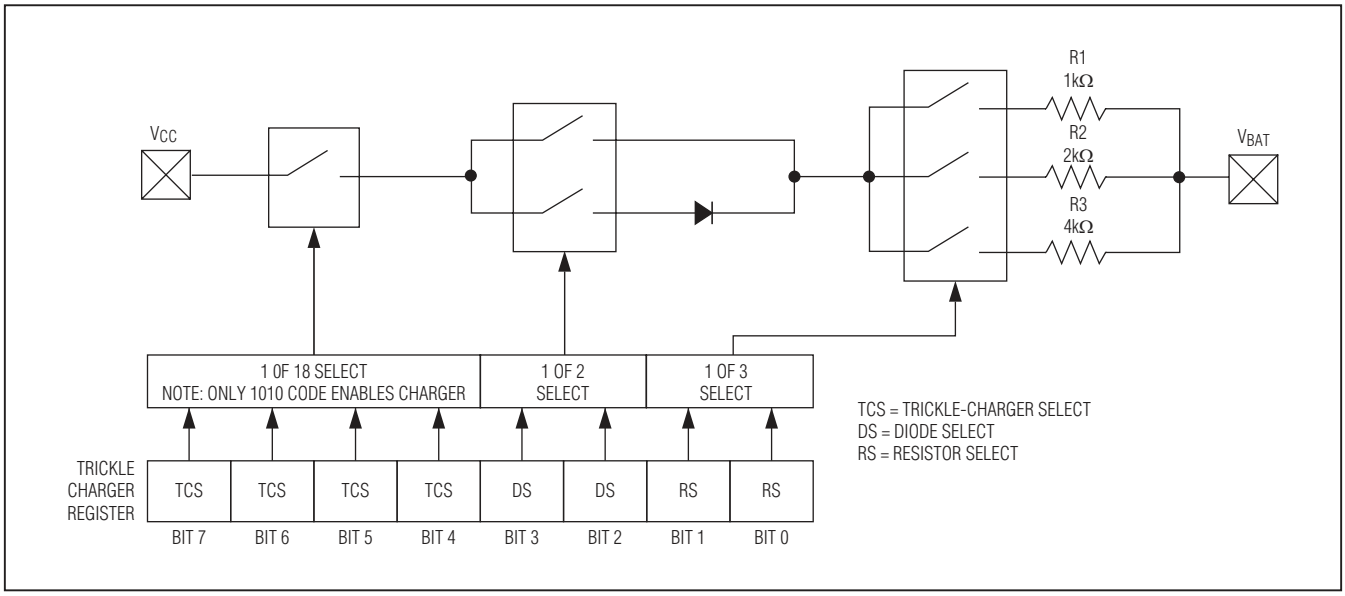


Figure 2. Trickle Charger Block Diagram

Table 3. Trickle-Charger Resistor and Diode Select

TCS3	TCS2	TCS1	TCS0	DS1	DS0	RS1	RS0	FUNCTION
X	X	X	X	X	X	0	0	Disabled
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
1	0	1	0	0	1	0	1	No diode, 1kΩ
1	0	1	0	0	1	1	0	No diode, 2kΩ
1	0	1	0	0	1	1	1	No diode, 4kΩ
1	0	1	0	1	0	0	1	One diode, 1kΩ
1	0	1	0	1	0	1	0	One diode, 2kΩ
1	0	1	0	1	0	1	1	One diode, 4kΩ
0	0	0	0	0	0	0	0	Initial power-on state—disabled

X = Don't care.

Assume, for the purposes of the example, that a system power supply of 5V is applied to V_{CC} and a super cap is connected to V_{BAT}. Also assume that the trickle charger has been enabled with one diode and resistor R1. The maximum current I_{MAX} would be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop})/R1 \approx (5.0V - 0.6V)/2k\Omega \approx 2.2mA$$

As the super cap charges, the voltage drop between V_{CC} and V_{BAT} decreases, and therefore, the charge current decreases.

Serial Port Operation

The devices offer the flexibility to choose between two serial-interface modes. The component can communicate with the SPI interface or with a standard 3-wire interface. The interface method used is determined by SERMODE. When SERMODE is connected to V_{CC}, SPI communication is selected. When SERMODE is connected to ground, standard 3-wire communication is selected.

Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a synchronous bus for address and data transfer, and is used when interfacing with the SPI bus on specific Motorola microcontrollers, such as the 68HC05C4 and the 68HC11A8. The SPI mode of serial communication is selected by connecting SERMODE to V_{CC}. Four pins are used for the SPI. The four pins are SDO (serial-data out), SDI (serial-data in), CE (chip enable), and SCLK (serial clock). The IC is the slave device in an SPI application, with the microcontroller being the master.

SDI and SDO are the serial-data input and output pins, respectively, for the device. The CE input is used to initiate and terminate a data transfer. SCLK is used to synchronize data movement between the master (microcontroller) and the slave (IC) devices.

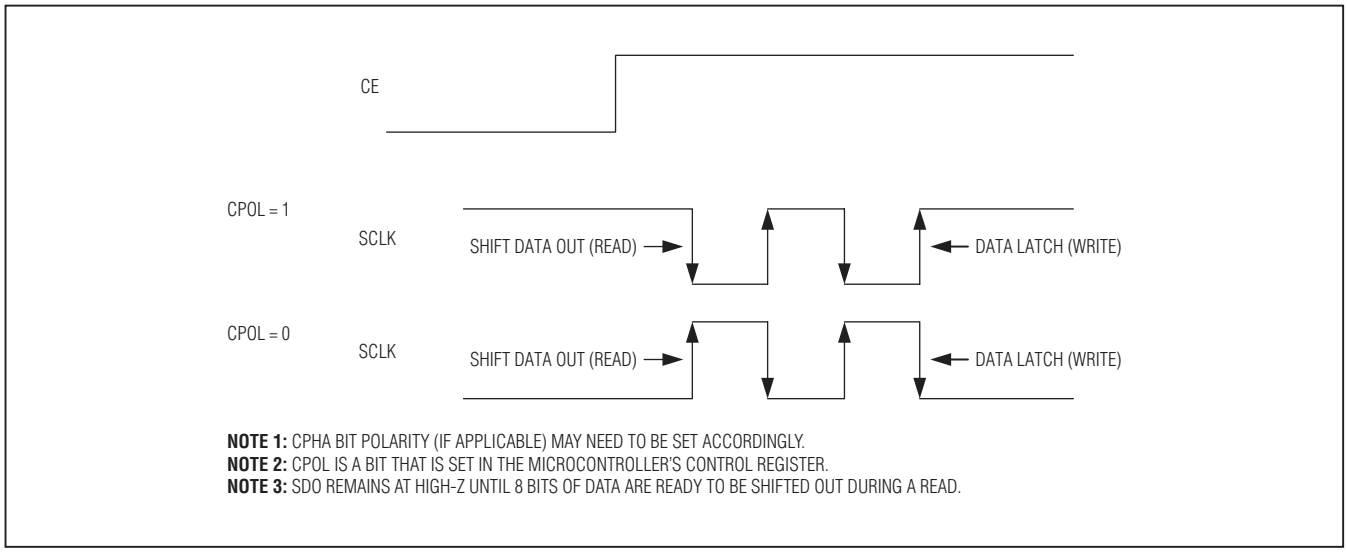
The input clock (SCLK), which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. The inactive clock polarity is programmable in some microcontrollers. The device determines the clock polarity by sampling SCLK when CE becomes active. Therefore, either SCLK polarity can be accommodated. Input data (SDI) is latched on the internal strobe edge and output data (SDO) is shifted out on the shift edge (Figure 3). There is one clock for each bit transferred. Address and data bits are transferred in groups of eight, MSB first.

Address and Data Bytes

Address and data bytes are shifted MSB first into the serial-data input (SDI) and out of the serial-data output (SDO). Any transfer requires the address of the byte to specify a write or read to either a RTC or RAM location, followed by one or more bytes of data. Data is transferred out of the SDO for a read operation and into the SDI for a write operation (Figure 4 and Figure 5).

The address byte is always the first byte entered after CE is driven high. The most significant bit ($\overline{R}/W$) of this byte determines if a read or write takes place. If $\overline{R}/W$ is 0, one or more read cycles occur. If $\overline{R}/W$ is 1, one or more write cycles occur.

Data transfers can occur 1 byte at a time or in multiple-byte burst mode. After CE is driven high an address is written to the device. After the address, one or more data bytes can be written or read. For a single-byte transfer, 1 byte is read or written and then CE is driven low. For a multiple-byte transfer, however, multiple bytes can be read or written to the device after the address has been written. Each read or write cycle causes the RTC register or RAM address to automatically increment. Incrementing continues until the device is disabled. When the RTC address space is selected, the address wraps to 00h after incrementing from 1Fh. When the RAM address space is selected, the address wraps to 20h after incrementing from 7Fh.



NOTE 1: CPHA BIT POLARITY (IF APPLICABLE) MAY NEED TO BE SET ACCORDINGLY.
NOTE 2: CPOL IS A BIT THAT IS SET IN THE MICROCONTROLLER'S CONTROL REGISTER.
NOTE 3: SDO REMAINS AT HIGH-Z UNTIL 8 BITS OF DATA ARE READY TO BE SHIFTED OUT DURING A READ.

Figure 3. Serial Clock as a Function of Microcontroller Clock Polarity (CPOL)

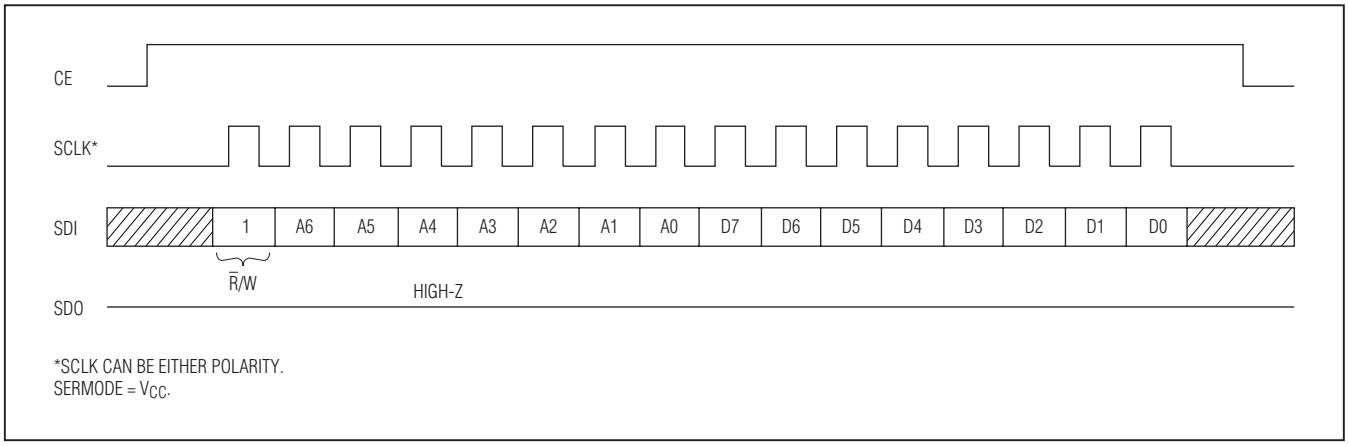


Figure 4. SPI Single-Byte Write

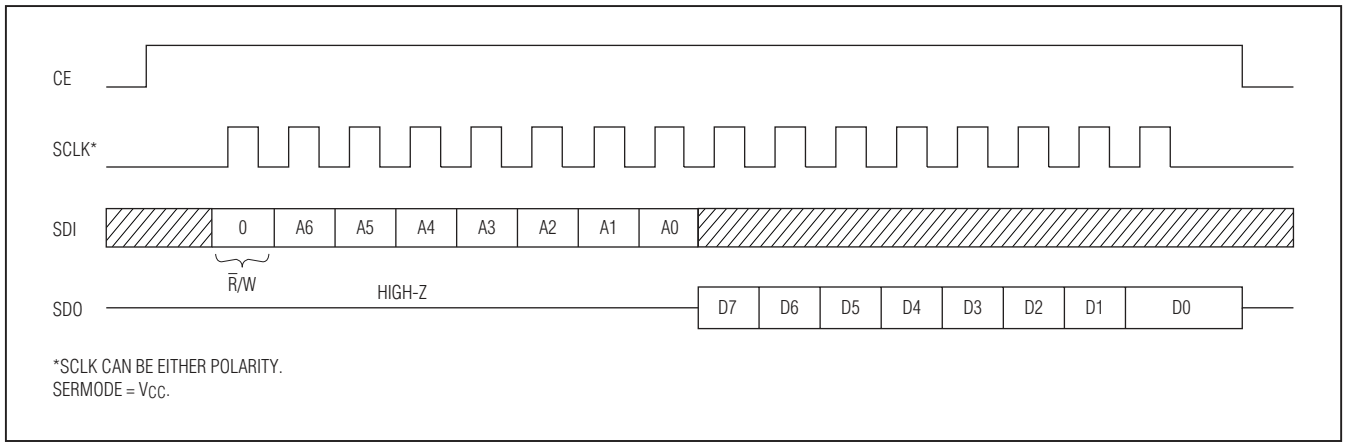


Figure 5. SPI Single-Byte Read

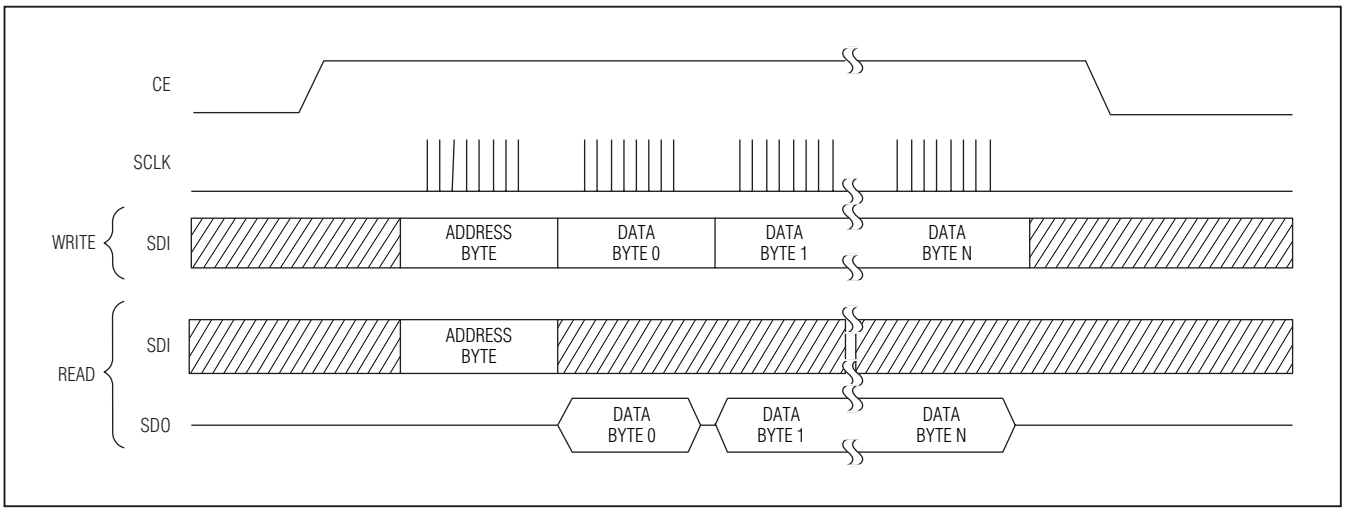


Figure 6. SPI Multibyte Burst Transfer

Reading and Writing in Burst Mode

Burst mode is similar to a single-byte read or write, except that CE is kept high and additional SCLK cycles are sent until the end of the burst. The clock registers and the user RAM can be read or written in burst mode. The address pointer wraps around to 00h after reaching 1Fh (RTC), and the address pointer wraps around to 20h after reaching 7Fh (RAM). See Figure 6.

3-Wire Interface

The 3-wire interface mode operates similarly to the SPI mode. However, in 3-wire mode there is one I/O instead of separate data-in and data-out signals. The 3-wire interface consists of the I/O (SDI and SDO pins connected together), CE, and SCLK pins. In 3-wire mode, each byte is shifted in LSB first, unlike SPI mode, where each byte is shifted in MSB first.

As is the case with the SPI mode, an address byte is written to the device followed by a single data byte or multiple data bytes. Figure 7 illustrates a write cycle, and Figure 8 illustrates a read cycle. In 3-wire mode, data is input on the rising edge of SCLK and output on the falling edge of SCLK.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the devices, decouple the V_{CC} power supply with a 0.01µF and/or 0.1µF capacitor. Use a high-quality, ceramic, surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Using Open-Drain Outputs

The $\overline{INT0}$ and $\overline{INT1}$ outputs are open drain and therefore require external pullup resistors to realize a logic-high output level.

Battery Charge Protection

The devices contain Maxim's redundant battery-charge protection circuit to prevent any charging of an external battery. The DS1343 and DS1344 are recognized by Underwriters Laboratories (UL) under file E141114.

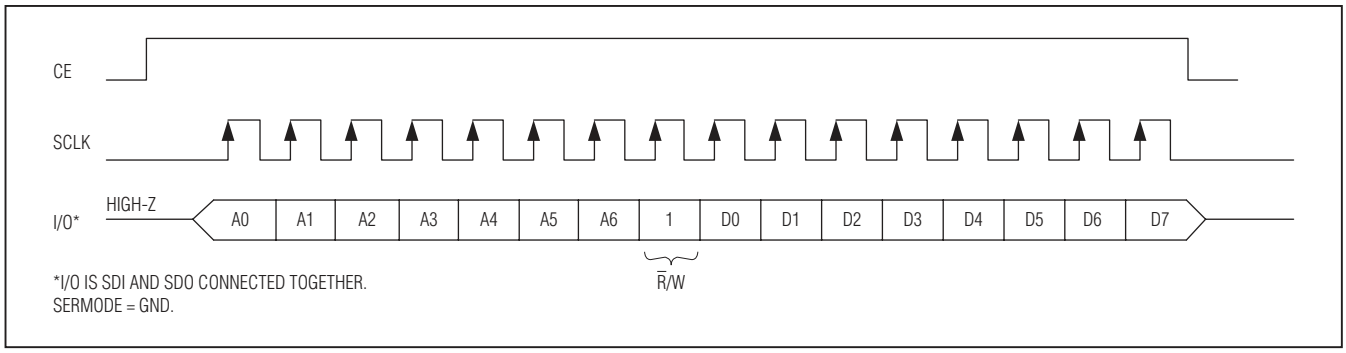


Figure 7. 3-Wire Single-Byte Write

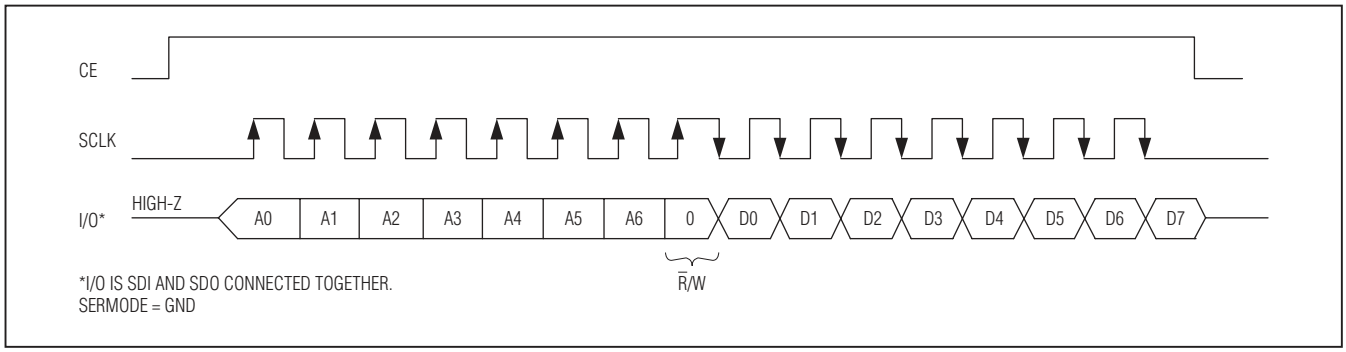


Figure 8. 3-Wire Single-Byte Read

Ordering Information

PART	TEMP RANGE	TYP OPERATING VOLTAGE (V)	OSC C_L (pF)	PIN-PACKAGE
DS1343E-18+*	-40°C to +85°C	1.8	6	20 TSSOP
DS1343E-3+*	-40°C to +85°C	3.0	6	20 TSSOP
DS1343E-33+	-40°C to +85°C	3.3	6	20 TSSOP
DS1343D-18+*	-40°C to +85°C	1.8	6	14 TDFN-EP**
DS1343D-3+*	-40°C to +85°C	3.0	6	14 TDFN-EP**
DS1343D-33+	-40°C to +85°C	3.3	6	14 TDFN-EP**
DS1344E-18+*	-40°C to +85°C	1.8	12.5	20 TSSOP
DS1344E-3+*	-40°C to +85°C	3.0	12.5	20 TSSOP
DS1344E-33+	-40°C to +85°C	3.3	12.5	20 TSSOP
DS1344D-18+*	-40°C to +85°C	1.8	12.5	14 TDFN-EP**
DS1344D-3+*	-40°C to +85°C	3.0	12.5	14 TDFN-EP**
DS1344D-33+	-40°C to +85°C	3.3	12.5	14 TDFN-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—Contact factory for availability.*
***EP = Exposed pad.*

Chip Information

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TSSOP	U20+1	**21-0066**	**90-0116**
14 TDFN-EP	T1433+2	**21-0137**	**90-0063**

Low-Current SPI/3-Wire RTCs

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—
1	12/11	Removed future status from several DS1344 parts in the *Ordering Information* table; added UL recognized to the *Features* and *Battery Charge Protection* sections; added I_{BATLKG} and DS1344 I_{BAT1}, I_{BAT2} specs to the *DC Electrical Characteristics* section; added DS1344 *Typical Operating Characteristics* graphs	1, 2, 7, 18, 19

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