Evaluation Board for Power Management Unit for Imaging Modules

EVAL-ADP5020

FEATURES

Input voltage: 2.4 V to 5.5 V
Evaluates three regulators (Buck 1, Buck 2, and LDO)
USB to I²C interface translation
Jumpers for input current measurement of regulators
Supports EN, SYNC, and XSHTDWN pin interface
Evaluation software included

GENERAL DESCRIPTION

The evaluation system is composed of a motherboard and a daughterboard. The motherboard provides the I²C® signals from the computer USB port and generates the I/O voltages and digital high and low signals for the daughterboard.

The motherboard features a 3.3 V regulator (VBOARD) a 3.7 V regulator (VBATT) and a 2.0 V regulator (VDDIO). VDDIO is the digital I/O voltage supplying the I²C interface and the control pins. VBOARD is the motherboard logic supply while VBATT provides power to the daughterboard. Jumpers on the top left of the motherboard define whether the internal regulators are supplied from the USB port or from external supplies connected to J10. The VBUS line from the USB connector powers the motherboard regulators when Jumper LK8 to Jumper LK10 are in the USB position. Connector J10 provides supply voltages for the motherboard and daughterboard when Jumper LK8 to Jumper LK10 are in the EXT position.

The daughterboard contains numerous jumpers, LEDs, and test points for easy evaluation and monitoring of the board.

MOTHERBOARD AND DAUGHTERBOARD LAYOUT

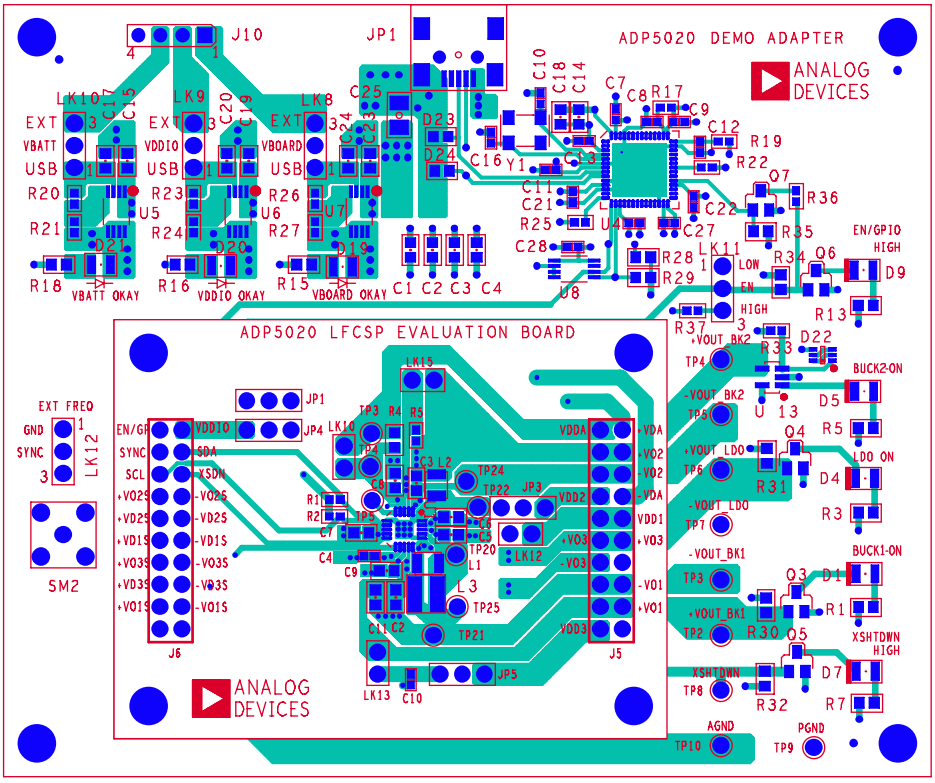

Figure 1.

Rev. 0

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REVISION HISTORY

5/09—Revision 0: Initial Version

SOFTWARE INSTALLATION

1. Before starting the software installation, make sure that the ADP5020 adapter board is not connected to the PC USB port.
2. The application software is a compiled LabVIEW™ program requiring the LabVIEW 8.5 run-time engine to be installed on the PC. Download the LabVIEW run-time engine from National Instruments.
3. After installation, reboot the PC to complete the operation if necessary. Note that if the PC already has LabVIEW installed, this step is not needed.
4. Launch the file **Setup.exe**. When the dialog box shown in Figure 2 appears, click **Next >** to continue.

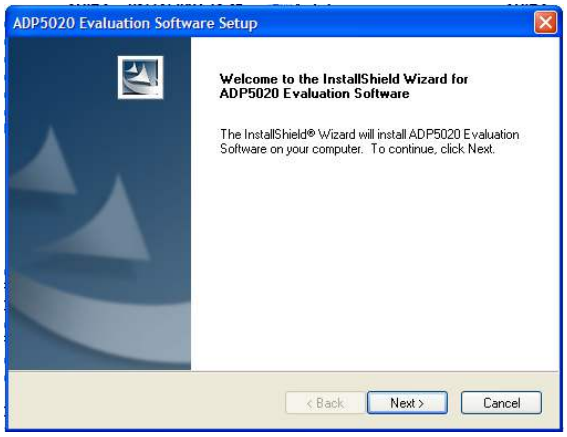


Figure 2. ADP5020 Evaluation Software Setup

5. Click **Yes** to accept the license agreement.

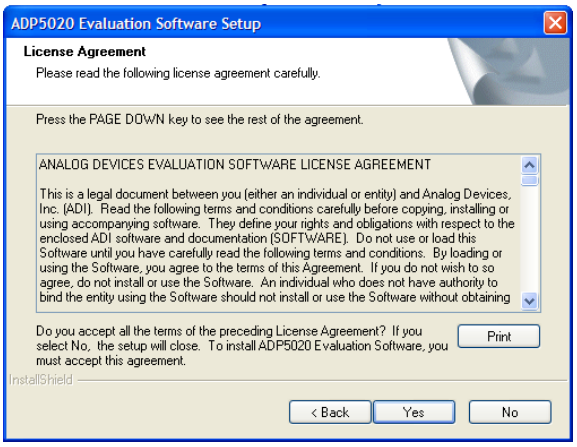


Figure 3. License Agreement

6. Click **Next >** to install the files to the default destination folder or click **Browse…** to choose a different file.

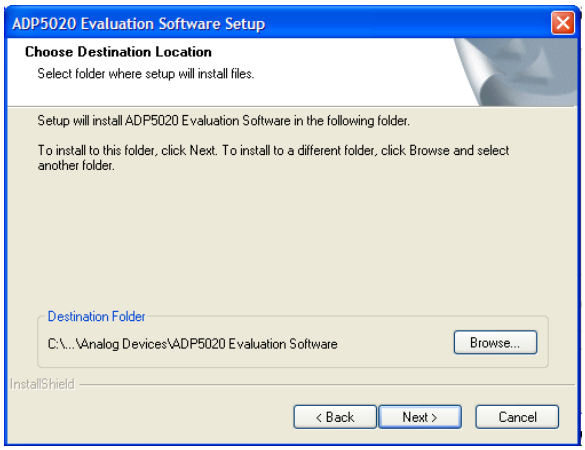


Figure 4. Choose Destination Location

7. Click **Next >** to continue with the installation.

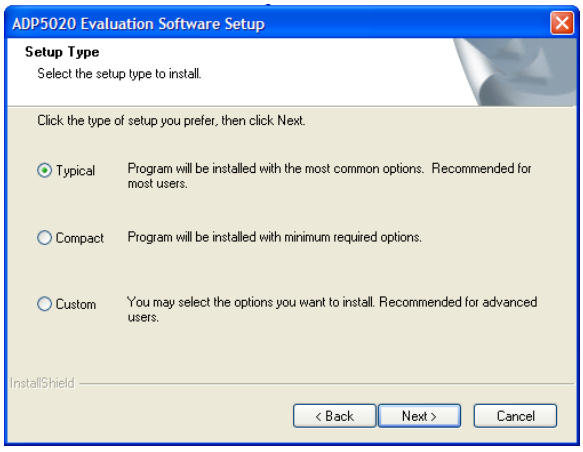


Figure 5. Setup Type

8. Click **Next >** to install the program to the default program folder.

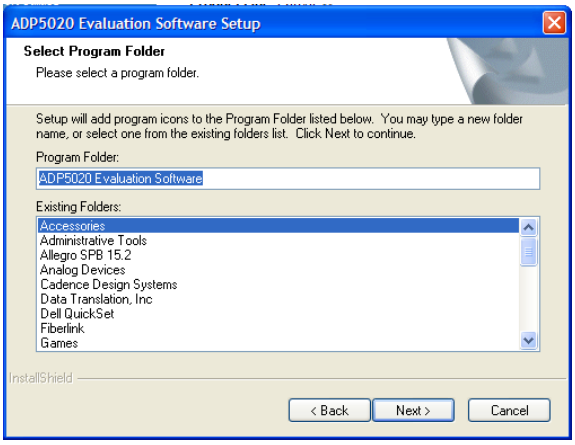


Figure 6. Select Program Folder

9. Wait while the program installs.

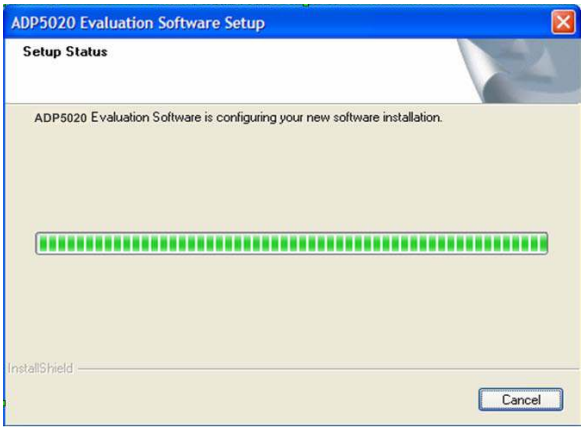


Figure 7. Setup Status

10. Click **Finish** to complete the installation.

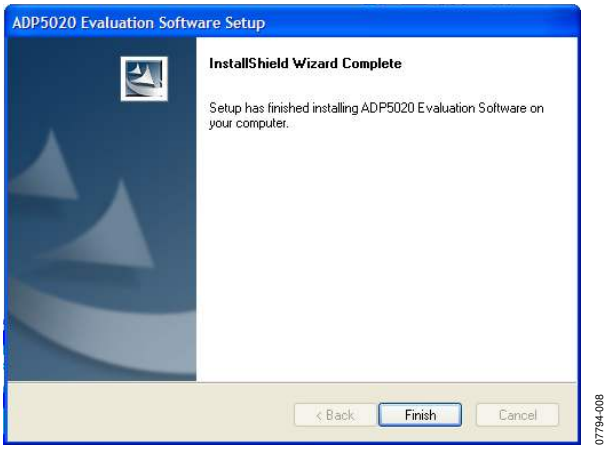


Figure 8. InstallShield Wizard Complete

USB DRIVER INSTALLATION

1. Plug the ADP5020 board into the computer using the USB cable provided with the evaluation kit. Once the system recognizes the board, the dialog box shown in Figure 9 appears.
2. Click **Next >** to install the driver.

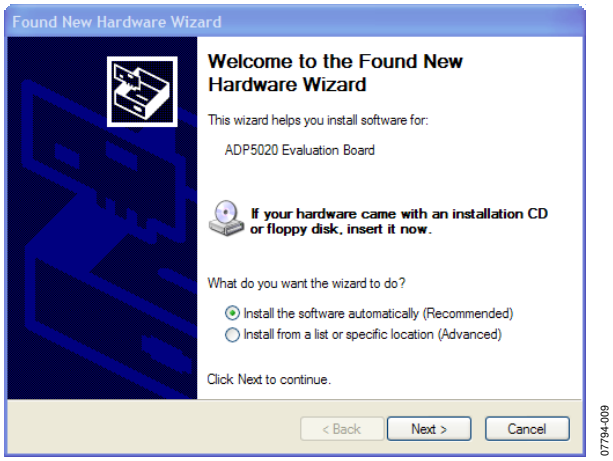


Figure 9. Found New Hardware Wizard

3. Click **Continue Anyway** and then **Finish** to complete the driver installation.

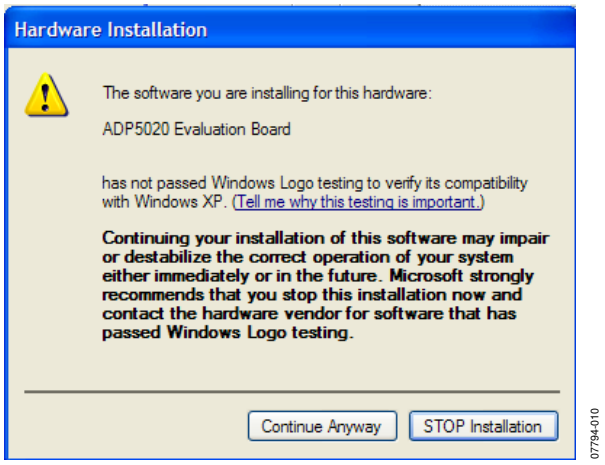


Figure 10. Hardware Installation

4. Open the Device Manager and check that the USB driver is installed properly.

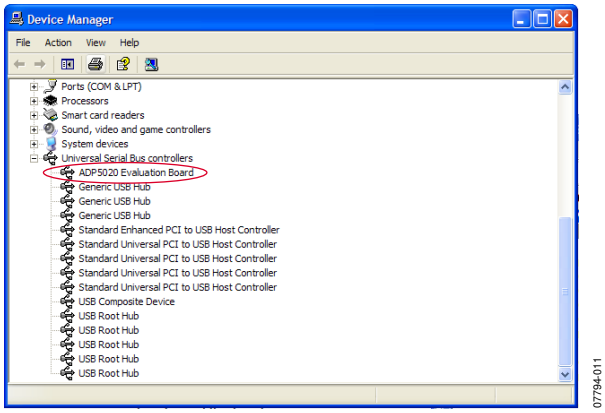


Figure 11. Check Driver Installation

When the USB cable is connected to a PC port different from the one used to install the driver, the PC device driver may ask to install the driver again for that specific port. If this happens, follows the same steps described in the USB driver installation.

EVALUATION BOARD SOFTWARE

QUICK START

Make sure that the software and the USB driver are installed as described in the Software Installation and USB Driver Installation sections. Connect the board as shown in Figure 12. Upon connecting the USB cable, the D19, D20, and D21 indicators light up, indicating that the supplies are connected.

Click the **Start** button, located at the bottom left-hand corner of your desktop. Select **All Programs**, then **Analog Devices**, then **ADP5020 Evaluation Software**, and then **ADP5020 Evaluation SW** to load the software**.** If the program starts correctly and the board is detected, the ADP5020 graphical user interface (GUI) appears as shown in Figure 13.

The program default settings are as follows:

- All registers initialized to zero.
- Software turn-on sequence is: Buck 1 first, Buck 2 second, LDO third. Delay between activations is 1000 ms.
- Software turn-off sequence is: LDO first, Buck 2 second, Buck 1 third. Delay between activations is 1000 ms.
- **Regs Refresh** check box is cleared (status registers are not read periodically).
- Refresh delay is 1000 ms.
- **Smart Update** check box is selected (any change to the registers control triggers a write operation to the device).
- **Verify after write** check box is selected (a write operation is followed by a read for verification).

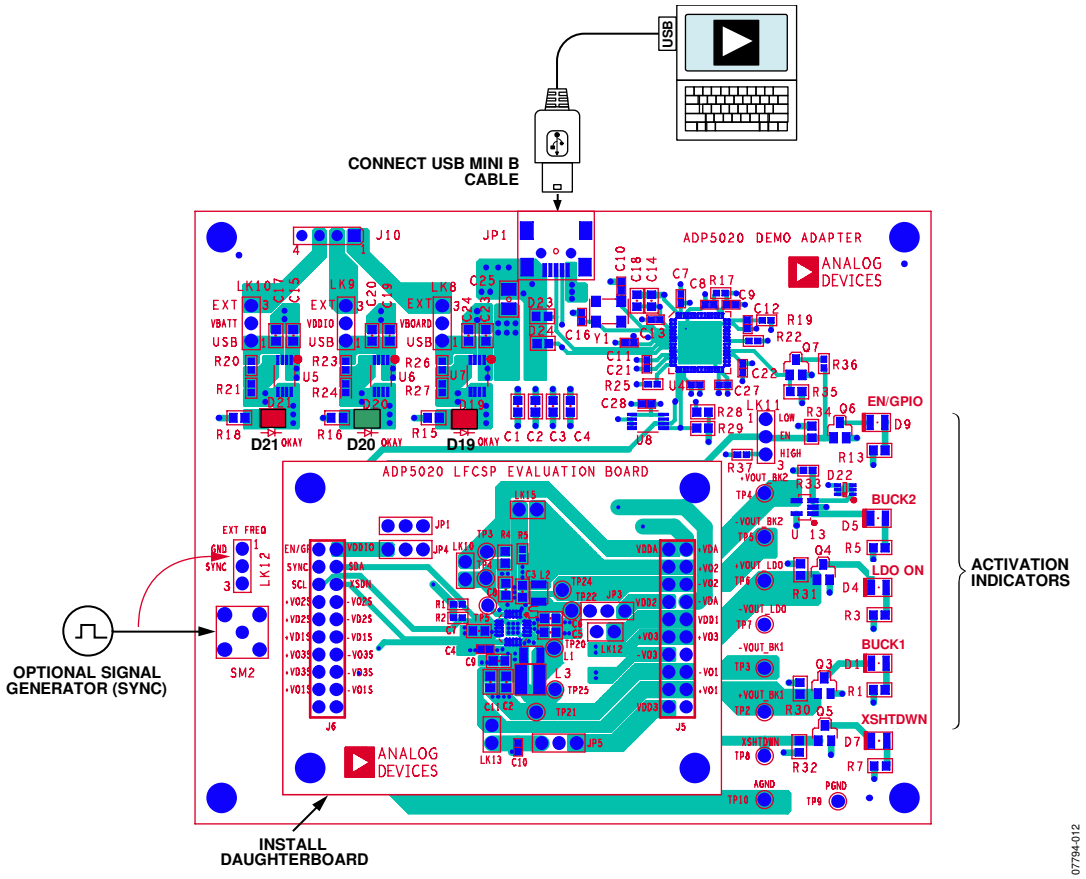


Figure 12. ADP5020 Board Connections

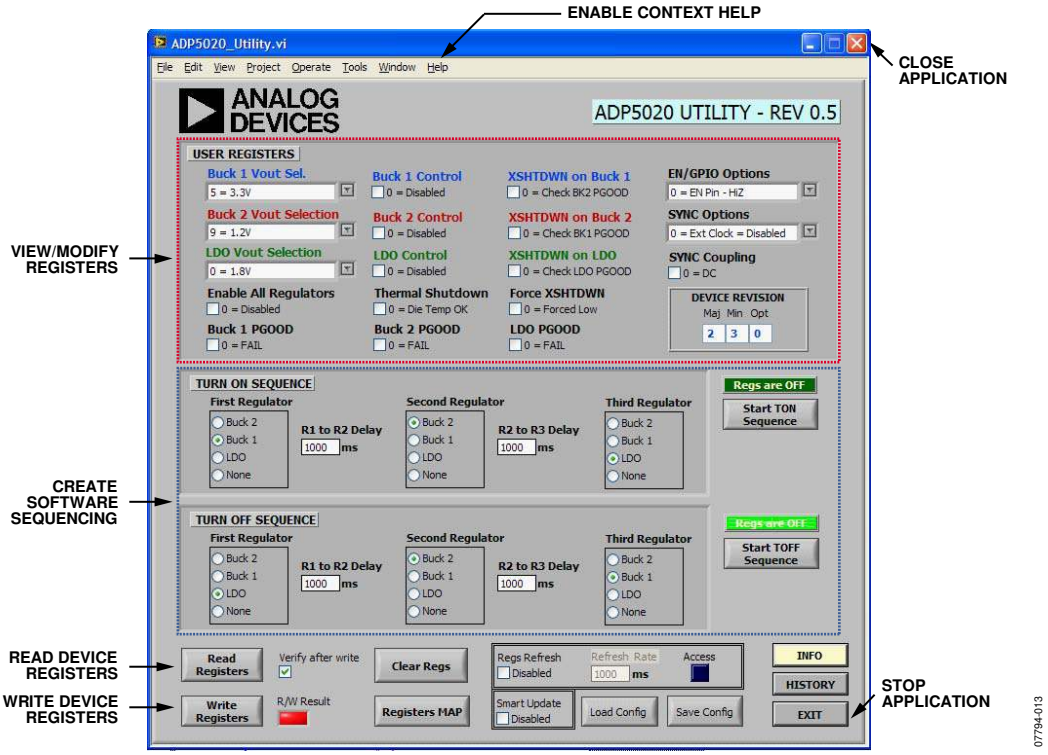
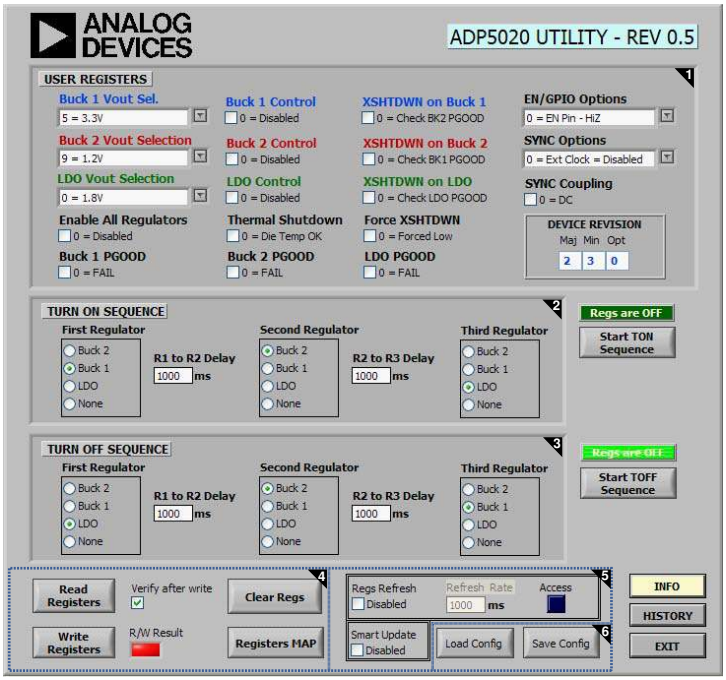


Figure 13. ADP5020 GUI

USING THE SOFTWARE



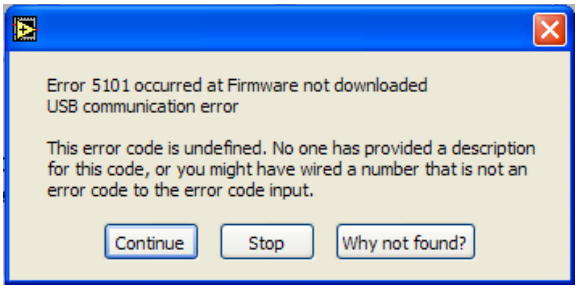
1. VIEW/MODIFY REGISTER SETTINGS.
2. PROGRAM/RUN SOFTWARE TURN-ON SEQUENCE.
3. PROGRAM/RUN SOFTWARE TURN-OFF SEQUENCE.
4. REGISTERS COMMANDS.
5. REGISTERS COMMANDS OPTIONS.
6. LOAD/SAVE REGISTERS CONFIGURATION.

07794-014

Figure 14. Evaluation Board Software

Before running the software, ensure that the board is plugged into the computer USB port (the VBATT OKAY, VDDIO OKAY, and VOBARD OKAY LEDs on the motherboard should light up).

Install the ADP5020 evaluation software as described in the Quick Start section. Failure to detect the adapter board prompts an error message, as shown in Figure 15. If this occurs, check the connection and restart the program.



07794-015

Figure 15. Board Detection Failure

VIEW/MODIFY REGISTER SETTINGS

The **USER REGISTERS** section of the GUI window displays the ADP5020 register settings (following a **Read Registers** operation) and allows you to modify the current values. To facilitate operation, all the possible device configurations are listed in the drop-down boxes. You can select the desired value, then program the device by clicking the **Write Registers** button. If the **Smart Update** check box is selected (default condition), as soon as a register value is changed, the application sends a programming command for that specific register without the need to click the **Write Registers** button. When the **Smart Update** check box is cleared, data is written to the device only after clicking the **Write Registers** button.

The **Buck 1 Vout Sel.** drop-down box allows you to change the Buck 1 regulator output voltage to one of the following settings: 2.5 V, 2.8 V, 2.9 V, 3.0 V, 3.2 V, 3.3 V, or 3.7 V. The default value is 3.3 V. This box corresponds to BK1_VSEL, Bits[2:0] in the BUCK1_VSEL register (Address 0x01).

The **Buck 2 Vout Selection** drop-down box allows you to change the Buck 2 regulator output voltage to one of the following settings: 1.1 V, 1.2 V, 1.3 V, 1.4 V, 1.5 V, 1.6 V, 1.7 V, or 1.8 V. The default value is 1.2 V. This box corresponds to BK2_VSEL, Bits[7:4] in the BUCK2_LDO_VSEL register (Address 0x02).

The **LDO Vout Selection** drop-down box allows you to change the LDO regulator output voltage to one of the following settings: 1.8 V, 1.9 V, 2.0 V, 2.1 V, 2.2 V, 2.3 V, 2.4 V, 2.5 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 3.2 V, or 3.3 V. The default value is 1.8 V. This box corresponds to LDO_VSEL, Bits[3:0] in the BUCK2_LDO_VSEL register (Address 0x02).

The **Buck 1 Control** check box activates, if selected, or deactivates, if cleared, the Buck 1 regulator. This check box corresponds to BK1_EN, Bit[7] in the REG_CONTROL_STATUS register (Address 0x03).

The **Buck 2 Control** check box activates, if selected, or deactivates, if cleared, the Buck 2 regulator. This check box corresponds to BK2_EN, Bit[6] in the REG_CONTROL_STATUS register (Address 0x03).

The **LDO Control** check box activates, if selected, or deactivates, if cleared, the LDO regulator. This check box corresponds to LDO_EN, Bit[5] in the REG_CONTROL_STATUS register (Address 0x03).

The **Enable All Regulators** check box activates, if selected, or deactivates, if cleared, all regulators available. This check box corresponds to EN_ALL, Bit[4] in the REG_CONTROL_STATUS register (Address 0x03).

The **XSHTDWN on Buck 1** check box allows you to mask the Buck 1 power-good (PGOOD) signal, if selected, or to control the power-good signal, if cleared, to generate the XSHTDWN signal. This check box corresponds to BK1_XSHTDN, Bit[3] in the OPERATIONAL_CONTROL register (Address 0x04).

The **XSHTDWN on Buck 2** check box allows you to mask the Buck 2 power-good (PGOOD) signal, if selected, or to control the power-good signal, if cleared, to generate the XSHTDWN signal. This check box corresponds to BK2_XSHTDN, Bit[2] in the OPERATIONAL_CONTROL register (Address 0x04).

The **XSHTDWN on LDO** check box allows you to mask the LDO power-good (PGOOD) signal, if selected, or to control the power-good signal, if cleared, to generate the XSHTDWN signal. This check box corresponds to LDO_XSHTDN, Bit[1] in the OPERATIONAL_CONTROL register (Address 0x04).

The **Force XSHTDWN** check box, if cleared, forces the XSHTDN pin level to Logic 0; if selected, the XSHTDN logic level depends on the power-good (PGOOD) status of the regulators. This check box corresponds to FORCE_XS, Bit[0] in the REG_CONTROL_STATUS register (Address 0x03).

The **Buck 1 PGOOD** check box shows the power-good status for the Buck 1 regulator. If the check box is selected, the Buck 1 regulator is operating correctly; if cleared, it indicates that the Buck 1 regulator is either not activated or in a failing condition. This check box corresponds to BK1_PGOOD, Bit[3] in the REG_CONTROL_STATUS register (Address 0x03).

The **Buck 2 PGOOD** check box shows the power-good status for the Buck 2 regulator. If the check box is selected, the Buck 2 regulator is operating correctly; if cleared, it indicates that the Buck 2 regulator is either not activated or in a failing condition. This check box corresponds to BK2_PGOOD, Bit[2] in the REG_CONTROL_STATUS register (Address 0x03).

The **LDO PGOOD** check box shows the power-good status for the LDO regulator. If the check box is selected, the LDO regulator is operating correctly; if cleared, it indicates that the LDO regulator is either not activated or in a failing condition. This indicator corresponds to LDO_PGOOD, Bit[1] in the REG_CONTROL_STATUS register (Address 0x03).

The **Thermal Shutdown** check box shows the status for the thermal shutdown (TSD) protection. If the check box is selected, the device is in a TSD condition; if cleared, it indicates that the device is operating normally. This check box corresponds to TSD, Bit[0] in the OPERATIONAL_CONTROL register (Address 0x04). When this check box is selected (set to 1), you must clear this check box, then write this bit back to the device to clear a TSD condition. Make sure to clear the **Regs Refresh** check box to override this indicator. If the **Regs Refresh** option is enabled (check box is selected), the periodic refresh writes back the TSD indicator and you will not be able to clear the TSD bit. You must not write this indicator (that is, you must not click the **Write Registers** button) while the **Thermal Shutdown** check box is selected (set to 1) because this forces a TSD condition and the regulators, if enabled, stops working.

The **EN/GPIO Options** drop-down box allows you to program the function associated with the EN/GPIO pin to one of the following settings: input high impedance, output low, or output high. This box corresponds to ENO_DRV, Bit[0], and ENO_HIZ_BAR, Bit[1], in the EN_CONTROL register (Address 0x05).

The **SYNC Options** drop-down box allows you to program the function associated with the SYNC pin to one of the following settings: internal clock, external dc-coupled 9.6 MHz clock, external dc-coupled 19.2 MHz clock, external ac-coupled 9.6 MHz clock, or external ac-coupled 19.2 MHz clock. This box corresponds to SYNC_9P6, Bit[6], and SYNC_19P2, Bit[5], in the OPERATIONAL_CONTROL register (Address 0x04).

The **DEVICE REVISION** box shows the major and minor revision, and the specific device option. It is not possible to alter the values in this box because it is a hard-coded value in the device. This box corresponds to MAJ, Bits[7:5], MIN, Bits[4:2], and OPT, Bits[1:0], in the revision register (Address 0x00).

To read or write the device register in bit or byte format as shown in the device memory map (see the ADP5020 data sheet), you can open the registers map utility by clicking the **Registers MAP** button. See the Registers Commands section for additional information.

PROGRAM/RUN TURN-ON SEQUENCE

The **TURN ON SEQUENCE** section of the GUI window allows you to create and run simple activation patterns for the available regulators, mimicking the desired regulator sequence needed for a specific application. The **First Regulator** option button allows you to turn on the first regulator and **R1 to R2 Delay** allows you to program the delay between the first and second regulator from 1 ms to 10 sec. The **Second Regulator** option button allows you to turn on the second regulator, and **R2 to R3 Delay** allows you to program the delay between the first and second regulator from 1 ms to 10 sec. Finally, the **Third Regulator** option button allows you to turn on the third and last regulator. It is not possible to select more than one regulator under each regulator box (for example, you cannot select both **Buck 2** and **Buck 1** under **First Regulator**). However, if the application requires more than one regulator to be turned on at the same time, set the **R1 to R2 Delay** time to 0 ms, then select another regulator under **Second Regulator**. If all three regulators must be activated at the same time, set the **R2 to R3 Delay** time to 0 ms, then select the third regulator under **Third Regulator**.

Click the **Start TON Sequence** button to run the programmed pattern. Once the pattern is sent to the ADP5020 in the daughter-board, the **Regs are OFF** indicator changes to **Regs are ON** and lights up.

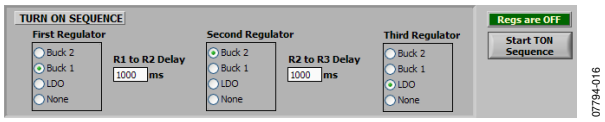


Figure 16. Turn-On Sequence Example

Figure 16 shows a sequencing example where the first regulator activated is Buck 1. After one second, Buck 2 is activated. After another second, the LDO turns on. The XSHTDWN signal becomes high 1 ms after the last regulator (LDO in this example). This delay is hardcoded in the ADP5020 and cannot be changed. The software automatically sets the XSHTDN masking bit if the regulators are set to **None**. Although unnecessary, it is possible to create a sequence where all the regulators are set to **None** (that is, all disabled).

Once a sequence is started, you can verify the PGOOD and TSD device status (under **Buck 1 PGOOD**, **Buck 2 PGOOD**, **LDO PGOOD**, and **Thermal Shutdown**) in the **USER REGISTER** section of the GUI. If the option **Regs Refresh** is enabled (that is, the check box is selected), the status of PGOOD and TSD is updated automatically at the rate programmed under the **Refresh Rate** box.

Note that the timing used for the sequencing uses the PC internal clock with 1 ms resolution. In addition, there are time lags due to the program execution and communication with the adapter board. Therefore, timing precision may be affected, especially for short durations, and may vary from PC to PC.

PROGRAM/RUN TURN-OFF SEQUENCE

The turn-off sequence follows the same indications provided for the turn-on sequence except that the operation is executed in reverse order.

REGISTERS COMMANDS

The **Read Registers** button, when clicked, reads all the ADP5020 internal registers (Addresses 0x00 to Address 0x05) and updates the **USER REGISTERS** section with the new values.

The **Write Registers** button, when clicked, writes the current registers values set in the **USER REGISTERS** section into the ADP5020 volatile memory. If the **Verify after write** check box is selected, the program reads back the programmed registers and compares the device values with the set values (buffer). If one or more errors are detected, a message appears, indicating the registers at fault. Figure 17 shows a verification error example.

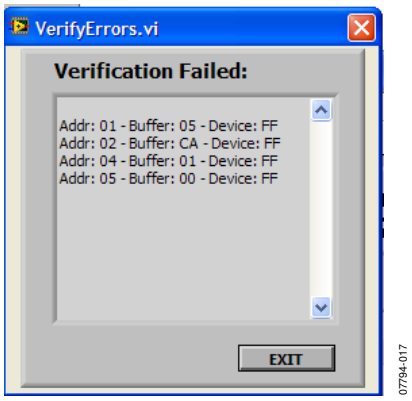


Figure 17. Verification Error

The **Clear Regs** button, when clicked, sets the registers to 0. A message appears requesting confirmation to continue (click **YES**) with the operation or abort it (click **NO**), leaving the registers unchanged.

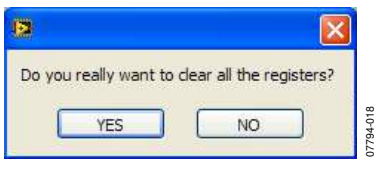


Figure 18. Register Clearing Confirmation

The **Registers MAP** button, when clicked, activates another method to read and write the ADP5020 registers, as shown in Figure 19.

The register values, previously set, are transferred into the **Register MAP** window. You have the choice to modify the registers bitwise by clicking the desired bit position. The bit value then switches from 0 to 1, or vice versa. It is not possible to change the values for the grayed bits. The register values can also be changed by entering a hexadecimal value in the text box for the respective register (for example, 4C is entered for Register 0x00 in Figure 19). The **Hex/Dec** button allows you to change the data format of the register values from hexadecimal to decimal, or vice versa. Binary and Byte controls are intercommunicating; therefore, changes to one control are automatically reflected in the other. The **R** and **W** buttons next to each register allow reading or writing a specific device address, and the **Read ALL** and **Write ALL** buttons allows you to read or write the entire register map from or to the ADP5020 under evaluation. The **OK/Fail** indicator next to these two buttons shows the operation result. Click **EXIT** to return in the main window. The modified registers are then transferred automatically into the **USER REGISTER** section of the GUI window.

The register map utility does not have the **Smart Update** option; therefore, a new value is written into the ADP5020 following a write operation (by clicking the **W** or **Write ALL** buttons).

REGISTER COMMAND OPTIONS

The **Regs Refresh** check box, when selected, enables the program to read the device statuses periodically. The refresh time is programmable in the **Refresh Rate** box from 100 ms to 10 sec. The registers read during the refresh are Register 0x00, the revision register, Register 0x03 (BK1_PGOOD, BK2_PGOOD, and LDO_PGOOD), and Register 0x04 (TSD), providing a real-time indication of the device functionality. If a thermal shutdown event is detected, you must disable the register refresh option (clear the **Regs Refresh** check box) to clear the TSD flag. The **Access** blue indicator, when lit up, indicates that the refresh operation is taking place.

The **Smart Update** check box, when selected, enables the program to automatically write an ADP5020 register when a **USER REGISTER** option has been changed. This avoids the need to click the **Write Registers** button every time a value is changed. The **Smart Update** check box must be cleared if you want to control the write operations.

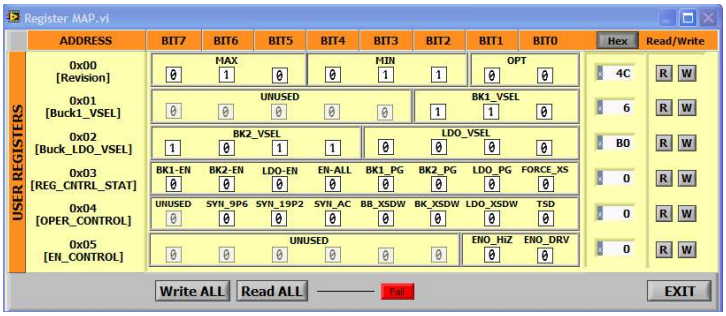


Figure 19. Register MAP Utility

LOAD/SAVE REGISTERS CONFIGURATION

The software program allows saving a specific register configuration and loading it back into the **USER REGISTERS** section. The **Save Config** button, when clicked, opens the file utility where you can specify the directory and file name to save. The default extension is ***.dat.** Maintaining this convention is recommended. If the file does not exist, it is created; if the file already exists, it is overwritten.

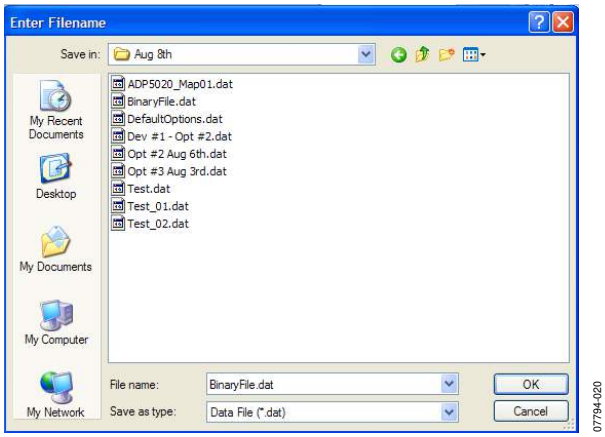


Figure 20. Save Configuration

The **Load Config** button, when clicked, opens the file utility where you can specify the directory and file name to load. The default extension is ***.dat**. If you choose to cancel the operation, an error message appears (see Figure 21). Click **Continue** to abort the operation.

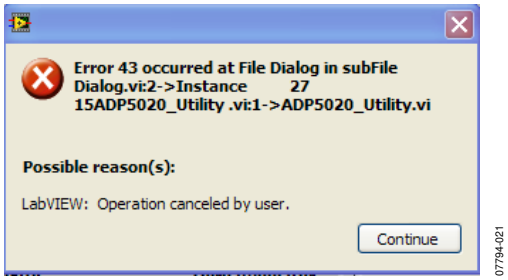


Figure 21. Load/Save Error Message

ADDITIONAL COMMANDS

The **INFO** button, when clicked, provides information regarding the software revision number and other release notes.

The **EXIT** button, when clicked, stops the program, leaving the window active and open. To terminate the program completely, click the close button (**X**) on the upper right corner of the application window.

On-line help is available by selecting **Show Context Help** from the **Help** menu, or by pressing **CTRL** + **H**. Moving the pointer over a control option or indicator displays information related to it in the context help window.

WARNING

Upon starting the ADP5020 application, a dedicated firmware is loaded into the adapter board processor (Cypress IC). This firmware is needed for the operation of the USB adapter and communication with the ADP5020 daughterboard. If the evaluation board is not connected through the USB cable, an error message, as indicated in Figure 15, appears on the screen. This indicates that the firmware was not loaded into the adapter board. If this happens, check the USB connection and ensure that Jumper LK10 is in the USB position. The firmware is loaded in volatile memory inside the Cypress processor; therefore, if power is removed or the USB cable is disconnected, the firmware is lost. If this happens, close the application, connect the adapter board, and then launch the ADP5020 application again to reload the firmware.

It is recommended to always stop the program (click the **EXIT** button) before removing the USB cable.

HISTORY

Whenever a command is issued (both read and write), it is recorded in the **History** dialog box shown in Figure 22.

To display the **History** dialog box, click the **History** button on the bottom right corner of the software GUI (see Figure 14). To clear the history, click **Clear History**.

You can copy and paste the history into a file for future evaluation purposes.

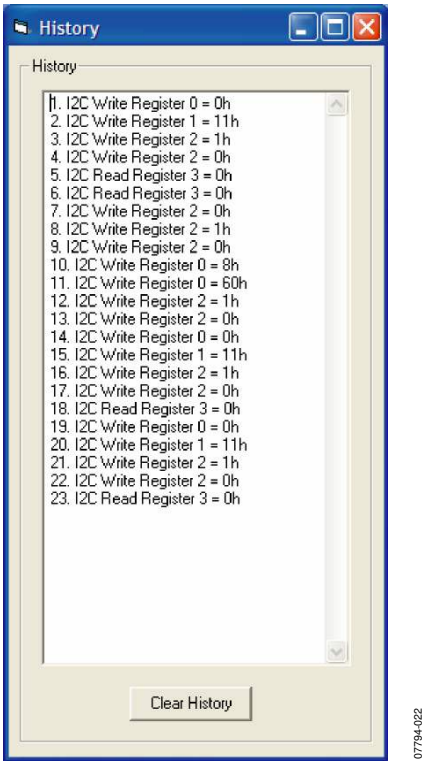


Figure 22. History

EVALUATION BOARD OVERVIEW

MOTHERBOARD

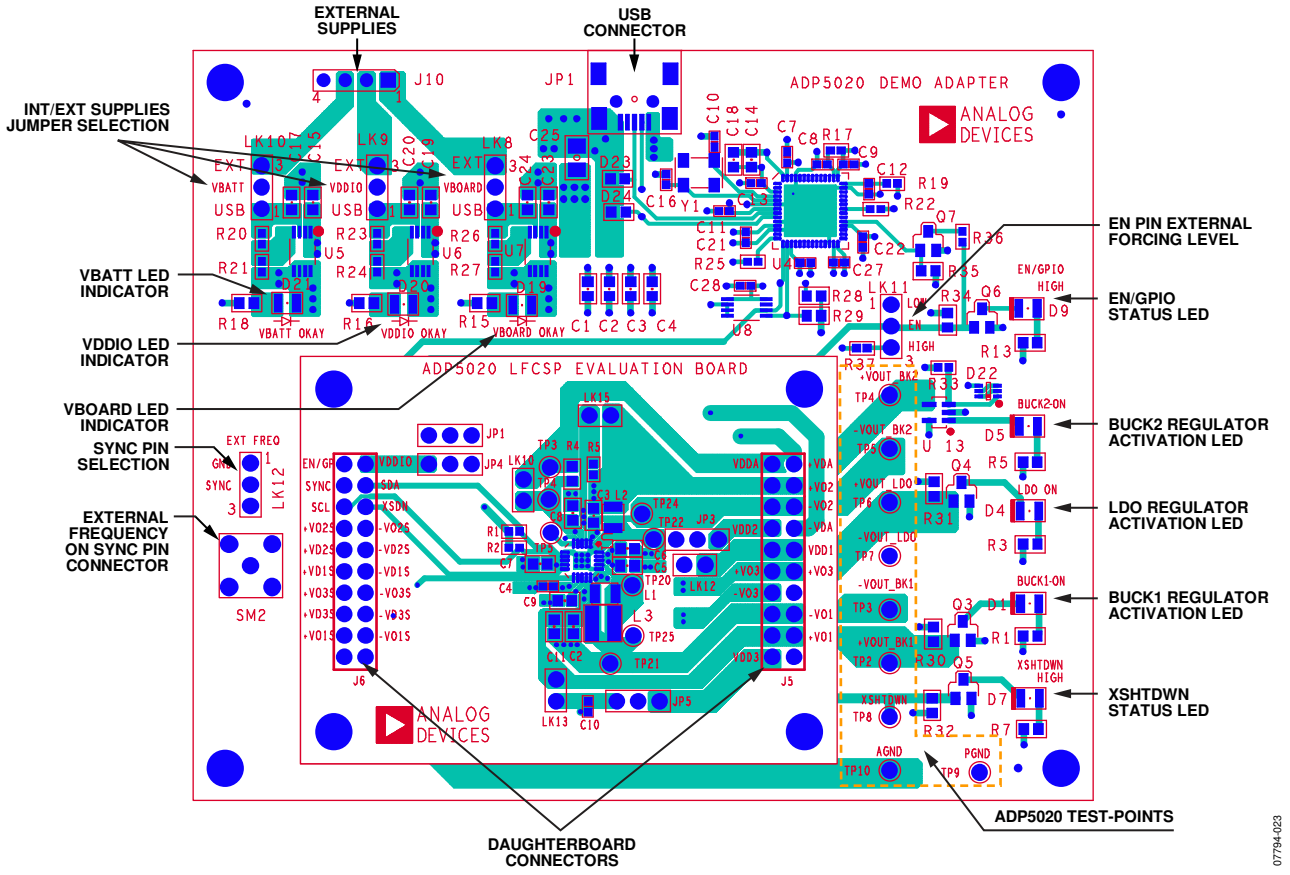


Figure 23. Motherboard

The ADP5020 motherboard provides the interface signals to the ADP5020 power management IC. These include the SDA and SCL lines for I²C, or the control line voltages for the hardware interface modes (EN/GPIO, SYNC, and XSHTDWN).

The Cypress Semiconductor Corporation CY7C68013A provides the USB interface and I²C signals. The selected I²C frequency is 100 kHz. The M24C64R serial EEPROM provides the USB address of the board. The interface voltage is selected with the VBOARD header on the board and is set to 3.3 V by default.

Typically, the daughterboard is inserted directly into the 2 × 20-pin header of the motherboard. For temperature measurements, however, it may be necessary to use an extension cable to connect the motherboard and the daughterboard because the Cypress CY7C68013A is not rated at −40°C. The 8-pin Header J10 on the top of the motherboard can be used to connect external supplies.

The VBATT OKAY, VDDIO OKAY, and VBOARD OKAY LEDs located at the top left of the board lights up when the board is powered from the USB cable, or when external supplies are connected to J10 and Jumper LK8 to Jumper LK10 are set in the EXT position. It is possible to choose several supply combinations. For example, VBOARD, which supplies the motherboard ICs, can be provided from the USB while VDDIO and VBATT are provided externally. The motherboard contains three LDOs generating the default supply voltage, as indicated in Table 1.

Table 1. Power Supply Options

Supply Line	LK8 to LK10 in USB Position	LK8 to LK10 in EXT Position
VBATT	Internal: 3.7 V	External: 2.3 V to 5.5 V
VDDIO	Internal: 2.0 V	External: 1.7 V to 3.6 V
VBOARD	Internal: 3.3 V	External: 2.7 V to 3.6 V

Jumper LK11 defines the forcing level for the EN/GPIO pin. With the jumper in the low position, the EN/GPIO pin is forced to logic low. With the jumper in the high position, the EN/GPIO pin is forced to logic high. The VDDIO supply line determines the logic level.

Jumper LK12 selects the clock mode for the SYNC pin. With the jumper in the GND position, the SYNC pin is tied to ground. With the jumper in the EXT position, an external frequency can be applied to the SYNC pin through Connector SM2. The logic level of the clock signal must be referred to the VDDIO supply level.

DAUGHTERBOARD

The ADP5020 evaluation daughterboard is designed to quickly evaluate key parameters of the ADP5020 IC. The board layout footprint is extended so that parts can be exchanged easily, and headers are available to measure currents using a current probe or ammeter.

Connect a power supply or Li-Ion battery with 2 A capability to VBATT. Up to 1.8 A (nominal) can be drawn from the battery; therefore, short thick cables are recommended to minimize the IR drops. A high current can cause a big IR drop, and VBATT can be low enough to put the part into UVLO.

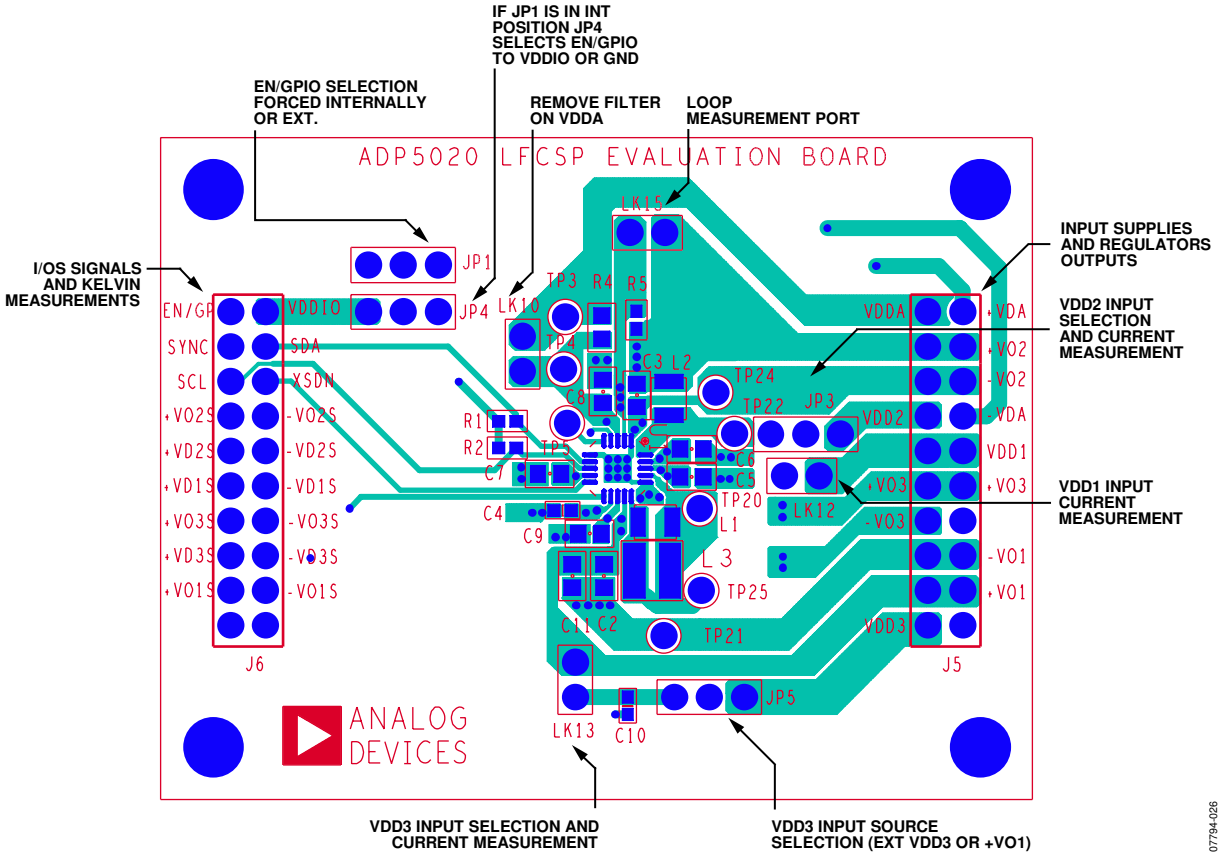


Figure 24. Daughterboard

Quiescent Current Measurement

The ADP5020 has separated supply lines for Buck 1 (V_{DD1}), Buck 2 (V_{DD2}) and LDO (V_{DD3}), in addition to the analog circuit supply (V_{DDA}). The I_{DD1} current can be measured using a current loop across LK12. I_{DD2} can be measured using a current loop across JP3 Position 1 to JP3 Position 2. I_{DD3} can be measured using a current loop across JP5 Position 1 to JP5 Position 2. I_{DDA} can be measured using a current loop across JP10. R4 must be removed.

Regulator Switching Nodes

The Buck 1 switching frequency can be measured on TP25 (SW1). TP21 is a local power ground that can be used to con-nect the scope probe to minimize the switching noise pickup.

Buck 2 switching frequency can be measured on TP22. TP24 is a local power ground that can be used to connect the scope probe to minimize the switching noise pickup.

Kelvin Measurements

The input and output voltages are routed to Connector J6 using Kelvin connections, meaning that the point of measurement is directly on the capacitor pads. This minimizes the measurement error due to IR drop from the trace resistance. Table 2 and Table 3 show the signals available on Connector J6 and Connector J5, respectively.

Power Board from USB Port Only

To power the board via the USB without using an external supply, short Jumper LK10 on the motherboard (USB position). Avoid exceeding the 500 mA current limit of the USB.

Table 2. Measurement Signals on J6

Signal	J6 Pins	Description
EN/GPIO	20	EN/GPIO pin from IC
VDDIO	19	ADP5020 logic supply
SYNC	18	External frequency
SDA	17	I^2C bidirectional line
SCL	16	I^2C clock line
XSHTDWN	15	XSHTDN pin from IC
+VO2S, VO2S	14, 13	Buck 2 output voltage (+/–)
+VD2S, –VD2S	12, 11	Buck 2 input voltage (+/–)
+VD1S,–VD1S	10, 9	Buck 1 input voltage (+/–)
+VO3S, –VO3S	8, 7	LDO output voltage (+/–)
+VD3S, –VD3S	6, 5	LDO input voltage (+/–)
+VO1S, –VO1S	4, 3	Buck 1 output voltage (+/–)
GND	2	Ground plane and digital grounds

Table 3. Measurement Signals on J5

Signal	J5 Pins	Description
VDDA	20	Analog supply input
+VDA, –VDA	19, 13	VDDA input voltage (+/–)
+VO2	18, 17	Buck 2 output positive voltage
–VO2	16, 15	Buck 2 output negative voltage
VDD2	14	Buck 2 input voltage
VDD1A, VDD1B	12, 11	Buck 1 input voltage
+VO3	10, 9	LDO output voltage (+)
–VO3	8	LDO output voltage (–)
–VO1	6, 5	Buck 1 output voltage (–)
+VO1	4, 3	Buck 1 output voltage (+)
VDD3	2	LDO input voltage
GND	7, 1	Ground plane and digital grounds

EVALUATION BOARD SCHEMATICS

MOTHERBOARD SCHEMATICS

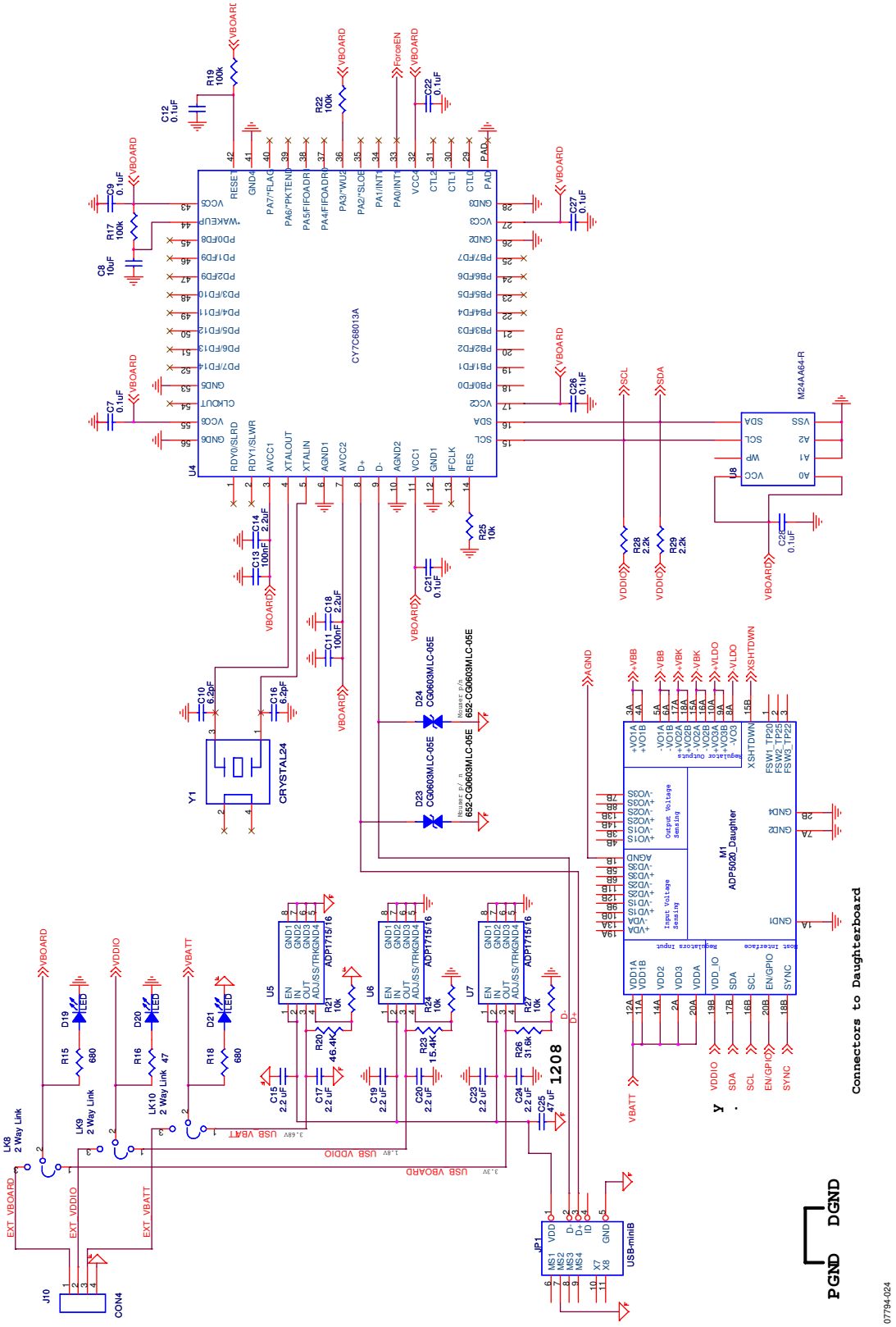


Figure 25. Motherboard Schematic—Main Section

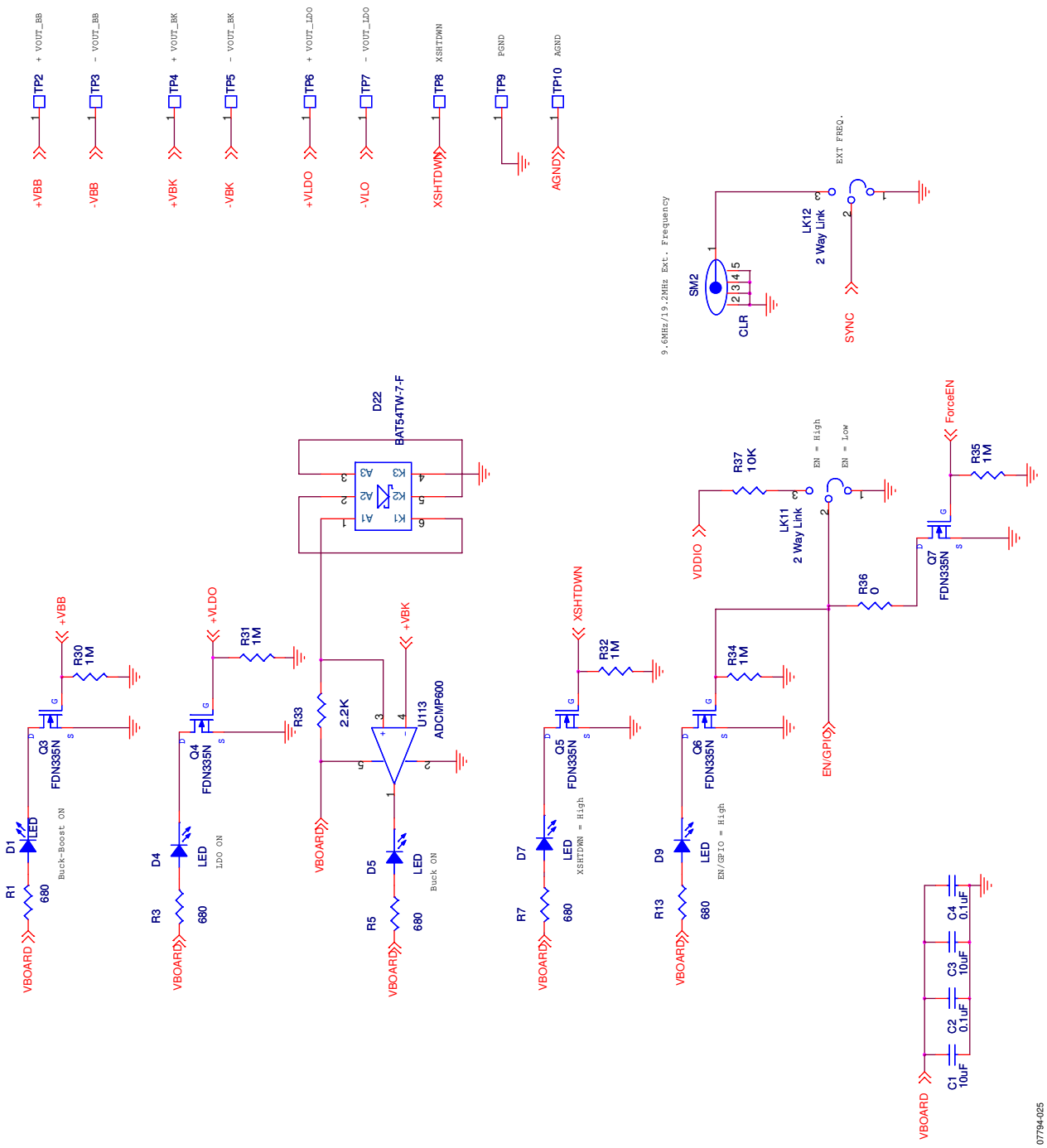


Figure 26. Motherboard Schematic—Interface Section

DAUGHTERBOARD SCHEMATIC

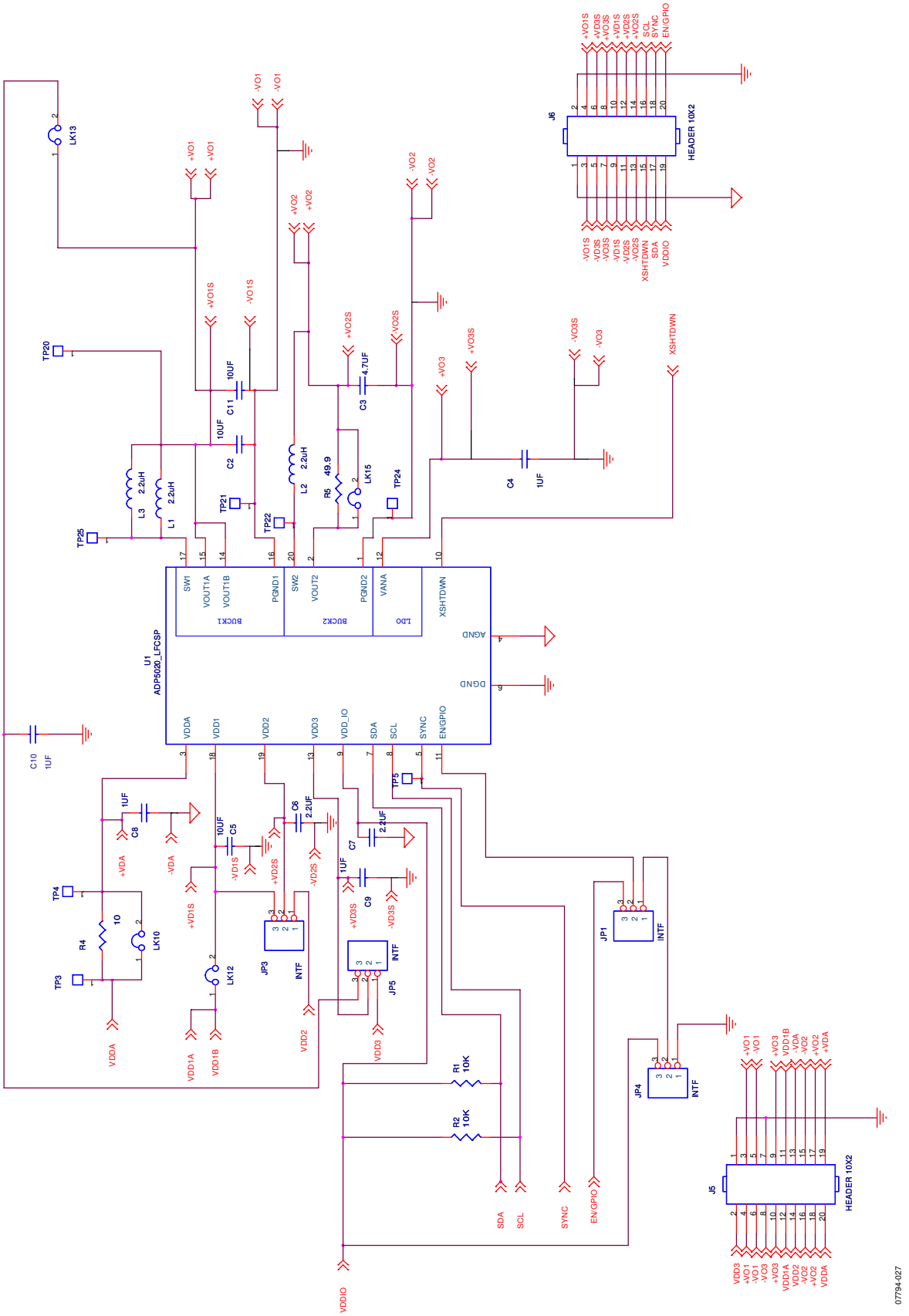


Figure 27. Daughterboard Schematic

PCB LAYOUT

Evaluation Board Layout

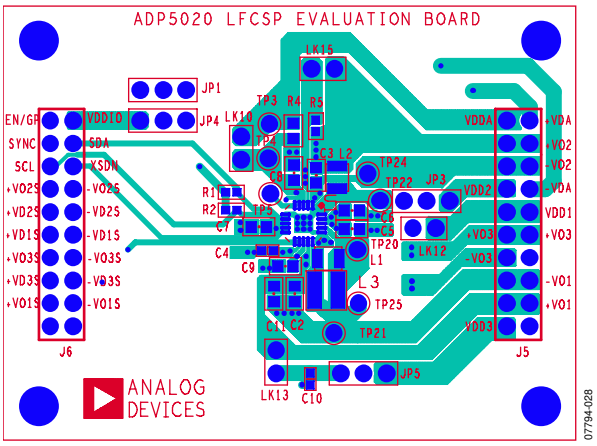


Figure 28. Top Layer

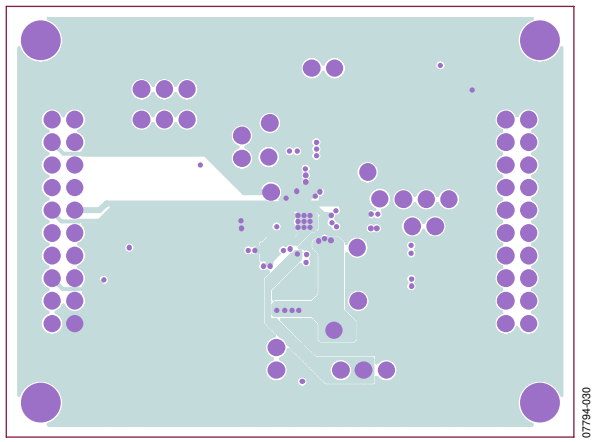


Figure 30. Inner Layer 2

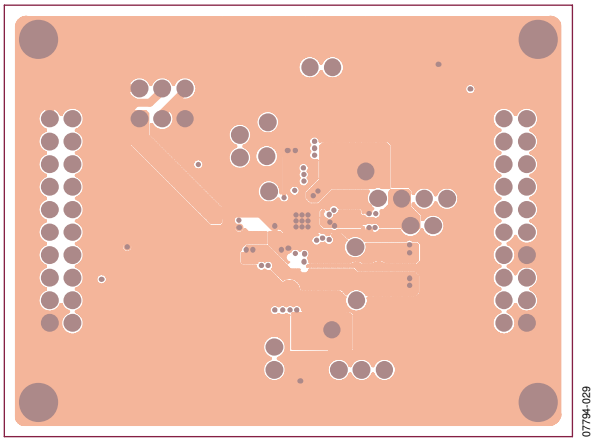


Figure 29. Inner Layer 1

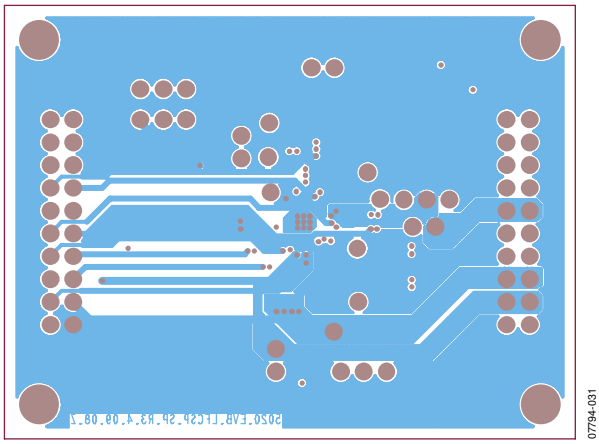


Figure 31. Bottom Layer

Motherboard Layout

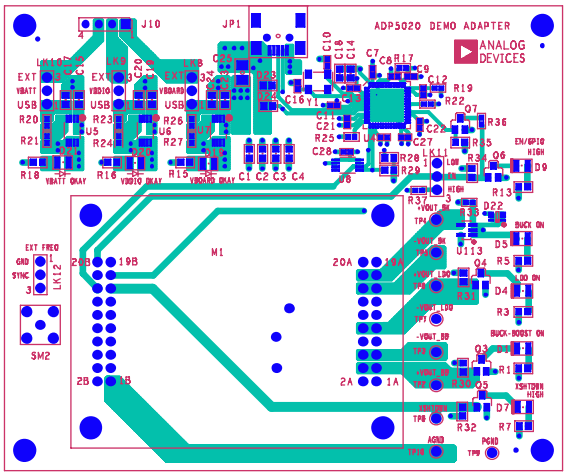


Figure 32. Top Layer

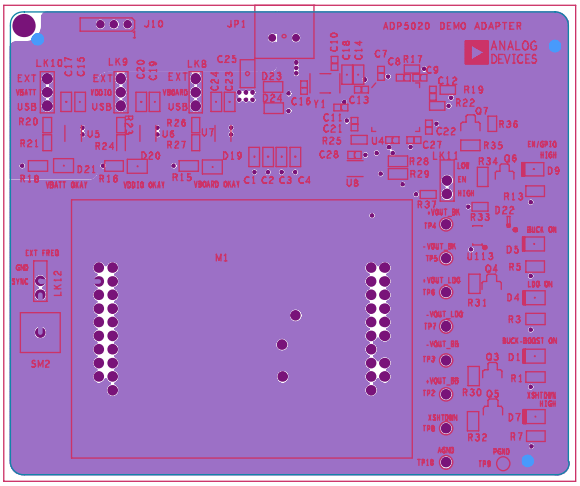


Figure 33. Inner Layer 1

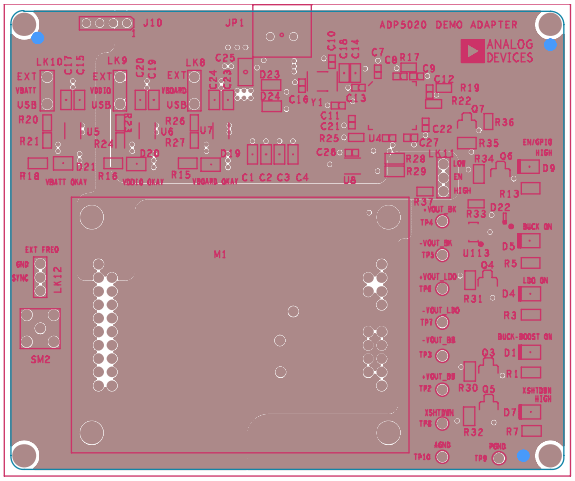


Figure 34. Inner Layer 2

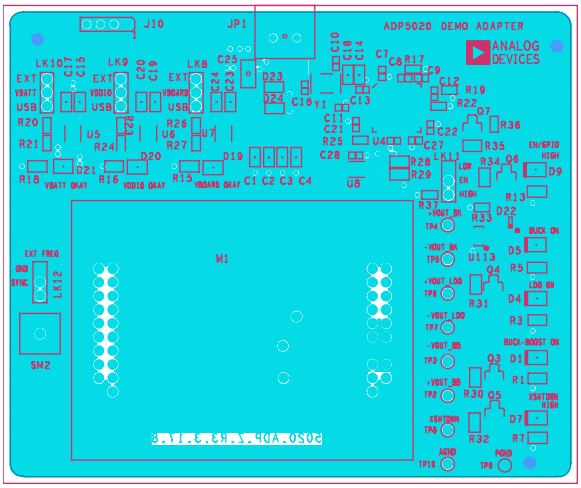


Figure 35. Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Description	Reference Designator	Qty	Manufacturer/Vendor	Part Number
Daughterboard				
Capacitor, MLCC, 10 µF, 6.3 V, 0603, X5R	C2, C5, C11	3	Taiyo Yuden	JMK107BJ106MA
Capacitor, MLCC, 1 µF, 6.3 V, 0402, X5R	C4	1	Taiyo Yuden	LMK105BJ105MV
Capacitor, MLCC, 4.7 µF, 6.3 V, 0603, X5R	C3	1	Taiyo Yuden	JMK107BJ475MA
Capacitor, MLCC, 2.2 µF, 6.3 V, 0402, X5R	C6, C7	2	Taiyo Yuden	JMK105BJ225MV
Capacitor, MLCC, 1 µF, 6.3 V, 0402, X5R	C8, C9, C10	3	Panasonic	ECJ-1VF1A105Z
Inductor, 2.2 µH	L1	1	Taiyo Yuden	BRL2518T2R2M
Inductor, 2.2 µH	L2	1	Taiyo Yuden	BRL2012T2R2M
Inductor, 2.2 µH	L3 (alternative to L1)	1	Coilcraft	LPS4012
Resistor, 10 kΩ, 1%, 0402	R1, R2	2	Vishay Dale	CRCW04021002F
Resistor, 10 Ω, 1%, 0403	R4	1	Panasonic	ERJ-3EKF10
Resistor, 49.9 Ω, 1%, 0404	R5	1	Panasonic	ERJ-2RKF49.9
ADP5020, 20-Lead LFCSP, 4 mm × 4 mm	U1	1	Analog Devices, Inc.	ADP5020
Header 0.100, Double-Row 10 Pins	J5, J6	2	SAMTEC	SSW-110-03-G-D
Header 0.100, Single, STR, 2 Pins	LK10, LK12, LK13, LK15	4	Sullins Electronics, Inc./3M	S1012-36-ND
Header 0.100, Single, STR, 3 Pins	JP1, JP3 to JP5	4	Sullins Electronics, Inc./3M	S1012-36-ND
Motherboard				
Capacitor, MLCC, 100 nF, 10 V, 0402, X5R	C2, C4, C7, C9, C11, C13, C12, C21, C22, C26, C27, C28	11	Murata Manufacturing Co., Ltd.	GRM155R61A104KA01B
Capacitor, MLCC, 10 µF, 6.3 V, 0805, X5R	C1, C3, C8	3	Murata Manufacturing Co., Ltd.	GRM21BR60J106K
Capacitor, MLCC, 6.2 pF, 0402, NP0	C10, C16	2	Vishay/Panasonic	ECJ-OEC1H0600
Capacitor, MLCC, 2.2 µF, 10 V, 0603, X5R	C14, C15, C17, C18, C19, C20, C23, C24	8	Murata Manufacturing Co., Ltd.	GRM188R61A225K
Capacitor, MLCC, 47 µF, 6.3 V, 1206, X5R	C25	1	Murata Manufacturing Co., Ltd.	GRM32ER61C476K
Red LED, 0402, SMD	D4, D19, D21,	3	Lumex Inc.	SML-LX0402SIC-TR
Green LED, 0402, SMD	D1, D5, D20	3	Lumex Inc.	SML-LX0402SUGC-TR
White LED, 0402, SMD	D7, D9	2	Lumex Inc.	LTW-170TK
Triple Schottky Diode, SC70	D22	1	Diodes, Inc.	BAT54TW-7-F
USB ESD Protector	D23, D24	2	Bourns	CG0603MLC-05E
Resistor, 680 Ω, 1%, 0402, SMD	R1, R3, R5, R7, R13, R15, R18	7	Vishay Dale or equivalent	CRCW04026810F
Resistor, 47 Ω, 1%, 0402, SMD	R16	1	Vishay Dale or equivalent	CRCW04024700F
Resistor, 100 kΩ, 1%, 0402, SMD	R17, R19, R22	3	Vishay Dale or equivalent	CRCW04021003F
Resistor, 15.4 kΩ, 1%, 0402, SMD	R23	1	Vishay Dale or equivalent	CRCW04021542F
Resistor, 31.6 kΩ, 1%, 0402, SMD	R26	1	Vishay Dale or equivalent	CRCW04023162F
Resistor, 0 Ω, 1%, 0402, SMD	R36	1	Vishay Dale or equivalent	CRCW04020000Z0ED
Resistor, 1 MΩ, 1%, 0402, SMD	R30, R31, R32, R34, R35	5	Vishay Dale or equivalent	CRCW04021004F
Resistor, 10 kΩ, 1%, 0402, SMD	R21, R24, R25, R27, R37	5	Vishay Dale or equivalent	CRCW040210022F
Resistor, 2.2 kΩ, 1%, 0402, SMD	R28, R29, R33	3	Vishay Dale or equivalent	CRCW040222021F
Resistor, 46.4 kΩ, 1%, 0402, SMD	R20	1	Vishay Dale or equivalent	CRCW04024642FF
IC MCU USB Periph High SPD-56QFN	U4	1	Cypress Semiconductor Corp	CY7C68013A
Microchip Serial EEPROM-64K, MSOP8	U8	1	Microchip	M24LC64 or 24AA64
IC Comparator	U113	1	Analog Devices	ADCMP600

Description	Reference Designator	Qty	Manufacturer/Vendor	Part Number
IC LDO Regulator, 500 mA, 8-Lead MSOP	U5, U6, U7	3	Analog Devices	ADP1715/16
Crystal 24 MHz	Y1	1	CTS Corporation	CTX651CT
MOSFET N-Channel, SOT23	Q3, Q4, Q5, Q6, Q7	5	Fairchild	FDN335N
USB Connector USB Mini B, 5p	JP1	1	Delphi Corporation/Molex	15430262-110
Header, Male 0.100, Dual, STR, 2 × 10 Pins	M1	2	Sullins Connector Solutions	PTC10SAAN
Header 0.100, Single, STR, 3 Pins	LK8, LK9, LK10, LK11, LK12	5	Sullins Connector Solutions	PEC03SAAN
Header 0.100, Single, STR, 4 Pins	J10	1	Sullins Electronics, Inc.	PEC36SAAN
SMB Connector, Receptacle	SM2	1	Emerson Network Power Connectivity Solution	131-3701-266

ORDERING GUIDE

Model	Description
ADP5020CP-EVALZ[1]	Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

NOTES

EB07794-0-5/09(0)