Integrated Device Technology, Inc.	64K/128K/256K/512K x 36 SYNCHRONOUS SRAM MODULE FAMILY	PRELIMINARY IDT7MPV4160 IDT7MPV4161 IDT7MPV4162 IDT7MPV4162A IDT7MPV4163

FEATURES:

- Pin compatible flow-through synchronous SRAM module family
- 144 position SO-DIMM Connector,
  – Berg part number: 61178
- As fast as 9ns Clk to Data Times
- All Inputs and Outputs are LVTTL Compatible
- Multiple Clock Pins for Reduced Loading
- Byte Write Capability
- Single 3.3V power supply (±5%)
- Multiple GND pins and decoupling capacitors for maximum noise immunity

DESCRIPTION:

The IDT7MPV416 module family consists of the following members:

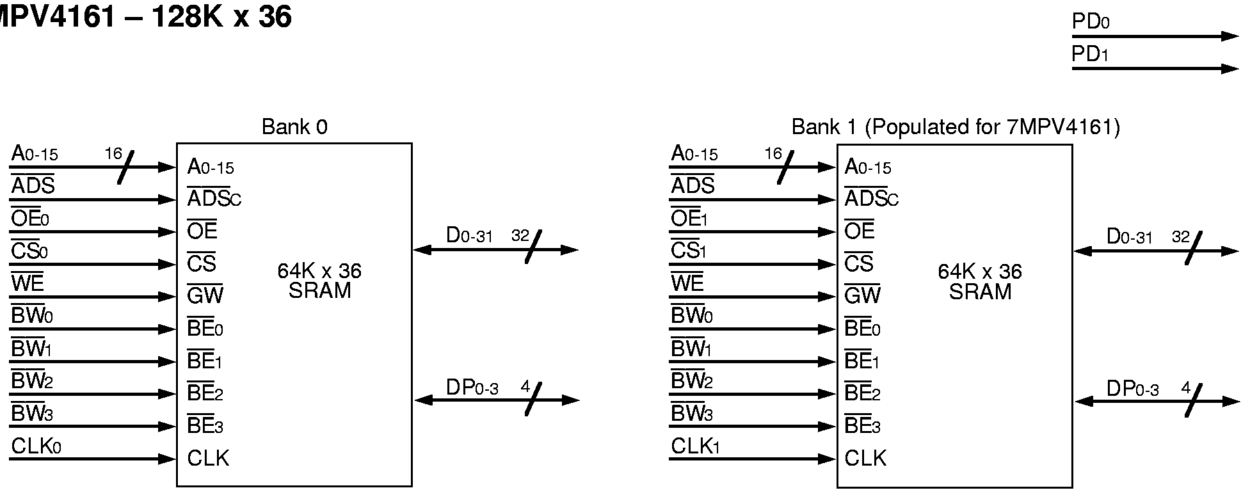
Module	Configuration	Base SRAM
7MPV4160	64K x 36	64K x 36
7MPV4161	128K x 36	64K x 36
7MPV4162	256K x 36	256K x 18
7MPV4162A	256K x 36	128K x 18
7MPV4163	512K x 36	256K x 18

4055 tbl 01

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 100 micro-inches of nickel covered by 30 micro-inches of selective deep gold plating.

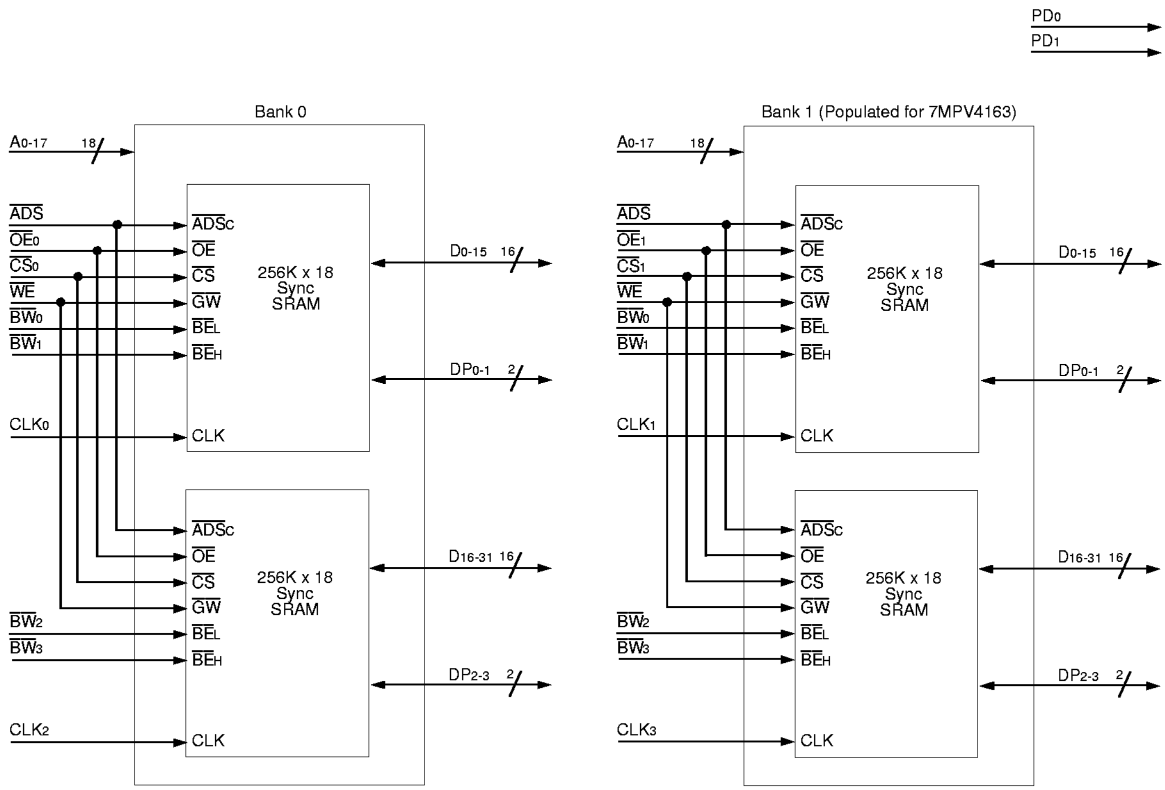
FUNCTIONAL BLOCK DIAGRAM
IDT7MPV4160 – 64K x 36
IDT7MPV4161 – 128K x 36



4055 dwg 01

NOTE:
1. D_0 - D_7 and DP_0 are associated with $\overline{BW_0}$, D_8 - D_{15} and DP_1 are associated with $\overline{BW_1}$, D_{16} - D_{23} and DP_2 are associated with $\overline{BW_2}$, and D_{24} - D_{31} and DP_3 are associated with $\overline{BW_3}$.

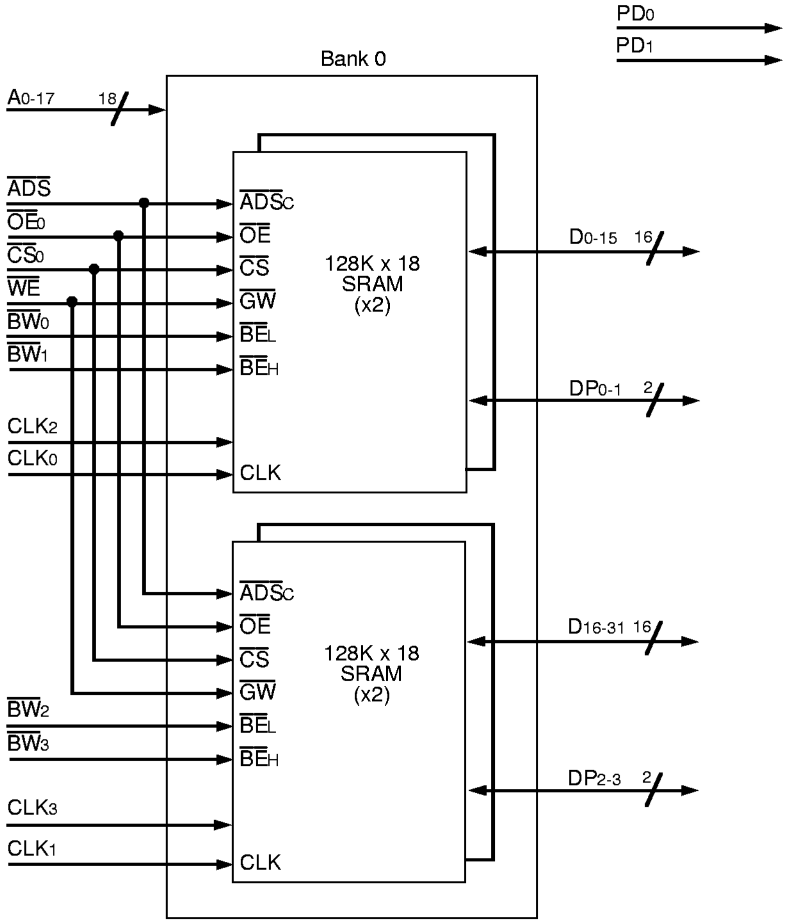
FUNCTIONAL BLOCK DIAGRAM
IDT7MPV4162 – 256K x 36
IDT7MPV4163 – 512K x 36



4055 dwg 02A

NOTE:
1. D_0 - D_7 and DP_0 are associated with $\overline{BW}_0$, D_8 - D_{15} and DP_1 are associated with $\overline{BW}_1$, D_{16} - D_{23} and DP_2 are associated with $\overline{BW}_2$, and D_{24} - D_{31} and DP_3 are associated with $\overline{BW}_3$.

FUNCTIONAL BLOCK DIAGRAM
IDT7MPV4162A – 256K x 36



NOTE:

1. D_0 - D_7 and DP_0 are associated with $\overline{BW}_0$, D_8 - D_{15} and DP_1 are associated with $\overline{BW}_1$, D_{16} - D_{23} and DP_2 are associated with $\overline{BW}_2$, and D_{24} - D_{31} and DP_3 are associated with $\overline{BW}_3$.

PIN NAMES

$A_0 - A_{17}$	Address Inputs
$D_0 - D_{31}$	Data Inputs/Outputs
$DP_0 - DP_3$	Data Parity Inputs/Outputs
$\overline{CS}_{0-1}$	Chip Select Inputs
$\overline{OE}_{0-1}$	Data Output Enable Inputs
$\overline{BW}_0 - \overline{BW}_3$	Data Write Enable Inputs
CLK_{0-3}	Clock Inputs
$\overline{ADS}$	Address Status Inputs
$\overline{WE}$	Global Write Input
RES	Reserved Pins
NC	No Connect
PD_0-PD_1	Presence Detect Pins
GND	Ground
V_{CC}	3.3 Volt Power Supply

4055 tbl 02

PRESENCE DETECT PINS

Configuration	**PD_1**	**PD_0**
IDT7MPV4160 - 64Kx36	GND	NC
IDT7MPV4161 – 128K x 36	NC	GND
IDT7MPV4162 – 256K x 36	GND	GND
IDT7MPV4162A - 256K x 36	GND	GND
IDT7MPV4163 – 512K x 36	NC	NC

4055 tbl 03

MODULE PINOUT

GND	1	2	GND
A_0	3	4	A_1
A_2	5	6	A_3
A_4	7	8	A_5
V_{CC}	9	10	V_{CC}
(1) RES	11	12	RES (1)
(1) RES	13	14	RES (1)
GND	15	16	GND
A_6	17	18	A_7
A_8	19	20	A_9
A_{10}	21	22	A_{11}
NC	23	24	NC
V_{CC}	25	26	V_{CC}
A_{12}	27	28	A_{13}
A_{14}	29	30	A_{15}
A_{16}	31	32	A_{17}
GND	33	34	GND
PD_0	35	36	PD_1
GND	37	38	GND
$\overline{BW}_0$	39	40	$\overline{BW}_1$
$\overline{CS}_0$	41	42	$\overline{OE}_0$
GND	43	44	GND
CLK_1	45	46	CLK_0
GND	47	48	GND
D_0	49	50	D_1
V_{CC}	51	52	V_{CC}
D_2	53	54	D_3
D_4	55	56	D_5
D_6	57	58	D_7
GND	59	60	GND
V_{CC}	61	62	V_{CC}
D_8	63	64	D_9
D_{10}	65	66	D_{11}
GND	67	68	GND
D_{12}	69	70	D_{13}
D_{14}	71	72	D_{15}
DP_0	73	74	DP_1
(1) RES	75	76	RES (1)
(1) RES	77	78	RES (1)
GND	79	80	GND
$\overline{WE}$	81	82	$\overline{ADS}$
NC	83	84	NC
V_{CC}	85	86	V_{CC}
NC	87	88	NC
NC	89	90	NC
NC	91	92	NC
V_{CC}	93	94	V_{CC}
NC	95	96	NC
NC	97	98	NC
NC	99	100	NC
GND	101	102	GND
$\overline{BW}_2$	103	104	$\overline{BW}_3$
$\overline{CS}_1$	105	106	$\overline{OE}_1$
V_{CC}	107	108	V_{CC}
D_{16}	109	110	D_{17}
D_{18}	111	112	D_{19}
NC	113	114	NC
NC	115	116	NC
NC	117	118	NC
GND	119	120	GND
CLK_3	121	122	CLK_2
GND	123	124	GND
D_{20}	125	126	D_{21}
GND	127	128	GND
D_{22}	129	130	D_{23}
D_{24}	131	132	D_{25}
D_{26}	133	134	D_{27}
D_{28}	135	136	D_{29}
V_{CC}	137	138	V_{CC}
D_{30}	139	140	D_{31}
DP_2	141	142	DP_3
GND	143	144	GND

SO-DIMM
TOP VIEW

4055 drw 03

NOTES:
1. These pins are No Connects; they are reserved for future modules.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 5%

4055 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.15	3.3	3.45	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 4055 tbl 05

1. V_{IL} = –1.0V for pulse width less than $t_{CYC}/2$, once per cycle.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM} for V_{CC}	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 4055 tbl 06

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 3.3V ± 5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS} \geq V_{IH}$, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –2 mA, V_{CC} = Min.	2.4	—	V

4055 tbl 07

Symbol	Parameter	Test Condition	'4160	'4161	'4162	'4162A	'4163	Unit
I_{CC}(3)	Operating Power Supply Current	$\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	330	390	600	860	930	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	60	120	330	520	660	mA

NOTES: 4055 tbl 08

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address inputs are switching at $1/t_{CYC}$ and CLK is cycling at $1/t_{CYC}$; f=0 means no input signals are changing.
3. I_{CC} specification for the 7MPV4161, 7MPV4162A, 7MPV4162A, and 7MPV4163 assumes that only one bank is selected.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	'4160 Max.	'4161 Max.	'4162 Max.	'4162A Max.	'4163 Max.	Unit
C_{IN1}	Input Capacitance Address, $\overline{ADS}$, $\overline{WE}$	V_{IN} = 3dV	10	20	20	35	35	pF
C_{IN2}	Input Capacitance $\overline{OE}$, $\overline{CS}$	V_{IN} = 3dV	10	10	20	35	20	pF
C_{IN3}	Input Capacitance $\overline{BW}_{0-3}$	V_{IN} = 3dV	10	20	10	20	20	pF
C_{INCLK}	Input Capacitance Clock	V_{IN} = 3dV	10	10	10	10	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	10	20	10	20	20	pF

NOTE: 4055 tbl 09

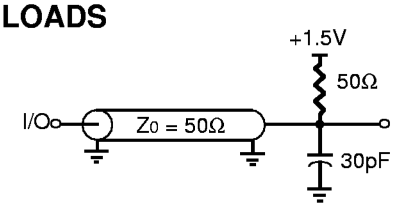
1. This parameter is guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

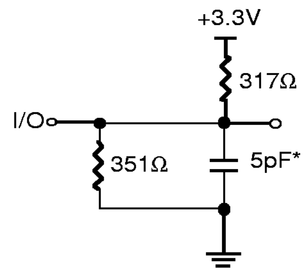
4055 tbl 09

AC TEST LOADS



4055 drw 04

Figure 1. AC Test Load

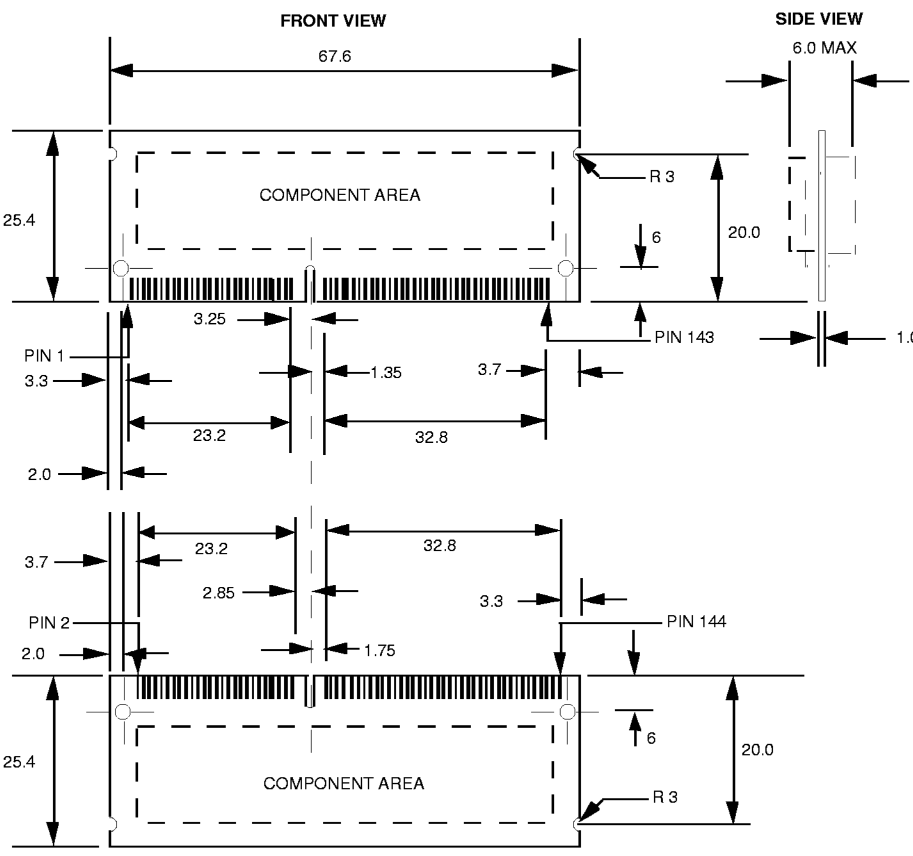


4055 drw 05

Figure 2. AC Test Load
(for t_{OHZ}, t_{CHZ}, t_{OLZ}, and t_{DC1})

* Including scope and jig

PACKAGE DIMENSIONS



4055 dwg 06

NOTES:
1. All dimensions are in millimeters.
2. Dimensions conform to the small outline DIMM 144 position connector from Berg (part number 61178).
3. Tolerances on all dimensions are ±0.15mm.

ORDERING INFORMATION

IDT XXXXX X X X X

Field	Code	Description
Device Type	7MPV4160	64K x 36 Flow-through Sync SRAM Module
	7MPV4161	128K x 36 Flow-through Sync SRAM Module
	7MPV4162	256K x 36 Flow-through Sync SRAM Module
	7MPV4162A	256K x 36 Flow-through Sync SRAM Module
	7MPV4163	512K x 36 Flow-through Sync SRAM Module
Power	S	Standard Version
	SA	Alternate Version (Based on 128K x 18's)
Speed	9 10 11 12	Clock-to-Data-Out Time in Nanoseconds (speed of the SRAMs used on the module)
Package	M	144 Position SO-DIMM
Process/ Temperature Range	Blank	Commercial (0°C to +70°C)

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