HARRIS SEMICONDUCTOR

HSP50306

January 1997

Digital QPSK Demodulator

Features

- 25.6MHz or 26.97MHz Clock Rates
- Single Chip QPSK Demodulator with 10kHz Tracking Loop
- Square Root of Raised Cosine (α = 0.4) Matched Filtering
- 2.048 MBPS Reconstructed Output Data Stream
- Bit Synchronization with 3kHz Loop Bandwidth
- Internal Equalization for Multipath Distortion
- 6-Bit Real Input: Digitized 10.7MHz or 2.1MHz IF
- Level Detection for External IF AGC Loop
- 0.1s Acquisition Time
- 10^{-9} BER
- <116mA on +5.0V Supply

Applications

- Cable Data Link Receivers
- Cable Control Channel Receivers

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP50306SC-27	0 to 70	16 Ld SOIC	M16.3
HSP50306SC-2796	0 to 70	Tape and Reel	
HSP50306SC-25	0 to 70	16 Ld SOIC	M16.3
HSP50306SC-2596	0 to 70	Tape and Reel	

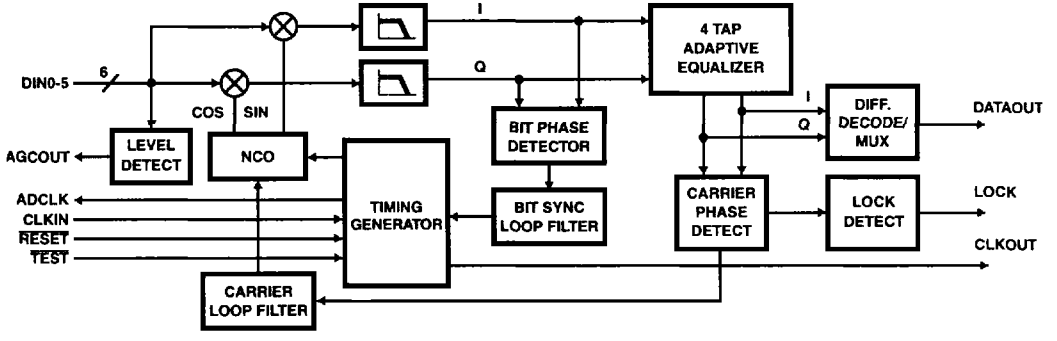
Description

The HSP50306 is a 6-bit QPSK demodulator chip designed for use in high signal to noise environments which have some multipath distortion. The part recovers 2.048 MBPS data from samples of a QPSK modulated 10.7MHz or 2.1MHz carrier. The chip coherently demodulates the waveform, recovers symbol timing, adaptively equalizes the signal to remove multipath distortion, differentially decodes and multiplexes the data decisions. A lock signal is provided to indicate when the tracking loops are locked and the data decisions are valid. To optimize performance, a gain error feedback signal is provided which can be filtered and used to close an I.F. AGC loop around the A/D converter.

The QPSK demodulator derives all timing from CLKIN. The chip divides this clock by 2 to provide the sample clock for the external A/D converter. The -27 version operates at a clock input of 26.97MHz and demodulates a 10.7MHz QPSK signal to recover the 2048 KSPS data. The -25 version operates at a clock input of 25.6MHz and demodulates a 2.1MHz QPSK signal to recover the 2048 KSPS data. Variation from these CLKIN frequencies will progressively degrade the receive data rate, the receive IF, acquisition sweep rate, acquisition sweep range and loop bandwidths as the deviation increases from normal CLKIN. Details on the maximum allowable deviation are found in the Input Characteristics section. The HSP50306 processes 6-bit offset binary data. 4-bit data provides adequate performance for many applications.

The block diagram of the QPSK Demodulator is shown below. To demodulate the data, the I.F. samples are multiplied by sine and cosine samples from a numerically controlled oscillator. The digital mixer outputs are then low pass filtered to remove mixer products. The filtered data is then equalized by a 4 tap equalizer (1 precursor, one reference tap, and a 2 tap Decision Feedback Equalizer (DFE)) to remove distortion caused by multipath. The output of the equalizer is differential decoded and multiplexed into the output data

Block Diagram



5 STANDARD PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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