

## LTC3308A 5V Input to 1.2V Output at 4A Synchronous Step-Down Silent Switcher Demo Circuit

### DESCRIPTION

Demonstration circuit 2991A features the [LTC®3308A](#) 5V, 4A synchronous step-down Silent Switcher® operating as a 2.0MHz, 3.3V to 1.2V 4A buck regulator. The LTC3308A supports adjustable output voltages from 0.5V to  $V_{IN}$  with operating frequencies from 1MHz up to 3MHz. The LTC3308A is a compact, ultralow emission, high efficiency, and high speed synchronous monolithic step-down switching regulator. A minimum on-time switching of 22ns enables high  $V_{IN}$  to low  $V_{OUT}$  conversion ratios at high frequencies.

The DC2991A operating mode may be selected as BURST, SKIP or Forced Continuous (FC) mode. Setting JP1 to the FC/SYNC position will allow the LTC3308A to sync to a clock frequency from 1MHz to 3MHz. The LTC3308A operates in forced continuous mode when syncing to an external clock. The DC2991A is set to a fixed 2MHz frequency by connecting RT to  $V_{IN}$  through a  $0\Omega$  resistor, R9. The frequency can be easily changed by removing R9 and setting an appropriate resistor in the R4 location to obtain the desired frequency. Refer to the LTC3308A data sheet for the proper RT value for a desired switching frequency.

The DC2991A also has an EMI filter to reduce conducted EMI. This EMI filter can be included by applying the input voltage at the  $V_{IN}$  EMI terminal. The EMI performance of the board is shown in the EMI Test Results section. The red lines in the EMI performance graphs illustrate the CISPR25 Class 5 peak limits for the conducted and radiated emission tests.

The LTC3308A data sheet gives a complete description of the device, operation and application information. The data sheet must be read in conjunction with this demo manual. The LTC3308A is assembled in a 2mm × 2mm LQFN package with exposed pads for low thermal resistance. The layout recommendations for low EMI operation and maximum thermal performance are available in the data sheet section: Low EMI PCB Layout.

The Efficiency vs Load graph shows the efficiency and the power loss of the circuit with a 3.3V input in Burst Mode operation.

[Design files for this circuit board are available.](#)

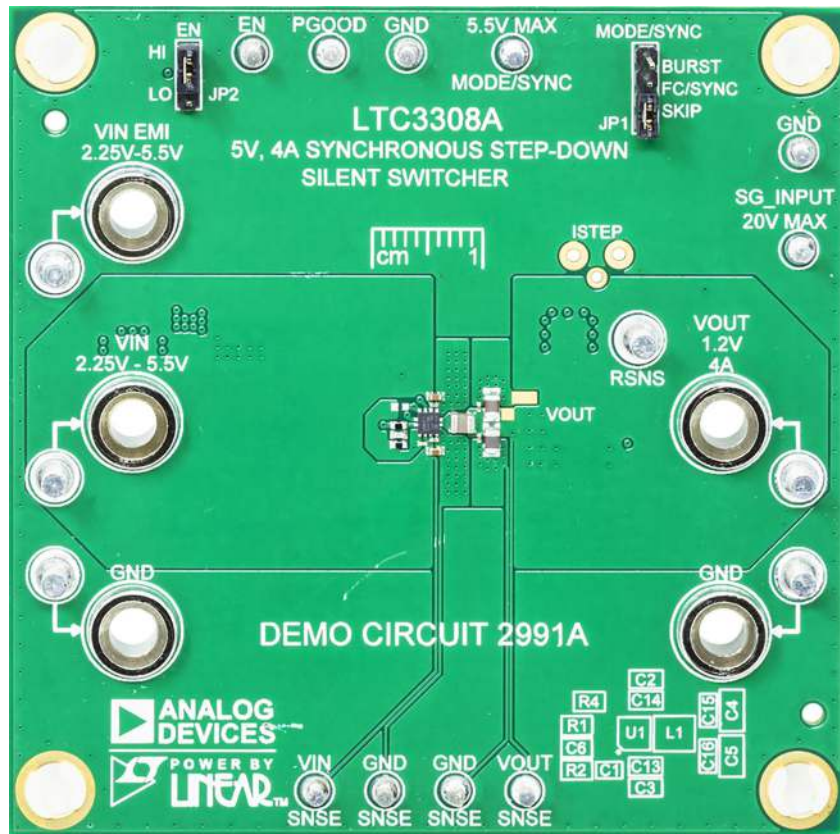
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### PERFORMANCE SUMMARY Specifications are at $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN}$	Input Voltage Range		2.25		5.5	V
$V_{OUT}$	$V_{OUT}$ Voltage Range*		1.183	1.2	1.217	V
$I_{OUT}$	Output Current				4	A
$f_{SW}$	Switching Frequency	$V_{IN}$ Greater than $V_{OUT}$	1		3	MHz
$T_{ON}$	Top Switch Minimum On-Time			22		ns
Duty Cycle	Top Switch Duty Cycle				100	%

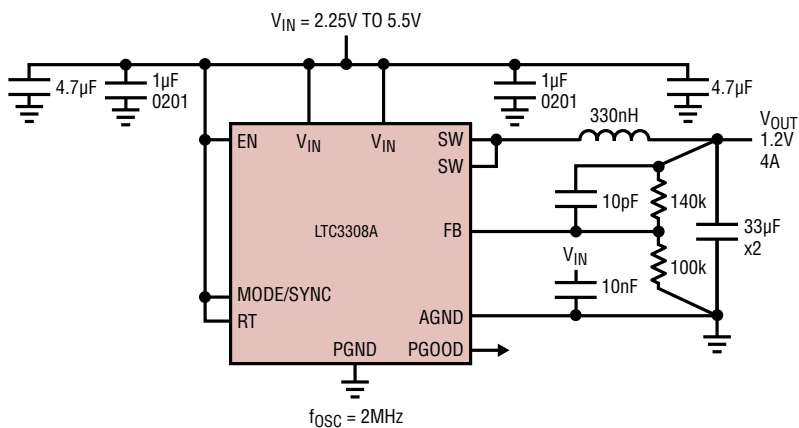
\*With 1% resistors. Accuracy will improve to within 1% using 0.1% resistors.

## BOARD PHOTO

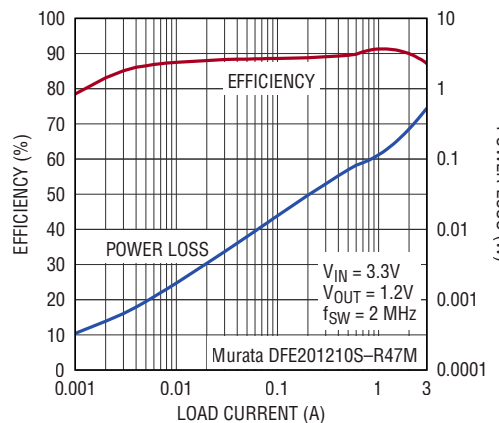


## CIRCUIT SCHEMATIC

High Efficiency, 2MHz, 1.2V 4A Step-Down Converter

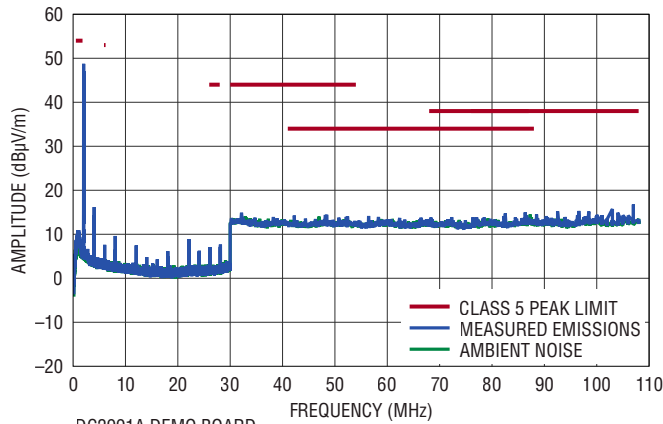


Efficiency and Power Loss in Burst Mode Operation



## EMI TEST RESULTS

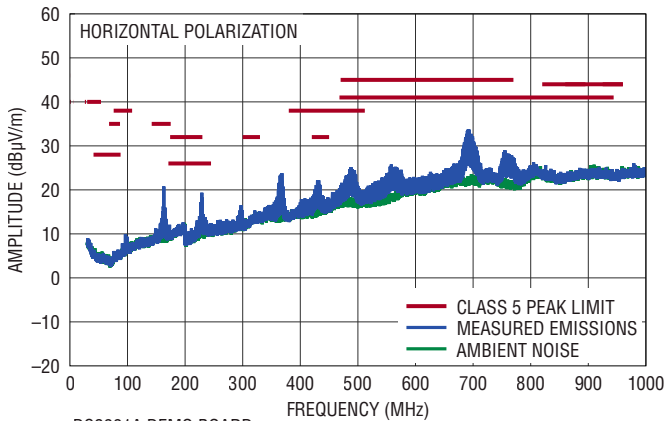
### Conducted EMI Performance (CISPR25 Conducted Emission Test with Class 5 Peak Limits)



DC2991A DEMO BOARD  
(WITH EMI FILTER INSTALLED)  
3.3V INPUT TO 1.2V OUTPUT AT 3.2A,  $f_{SW} = 2\text{MHz}$

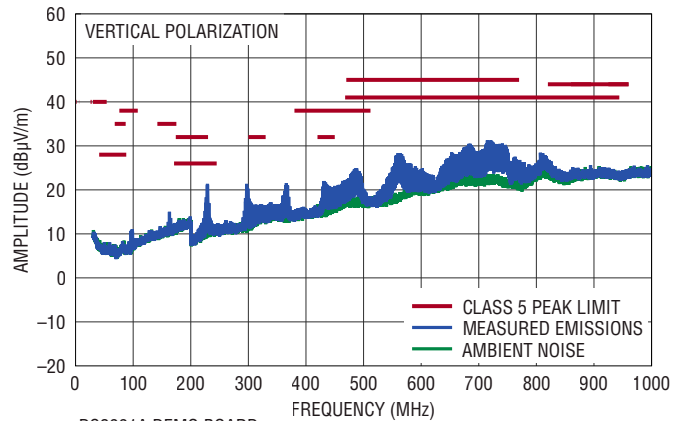
dc2991A G01

### Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



DC2991A DEMO BOARD  
(WITH EMI FILTER INSTALLED)  
3.3V INPUT TO 1.2V OUTPUT AT 3.2A,  $f_{SW} = 2\text{MHz}$

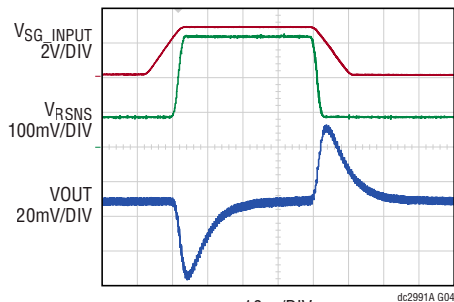
dc2991A G02



DC2991A DEMO BOARD  
(WITH EMI FILTER INSTALLED)  
3.3V INPUT TO 1.2V OUTPUT AT 3.2A,  $f_{SW} = 2\text{MHz}$

dc2991A G03

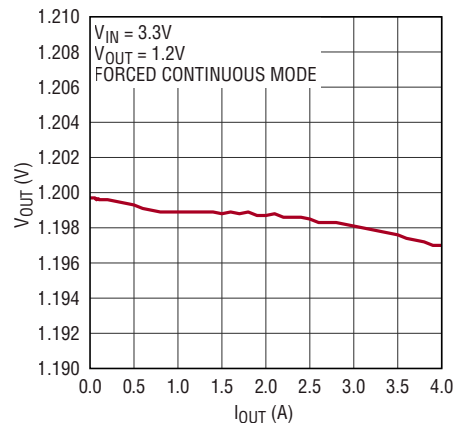
### Load Transient Response Forced Continuous Mode



3.3V<sub>IN</sub> TO 1.2V<sub>OUT</sub>  
LOAD STEP 0.8A TO 3.2A 1A/µs

dc2991A G04

### LTC3308A Load Regulation



dc2991A G05

## QUICK START PROCEDURE

Demonstration circuit 2991A is easy to set up and use to evaluate the performance of the LTC3308A. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

**NOTE:** For accurate  $V_{IN}$ ,  $V_{OUT}$  and efficiency measurements, measure  $V_{IN}$  at the  $V_{IN}$  SNSE and GND SNSE turrets and  $V_{OUT}$  at the  $V_{OUT}$  SNSE and GND SNSE turrets as illustrated as VM1 and VM2 in Figure 1. When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe.

1. Set the JP1 jumper to the SKIP position and JP2 to the HI position.
2. With power off, connect the input power supply to  $V_{IN}$  and GND. If the input EMI filter is desired, connect the input power supply to  $V_{IN}$ .
3. Slowly increase PS1 to 1.0V. If AM1 reads less than 20mA, increase PS1 to 3.3V. Verify that VM1 reads 3.3V and VM2 reads 1.2V.
4. Connect an oscilloscope voltage probe as shown in Figure 2 in parallel with VM2. Set channel to AC coupled, voltage scale to 20mV and time base to 10 $\mu$ s. Observe the  $V_{OUT}$  ripple voltage.  
**NOTE:** Measure the output voltage ripple by touching the probe tip directly across the output turrets or to TP1 as shown in . TP1 is designed for a 50 $\Omega$  coax cable to reduce any high frequency noise that might couple into the oscilloscope probes.
5. Verify that PGOOD turret is high.
6. Increasing the load by 1A intervals up to 4A and record VM1, VM2, AM1 and AM2 for each interval.
7. Repeat Step 6 for PS1 set to 2.5V and again for PS1 set to 5.0V.
8. Set the load to a constant 2A. Remove the oscilloscope voltage probe from  $V_{OUT}$ . Place a ground clip on PGND terminal and set the voltage scale to 1V and the time scale to 500ns/Division. Trigger on the rising edge of the voltage probe. Using a tip on the voltage probe, contact the SW node on the pad of L1. Observe the duty cycle and the period of the switching waveform (~500ns).

9. Set the load current to 0.3A and repeat Step 8. Observe that the switching waveform is now operating in pulse-skipping mode.
10. Move the jumper on JP2 to LO. Verify that  $V_{OUT}$  reads 0V and verify that PGOOD is low. Return jumper on JP2 to HI and verify VM2 is 1.2V and verify PGOOD2 is high.
11. If forced continuous or Burst Mode operation is desired, set PS1 to 0V. Move JP1 to FC/SYNC or BURST. Repeat Steps 3 through 9. In Step 9 observe that the switching waveform is now operating in forced continuous or Burst Mode operation.
12. To change the frequency, remove R9 if installed. Install the desired  $R_T$  resistor in the R4 location. Size the inductor and output capacitors to provide the desired inductor ripple and a stable output. Refer to the LTC3308A data sheet and [LTpowerCAD](#) for more information on choosing the required components.
13. To test the transient response with a base load, add the desired resistor to produce a minimum load between  $V_{OUT}$  and RSNS turrets ( $R_L$  shown on Figure 1). Note that the total load resistance will be  $R_L$  plus R11 (100m $\Omega$ ).
14. Adjust a signal generator with a 10ms period, 10% duty cycle and an amplitude from 1V to 2V to start.
15. Measure the RSNS voltage to observe the current, RSNS/100m $\Omega$ . Adjust the amplitude of the pulse to provide the desired transient. Adjust the rising and falling edge of the pulse to provide the desired ramp rate. Refer to the following equations and the optional transient response circuit.  
$$I_{OUT} = V_{RSNS}/100m\Omega$$
Where:  
$$V_{SG\_INPUT} = V_{SG\_INPUT} - V_{GS}$$
16. When done, turn off PS1 and load. Remove all connections to the demo board.

**QUICK START PROCEDURE**

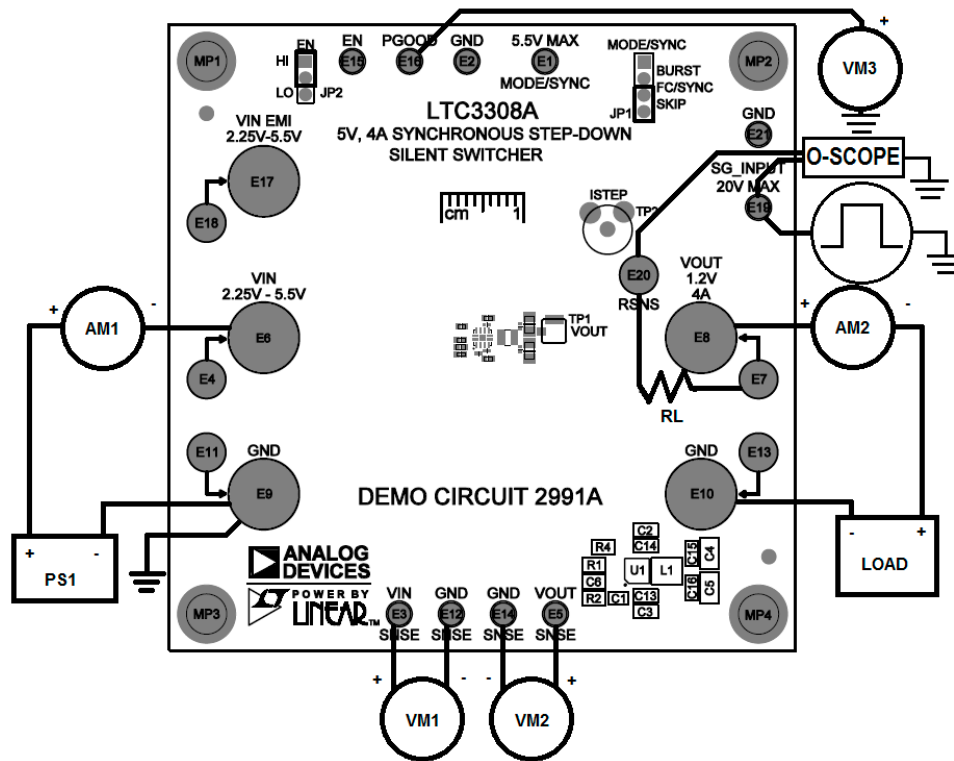


Figure 1. Test Setup for the DC2991A Demo Board

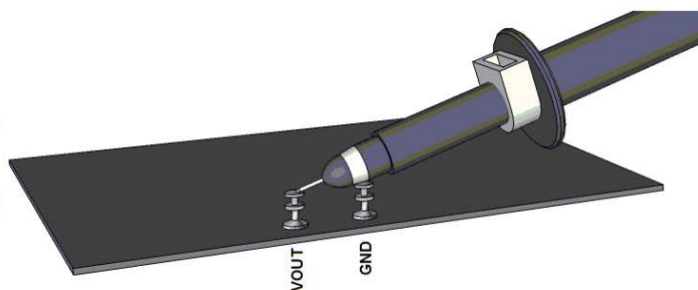


Figure 2. Technique for Measuring Output Ripple and Step Response with a Scope Probe

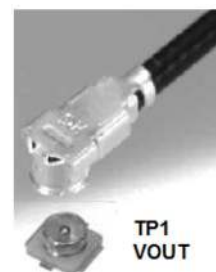


Figure 3. Technique for Measuring Output Ripple and Step Response with a Low Inductance Connector (Not Supplied)

## QUICK START PROCEDURE

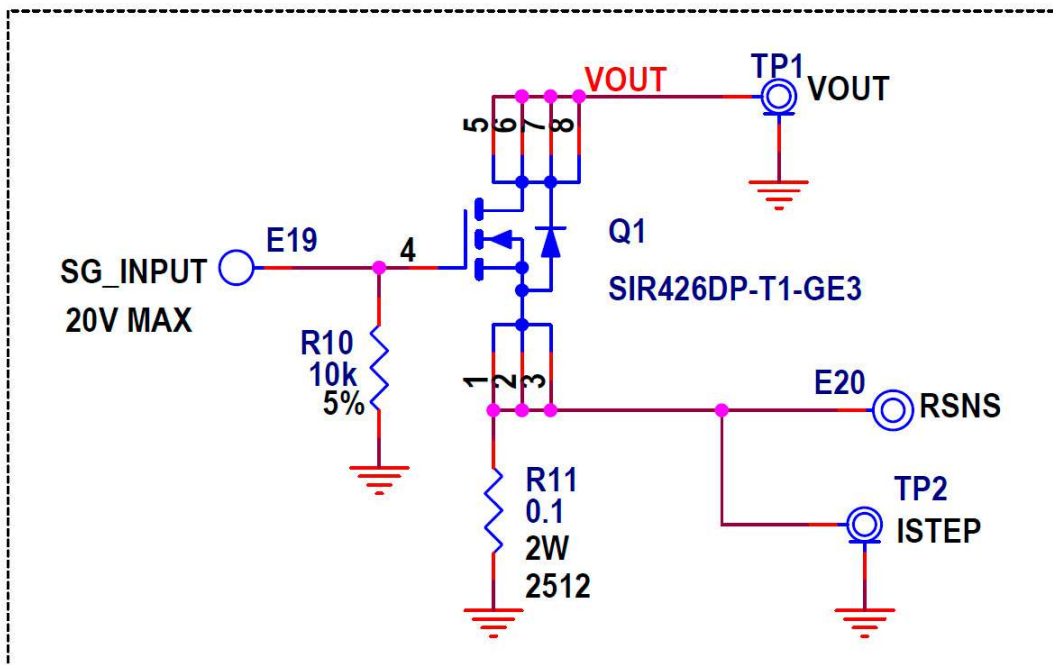


Figure 4. Optional Transient Response Circuit

## THEORY OF OPERATION

### Introduction to the DC2991A

The DC2991A features the LTC3308A, a low voltage synchronous step-down Silent Switcher. The LTC3308A is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch comparator trips and turns off the top power switch. If the EN pin is low, the LTC3308A is in shutdown and in a low quiescent current state. When the EN pin is above its threshold, the switching regulator will be enabled.

The MODE/SYNC pin sets the switching mode to pulse-skipping, forced continuous, or Burst Mode operation. If an external 1MHz to 3MHz clock is connected to the MODE/SYNC turret while the JP1 is set to the FC/SYNC position, the LTC3308A switching frequency will sync to

the external clock while operating in forced continuous mode. See the LTC3308A data sheet for more detailed information.

The maximum allowable operating frequency is influenced by the minimum on-time of the top switch and the ratio of  $V_{OUT}$  to  $V_{IN}$ . The maximum allowable operating frequency may be calculated using a minimum  $T_{ON}$  of 42ns in Equation 1.

$$f_{SWMAX} = \frac{V_{OUT}}{V_{INMAX} \cdot T_{ONMIN}} \quad (1)$$

Select an operating switching frequency below  $f_{SWMAX}$ . The recommended ripple current in the output inductor is 1.2A peak-to-peak for the LTC3308A. This determines the recommended inductor value for the inductor.

## THEORY OF OPERATION

### Accurately Measuring Output Ripple of the LTC3308A

With the fast edge rates of the circuit, high frequency noise can be observed when measuring the output voltage with 1MΩ terminated oscilloscope probes. To better view the output ripple with oscilloscopes of 400MHz bandwidth and above a 50Ω coax cable connected as close to the output capacitor as possible should be used with the oscilloscope channel terminated to 50Ω at the scope. This will help to reduce the noise coupling onto and displaying on the scope. The demo board is set up to solder an U.FL,RECEPT,ST SMD, 0Hz to 6GHz 50Ω connector (TP1) near the output capacitor C4. These pads can also be used to solder a coax cable or other oscilloscope probe connector if desired.

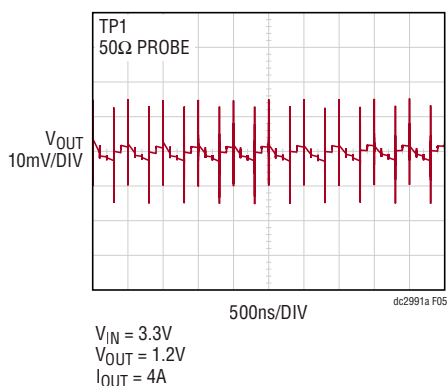


Figure 5.

The high frequency spikes are partially attributed to the interwinding capacitance of the inductor and the voltage step is partially attributed to the inductance in the output capacitors. This can be reduced by choosing low ESL capacitors or adding small low ESL capacitors in parallel

to the output capacitors as close to the inductor as possible. Adding capacitors close to the load creating a π filter between the output caps, trace inductance, and load decoupling capacitors will also help to reduce the ripple. Figure 6 shows the output ripple using a 500MHz scope, 50Ω probe with C4 and C5 reduced to 22μF 0603 capacitors. The capacitors near the V<sub>OUT</sub> turret on the bottom of the board were also populated with C17 = 1μF 0402, plus C18 and C19 = 10μF 0603 capacitors. The output ripple was measured at TP3 on the bottom of the board near the V<sub>OUT</sub> turrets.

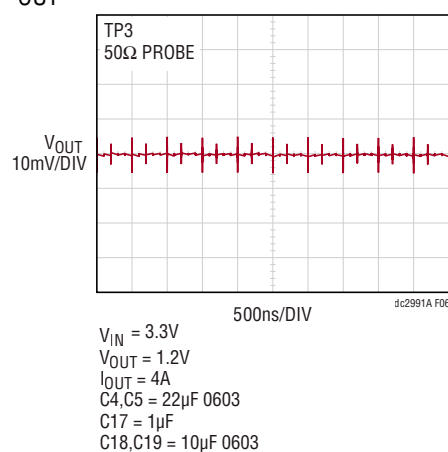


Figure 6.

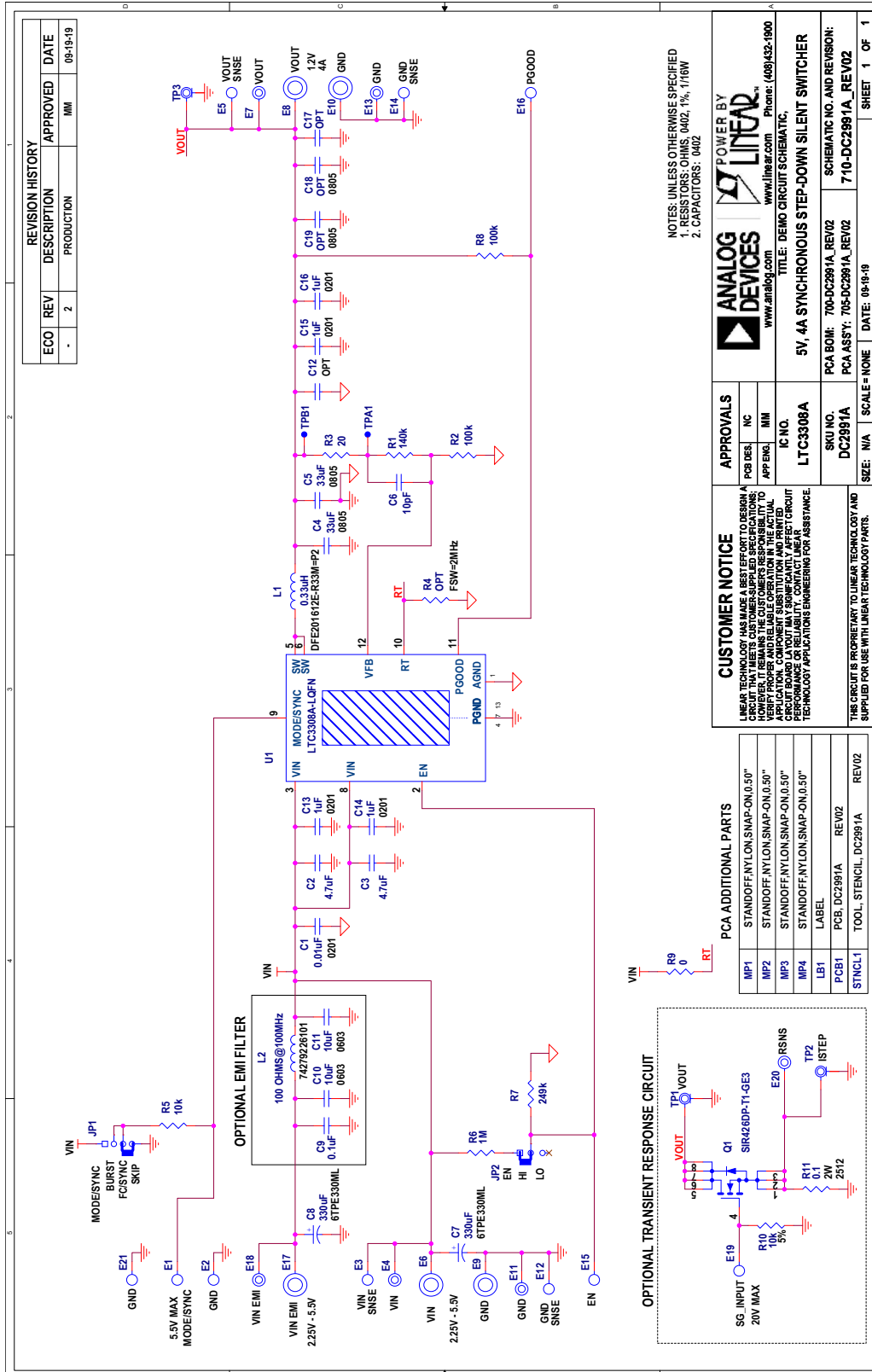
# DEMO MANUAL DC2991A

## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
<b>Required Circuit Components</b>				
1	1	C1	CAP., 0.01 $\mu$ F, X7R, 10V, 10%, 0201	MURATA, GRM033R70J103KA01D
2	2	C2, C3	CAP., 4.7 $\mu$ F, X6S, 6.3V, 20%, 0402	MURATA, GRM155C80J475MEAAD
3	2	C4, C5	CAP., 33 $\mu$ F, X5R, 10V, 20%, 0805	TDK, C2012X5R1A336M125AC
4	1	C6	CAP., 10pF, C0G, 50V, 5%, 0402, AEC-Q200	MURATA, GCM1555C1H100JA16D
5	2	C13, C14	CAP., 1 $\mu$ F, X7T, 6.3V, 20%, 0201	MURATA, GRM033D70J105ME01D
6	1	L1	IND., 0.33 $\mu$ H, PWR, FIXED, 20%, 6.3A, 21m $\Omega$ , 0806	MURATA, DFE201612E-R33M=P2
7	1	R1	RES., 140k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402140KFKED
8	1	R2	RES., 100k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402100KFKvED
9	1	U1	IC, 5V, 4A SYNCHRONOUS STEP-DOWN Silent Switcher, LQFN	ANALOG DEVICES, LTC3308AEV#PBF
<b>Additional Demo Board Circuit Components</b>				
1	2	C7, C8	CAP., 330 $\mu$ F, TANT. POSCAP, 6.3V, 20%, 7343, 25m $\Omega$ , TPE	PANASONIC, 6TPE330ML
2	1	C9	CAP., 0.1 $\mu$ F, X7R, 16V, 10%, 0402, AEC-Q200	MURATA, GCM155R71C104KA55D
3	2	C10, C11	CAP., 10 $\mu$ F, X7S, 6.3V, 20%, 0603	TDK, C1608X7S0J106M080AC
4	2	C15, C16	CAP., 1 $\mu$ F, X7T, 6.3V, 20%, 0201	MURATA, GRM033D70J105ME01D
5	1	L2	IND., 100 $\Omega$ @ 100MHz, FERRITE BEAD, 25%, 8A, 6m $\Omega$ , 1812	WURTH ELEKTRONIK, 74279226101
6	1	Q1	XSTR., MOSFET, N-CH, 40V, 15.9A, PPAK SO-8	VISHAY, SIR426DP-T1-GE3
7	1	R3	RES., 20 $\Omega$ , 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040220R0FKED
8	1	R5	RES., 10k, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040210K0JNED
9	1	R6	RES., 1M $\Omega$ , 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04021M00FKED
10	1	R7	RES., 249k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402249KFKED
11	1	R8	RES., 100k, 5%, 1/16W, 0402	YAGEO, RC0402JR-07100KL
12	1	R9	RES., 0 $\Omega$ , 1/16W, 0402	VISHAY, CRCW04020000Z0ED
13	1	R10	RES., 10k, 5%, 1/10W, 0402, AEC-Q200	PANASONIC, ERJ2GEJ103X
14	1	R11	RES., 0.1 $\Omega$ , 1%, 2W, 2512, SENSE, AEC-Q200	IRC, LRC-LR2512LF-01-R100-F
<b>Hardware: For Demo Board Only</b>				
1	10	E1-E3, E5, E12, E14-E16, E19, E21	TEST POINT, TURRET, 0.064 MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2308-2-00-80-00-00-07-0
2	6	E4, E7, E11, E13, E18, E20	TEST POINT, TURRET, 0.094 MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2501-2-00-80-00-00-07-0
3	5	E6, E8-E10, E17	CONN., BANANA JACK, FEMALE, THT, NON-INSULATED, SWAGE, 0.218"	KEYSTONE, 575-4
4	1	JP1	CONN., HDR, MALE, 1x4, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000411121
5	1	JP2	CONN., HDR, MALE, 1x3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000311121
6	4	MP1-MP4	STANDOFF, NYLON, SNAP-ON, 0.50"	WURTH ELEKTRONIK, 702935000
7	0	TP1, TP3	CONN., U.FL, RECEIPT, ST SMD, 0Hz to 6GHz 50 $\Omega$	HIROSE ELECTRIC, U.FL-R-SMT-1(10)
8	2	XJP1, XJP2	CONN., SHUNT, FEMALE, 2 POS, 2mm	WURTH ELEKTRONIK, 60800213421



## SCHEMATIC DIAGRAM





## ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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