3-to-8 Line Decoder

MC74VHCT138A

The MC74VHCT138A is an advanced high speed CMOS 3–to–8 decoder fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

When the device is enabled, three Binary Select inputs (A0 – A2) determine which one of the outputs ($\overline{Y0} - \overline{Y7}$) will go Low. When enable input E3 is held Low or either $\overline{E2}$ or $\overline{E1}$ is held High, decoding function is inhibited and all outputs go high. E3, $\overline{E2}$, and $\overline{E1}$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

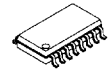
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because they have full 5V CMOS level output swings.

The VHCT138A input structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 7.6ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 122 FETs or 30.5 Equivalent Gates

D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01

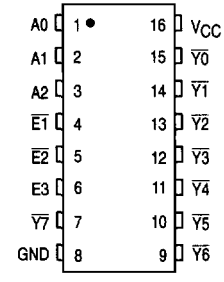


M SUFFIX
16–LEAD SOIC EIAJ PACKAGE
CASE 966–01

ORDERING INFORMATION

MC74VHCTXXXAD	SOIC
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

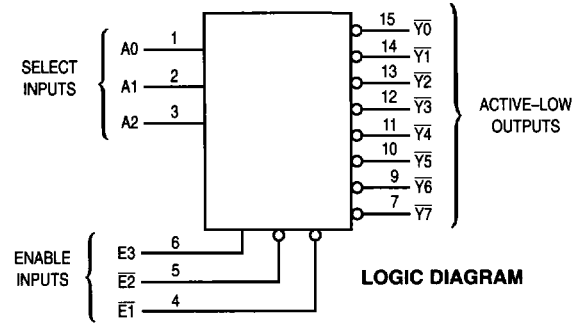
PIN ASSIGNMENT



FUNCTION TABLE

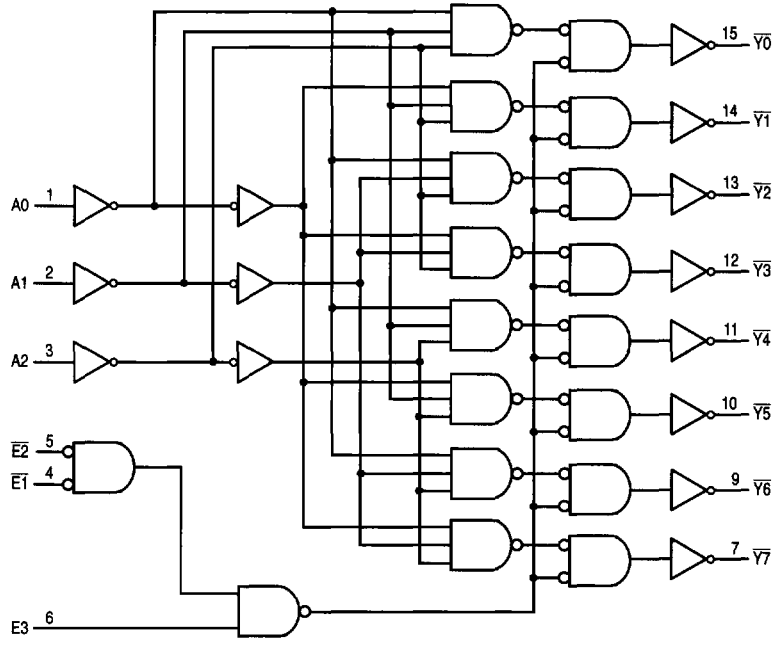
Inputs						Outputs							
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level (steady state); L = low level (steady state); X = don't care



LOGIC DIAGRAM

EXPANDED LOGIC DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		– 0.5 to + 7.0	V
V_{in}	DC Input Voltage		– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	V_{CC} = 0 High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})		± 20	mA
I_{out}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
P_D	Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature		– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage	V_{CC} = 0 High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50μA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		20.0	μA
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		7.6	10.4	1.0	12.0	ns
		$C_L = 50pF$		8.1	11.4	1.0	13.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, E3 to Y	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		6.6	9.1	1.0	10.5	ns
		$C_L = 50pF$		7.1	10.1	1.0	11.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{E2}$ or $\overline{E1}$ to Y	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		7.0	9.6	1.0	11.0	ns
		$C_L = 50pF$		7.5	10.6	1.0	12.0	
C_{in}	Maximum Input Capacitance			4	10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 1.)	49	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

SWITCHING WAVEFORMS

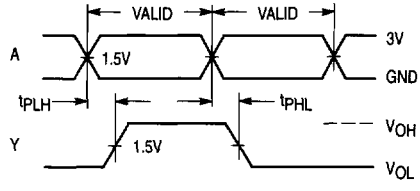


Figure 1.

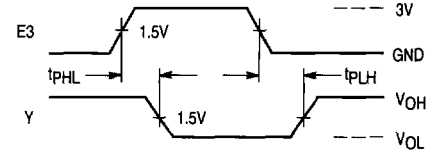


Figure 2.

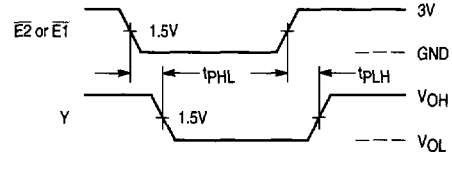
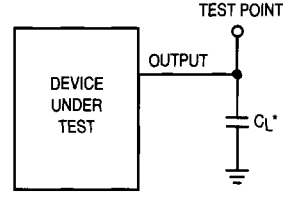


Figure 3.

TEST CIRCUIT



* Includes all probe and jig capacitance

Figure 4. Test Circuit