DATA SHEET

SKY73208-11: 350-5000 MHz Wideband Receive Mixer with Integrated Integer-N PLL and VCO

DISCONTINUED

Applications

- Cellular base station systems: GSM/EDGE, CDMA2000, WCDMA, TD-SCDMA
- Other wireless communication systems

Features

- RF frequency range: 350 to 5000 MHz
- IF frequency range: 50 to 500 MHz
- Conversion gain: 6 dB
- IIP3: +26 dBm; OIP3: +32 dBm
- Noise figure: 14 dB
- Integrated RF balun
- Integer-N frequency synthesizer
- Low phase-noise VCO
- Low RF output comparison spurs
- Programmable 18-bit N-counter and 11-bit R-counter
- Wide range of reference frequencies
- Programmable charge pump currents
- Flexible configuration that allows connection to an external VCO or PLL
- Digital lock detector
- Power supply for mixer: 5 V; power supply for synthesizer: 3.3 V
- Small, low-cost MCM (36-pin, 6 x 6 mm) SMT package (MSL3, 260 °C per JEDEC J-STD-020)

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Description

The Skyworks SKY73208-11 is a fully integrated wideband receive downconverter that includes a high-linearity mixer and a complete voltage-controlled oscillator (VCO), synthesizer, and local oscillator (LO) chain. A low-loss RF balun has also been included to reduce design complications and to lower system cost.

The SKY73208-11 features a third order input intercept point (IIP3) of +26 dBm and a noise figure (NF) of 14 dB, which make the device an ideal solution for high dynamic range systems such as 2G/3G base station receivers.

The SKY73208-11 also includes a fully integrated wideband VCO/Integer-N frequency synthesizer. The device includes four differential VCOs that cover the output frequency range from 2.8 GHz to 6.0 GHz. By applying internal VCO division, the output LO frequency can be set to the desired value while minimizing the phase noise. The direct, non-divided internal VCO frequency can also be monitored at the bidirectional VCO pins.

The flexible SKY73208-11 LO configuration allows the loop to be locked by an external VCO or external phase locked loop (PLL), or the device can use the divider chain only. The SKY73208-11 is controlled by a serial peripheral interface (SPI).

The SKY73208-11 is manufactured using a robust silicon BiCMOS process and has been designed for optimum long-term reliability. It is manufactured in a compact, 36-pin 6 x 6 mm Multi-Chip Module (MCM). A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

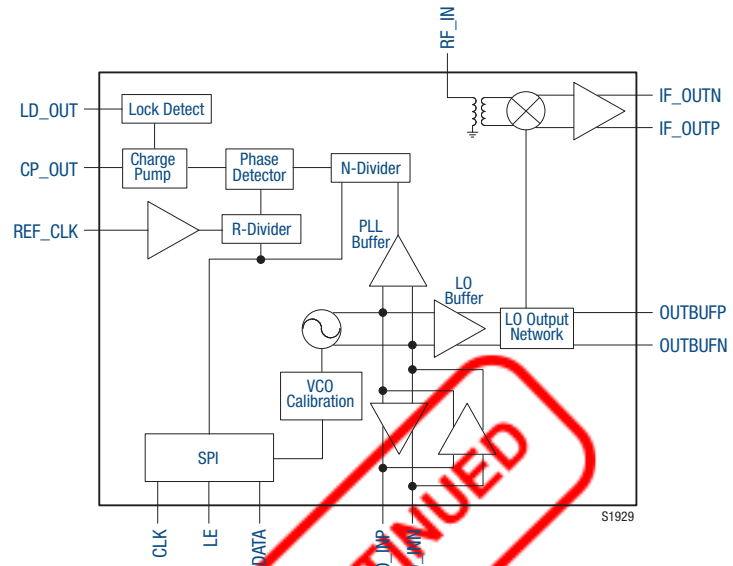


Figure 1. SKY73208-11 Block Diagram

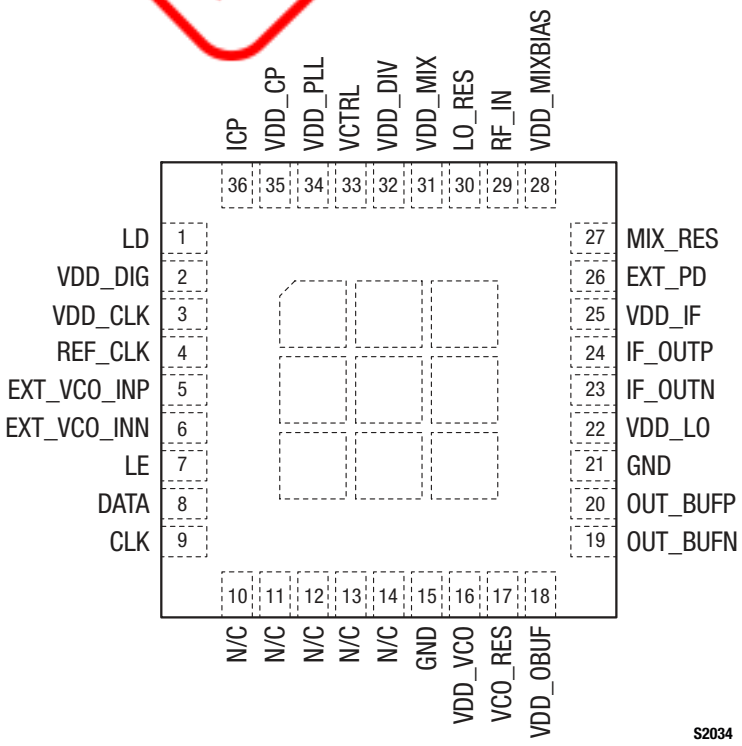


Figure 2. SKY73208-11 Pinout
(Top View)

Table 1. SKY73208-11 Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	LD	Lock detect output	19	OUT_BUFN	LO negative output
2	VDD_DIG	+3.3 V supply for digital blocks	20	OUT_BUFP	LO positive output
3	VDD_CLK	+3.3 V supply for reference buffer	21	GND	Ground
4	REF_CLK	Reference clock input	22	VDD_LO	+5 V supply for mixer LO buffer
5	EXT_VCO_INP	External VCO positive input	23	IF_OUTN	Negative IF output
6	EXT_VCO_INN	External VCO negative input	24	IF_OUTP	Positive IF output
7	LE	Latch enable input for SPI	25	VDD_IF	+5 V supply for mixer output
8	DATA	Data input for SPI	26	EXT_PD	Power-down control pin for mixer
9	CLK	Clock input for SPI	27	MIX_RES	External bias resistor for mixer
10	N/C	No connection	28	VDD_MIXBIAS	+5 V supply for mixer bias
11	N/C	No connection	29	RF_IN	RF mixer input
12	N/C	No connection	30	LO_RES	External bias resistor for LO chain
13	N/C	No connection	31	VDD_MIX	+5 V supply for mixer
14	N/C	No connection	32	VDD_DIV	+3.3 V supply for LO dividers
15	GND	Ground	33	VCTRL	Tuning voltage for VCO
16	VDD_VCO	+3.3 V supply for VCO	34	VDD_PLL	+3.3 V supply for PLL
17	VCO_RES	External 15 kΩ resistor to set VCO bias	35	VDD_CP	+3.3 V supply for charge pump
18	VDD_OBUF	+3.3 V supply for output LO buffer	36	ICP	Charge pump output

Functional Description

The SKY73208-11 is comprised of four main functional blocks:

- RF mixer
- Synthesizer
- VCO
- VCO dividers and LO chain

RF Mixer

The high linearity SKY73208-11 integrates an active, double balanced mixer that provides good noise performance and an excellent third order input intercept point (IIP3).

The balanced nature of the mixer also provides for high port-to-port isolation. A wideband match to 50 Ω is provided internally, which eliminates the need for any external matching components except for a coupling capacitor.

The IF outputs are designed for a 200 Ω differential impedance and require off-chip matching.

Synthesizer

The frequency synthesizer is composed of the R-divider, N-divider, phase detector, charge pump, and lock detector.

R-Divider

The 11-bit programmable R-divider divides the reference input frequency and generates the reference input for the phase detector. The R-divider range varies from 1 to 2^{11} –1 (= 2047).

N-Divider

The N-divider consists of a selectable 16/17 or 32/33 prescaler, 13-bit main counter, and 5-bit swallow counter. The 18-bit N-divider ratio is calculated as:

$$N = P \times M + S$$

Where: P = Prescaler value
M = Main counter value
S = Swallow counter value

The N-divider range is from P^2 to 2^{18} – 1. For a 32/33 prescaler, the N-divider range varies from 1024 to 262143.

Phase Detector

The phase detector is an edge-controlled digital circuit. The circuit has two inputs: the reference signal (*Ref*) and the N-divider output. There are two digital outputs (*Up* and *Dn*) that drive the charge pump.

When the input phase difference is positive, the *Up* output is pulled up to VDD. When the input phase difference is negative, the *Dn* output is pulled down to ground. This type of phase detector acts only on the positive edges of the input signals.

Charge Pump

The charge pump is used to convert the logic levels of the *Up* and *Dn* pulses, carrying the phase error between the reference and the divided signal into analog quantities/current pulses.

The output of the SKY73208-11 charge pump is programmable and varies between 1.2 mA and 7.2 mA. Additional adjustment of the charge pump current can be accomplished by changing the value of the external PLL bias resistor.

Lock Detector

The lock detector circuit is activated when the phase difference between the *Up* and *Dn* phase detector signals for a given number of comparison cycles is shorter than a fixed delay. The CMOS output is active high when the loop is locked. The lock detector can be monitored from pin 1 (LD).

VCO

The VCO is designed to generate the LO signal with the tuning function controlled by the synthesizer.

VCO Dividers and LO Chain

The divider chain consists of dividers and LO drivers.

The direct, non-divided VCO output can be monitored at the bi-directional internal/external VCO pins 5 and 6 (EXT_VCO_INP and EXT_VCO_INN, respectively). The divider chain and the internal PLL can be locked by an external VCO.

External LO

The SKY73208-11 can accept an external LO signal and disable the internal synthesizer. The high impedance differential injection port is at pins 5 and 6 (EXT_VCO_INP and EXT_VCO_INN, respectively).

If single-ended input is required, one of the pins can be grounded or an external balun can be used. The register settings to enable this mode of operation are detailed in the Skyworks document, *Wideband, Integer-N Phase-Locked Loop Programming Guide*, document #201322.

LO Output

It is possible to monitor the LO signal (either the internally generated LO or an externally applied LO) or route the signal to another device that requires the same LO frequency. The differential LO output is available at pins 19 and 20 (OUTBUFN and OUTBUFP, respectively) using external coupling capacitors.

If single-ended output is desired, use pin 19 or an external balun. This feature does not require any specific register bit setting and these pins can be left floating if not used.

Digital Interface

A three-wire SPI provides mode and bias control, and control of the PLL. The serial interface consists of three signals: the bus clock (CLK), latch enable (LE), and the serial data line (DATA).

A write data stream consists of 25 bits:

Bits[15:0] provide the 16-bit data block.

Bits[20:16] provide the register address.

Bits[24:21] provide the device address (the SKY73208-11 is 0110b).

A timing diagram for the SPI write cycle is shown in Figure 3.

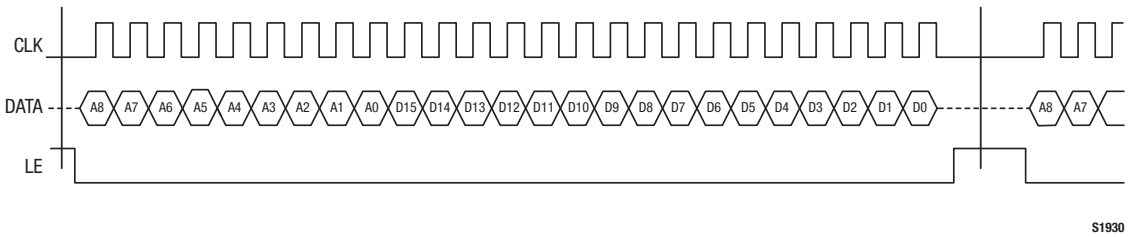


Figure 3. SPI Write Cycles

Table 2. SPI Timing Requirements

Timing	Description	Minimum Time (ns)
t_{period}	Clock period	25
t_{high}	Clock high time	10
t_{su}	Data setup to clock rise	5
t_{hld}	Data hold from clock rise	5
t_{elch}	Enable low to clock rise	10
t_{width}	Enable high width	10
t_{efeh}	Clock fall to enable high	20

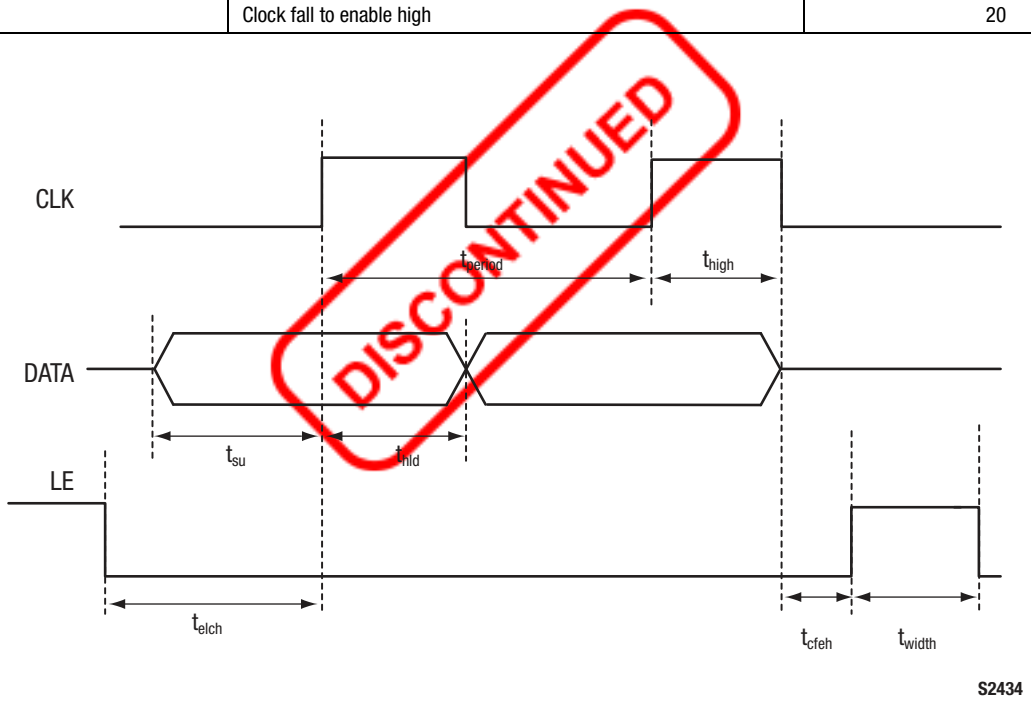


Figure 4. SPI Input Timing Diagram

Serial Bus Timing

The SPI bus speed is programmable. Timing requirements for the CLK, DATA, and LE signals are provided in Table 2. A serial data input timing diagram is shown in Figure 4.

PLL Control Registers (R-Divider and N-Divider)

There are three digital PLL control registers that are used to store the R-divider and N-divider values: R_DIV, N_DIV1, and N_DIV2. By default, all registers are 25 bits wide. Bits[20:16] are the address bits of the registers. The 16 least significant bits (LSBs) represent the data bits.

Three values are needed to calculate the three PLL dividers: the desired frequency (F_{RF}), the VCO divider (D), and the frequency step size (F_{STEP}).

The VCO frequency (F_{VCO}) has a range of 2.8 GHz to 6.0 GHz, and is defined by the product of the desired frequency (F_{RF}) and the VCO divider, D:

$$F_{VCO} = F_{RF} \times D \quad (1)$$

The VCO divider (equal to 1, 2, 4, or 8) is chosen so that the product of $F_{RF} \times D$ is within the specified VCO range.

The frequency step size (F_{STEP}) is a user-defined value. Given F_{STEP} and D, the comparison frequency (F_{COMP}) can be calculated by:

$$F_{COMP} = F_{STEP} \times D \quad (2)$$

The R_DIV register stores the value of the 11-bit R-divider that produces the desired comparison frequency (*FCOMP*) for the RF PLL according to the following equation:

$$R = \frac{F_{REF}}{F_{COMP}} \quad (3)$$

Where *FREF* is the reference frequency provided to the device.

The N_DIV1 and N_DIV2 registers store the value of the N-divider according to the following equation:

$$N = \frac{F_{VCO}}{F_{REF}} \times R \quad (4)$$

Bits[1:0] of the N_DIV2 register are the most significant bits (MSBs) of the 18-bit representation of the N number.

Bits[15:0] of the N_DIV1 register are the LSBs of the 18-bit binary representation of the N number.

The calculated R-divider and N-divider values are programmed into the SKY73208-11 using the SPI interface.

Additional programming information is provided in the document, *Skyworks Wideband, Integer-N Phase-Locked Loop Programming Guide*, document number 201322.

Example:

A desired RF output frequency of 1800 MHz is required using a reference frequency of 76.8 MHz and a desired frequency step size of 400 kHz. If the VCO divider is equal to 2, the VCO frequency is 3600 MHz from Equation 1 and the comparison frequency is equal to 800 kHz from Equation 2.

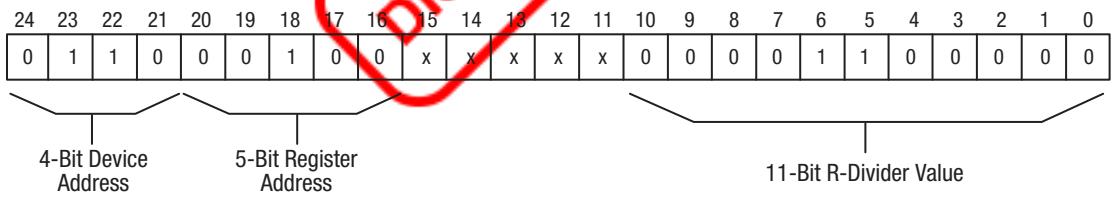
From Equations 3 and 4, the R and N values become:

R = 96 = 1100000b

N = 4500 = 1000110010100b

These values would be programmed through the SPI interface.

Figure 5 represents the bits of the R_DIV register with the value of R = 96. Figures 6 and 7 represent the bits of the N_DIV1 and N_DIV2 registers, respectively, with the value of N = 4500.



Note: Value of bits [15:11] can vary. Refer to the *Skyworks Wideband, Integer-N Phase-Locked Loop* Programming Guide, document number 201322.

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Figure 5. R_DIV Register Showing an R-Divider Value of 96

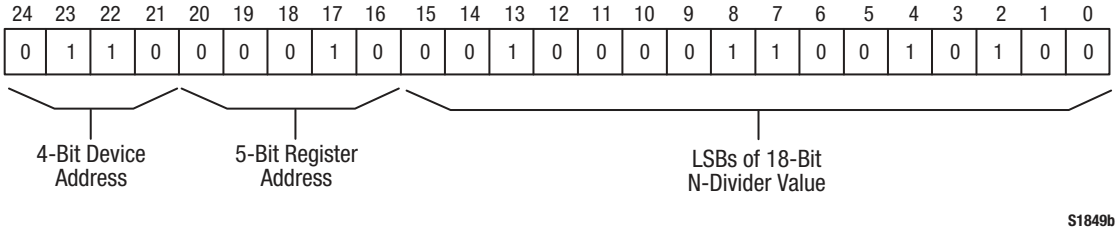

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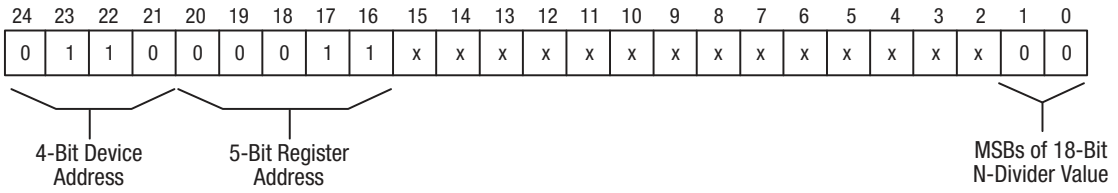
Figure 6. N_DIV1 Register Showing an N-Divider Value of 4500 (LSBs)



Note: Value of bits [15:2] can vary. Refer to the *Skyworks Wideband, Integer-N Phase-Locked Loop* Programming Guide, document number 201322. **S1848b**

Figure 7. N_DIV2 Register Showing an N-Divider Value of 4500 (MSBs)

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY73208-11 are provided in Table 3. The recommended operating conditions are specified in Table 4 and electrical specifications are provided in Table 5.

Table 3. SKY73208-11 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Mixer supply voltage (VDD_LO, VDD_IF, VDD_MIXBIAS, and VDD_MIX = +5 V)	V_{DD_MIX}			5.5	V
Synthesizer supply voltage (VDD_VCO, VDD_OBUF, VDD_PLL, VDD_CLK, VDD_DIV, VDD_CP, and VDD_DIG = +3.3 V)	V_{DD_SYNTH}			3.6	V
Mixer supply current (VDD_LO, VDD_IF, VDD_MIXBIAS, and VDD_MIX = +5 V)	I_{DD_MIX}			200	mA
Synthesizer supply current (VDD_VCO, VDD_OBUF, VDD_PLL, VDD_CLK, VDD_DIV, VDD_CP, and VDD_DIG = +3.3 V)	I_{DD_SYNTH}			150	mA
RF input power	P_{IN}			+10	dBm
Operating case temperature	T_C	–40		+85	°C
Junction temperature	T_J			+150	°C
Storage case temperature	T_{STG}	–40		+125	°C

Notes: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 4. SKY73208-11 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Mixer supply voltage (VDD_LO, VDD_IF, VDD_MIXBIAS, and VDD_MIX pins)	V_{DD_MIX}	4.75	5.00	5.25	V
Synthesizer supply voltage (VDD_VCO, VDD_OBUF, VDD_PLL, VDD_CLK, VDD_DIV, VDD_CP, and VDD_DIG pins)	V_{DD_SYNTH}	3.0	3.3	3.6	V
RF frequency range	f_{RF}	350		5000	MHz
IF frequency range	f_{IF}	50		500	MHz
Mixer supply current (VDD_LO, VDD_IF, VDD_MIXBIAS, and VDD_MIX pins)	I_{DD_MIX}		135		mA
Synthesizer supply current (VDD_VCO, VDD_OBUF, VDD_PLL, VDD_CLK, VDD_DIV, VDD_CP, and VDD_DIG pins)	I_{DD_SYNTH}		120		mA
Operating case temperature	T_C	–40		+85	°C
SPI logic levels (CLK, DATA, LE): Low High	 V_{IL} V_{IH}	 $0.8 \times V_{DD\_3.3V}$		 $0.2 \times V_{DD\_3.3V}$	 V V
External LO input level (Note 1)		500			mVp-p, diff.

Note 1: Input signal level that maintains the mixer performance described in Table 5.

Table 5. SKY73208-11 Electrical Specifications (1 of 2) (Note 1)
(V_{DD_MIX} = +5 V, V_{DD_SYNTH} = +3.3 V, T_C = +25 °C, RF Frequency = 700 to 2700 MHz, IF Frequency = 100 MHz, LO Frequency = 800 to 2800 MHz High-Side Injection or 600 to 2600 MHz Low-Side Injection, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Mixer						
Conversion gain	G	f_{RF} = 915 MHz f_{RF} = 1980 MHz f_{RF} = 2700 MHz	6.0 5.5 4.5	6.5 6.0 5.0		dB dB dB
Gain variation over temperature				±0.5		dB
Noise figure	NF	f_{RF} = 915 MHz f_{RF} = 1980 MHz f_{RF} = 2700 MHz		14.5 14.0 15.5	15.5 15.5 16.0	dB
Third order input intercept point	IIP3	f_{RF} = 915 MHz f_{RF} = 1980 MHz f_{RF} = 2700 MHz	+21.5 +21.5 +20.0	+24.5 +25.5 +23.0		dBm dBm dBm
IIP3 variation over temperature				±1.2		dB
Third order output intercept point	OIP3	f_{RF} = 915 MHz f_{RF} = 1980 MHz f_{RF} = 2700 MHz	+27.0 +26.0 +24.0	+31.0 +31.5 +28.0		dBm dBm dBm
2RF to 2LO	2x2	f_{RF} = 915 MHz f_{RF} = 1980 MHz f_{RF} = 2700 MHz		–66.5 –73.5 –62.0	–50.0 –50.0 –50.0	dBc dBc dBc
3RF to 3LO	3x3	f_{RF} = 915 MHz f_{RF} = 1980 MHz f_{RF} = 2700 MHz		–79.0 –72.5 –72.5	–60.0 –60.0 –60.0	dBc dBc dBc
1 dB input compression point	IP1dB	f_{RF} = 915 MHz f_{RF} = 1980 MHz f_{RF} = 2700 MHz	+4.0 +4.0 +6.0	+5.0 +5.5 +6.5		dBm dBm dBm

Table 5. SKY73208-11 Electrical Specifications (2 of 2) (Note 1)
(V_{DD_MIX} = +5 V, V_{DD_SYNTH} = +3.3 V, T_C = +25 °C, RF Frequency = 700 to 2700 MHz, IF Frequency = 100 MHz, LO Frequency = 800 to 2800 MHz High-Side Injection or 600 to 2600 MHz Low-Side Injection, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Mixer (continued)						
1 dB output compression point	OP1dB	f_{RF} = 915 MHz f_{RF} = 1980 MHz f_{RF} = 2700 MHz	+9.0 +9.0 +9.0	+10.5 +10.5 +10.5		dBm dBm dBm
RF-to-IF isolation (Note 2)		f_{RF} = 1980 MHz			–30	dBc
LO leakage @ RF port		f_{RF} = 915 MHz f_{RF} = 1980 MHz f_{RF} = 2700 MHz			–30 –30 –30	dBm dBm dBm
RF port input return loss	Z_{IN_RF}	No matching: f_{RF} = 915 MHz f_{RF} = 1980 MHz f_{RF} = 2700 MHz		 –19 –14 –13	 –14 –12 –11	 dB dB dB
Synthesizer						
Reference input frequency	f_{REF}		10.0	153.6	200.0	MHz
Reference input sensitivity			0.2	1.5		Vp-p
Charge pump current	I_{CP}		1.2	4.8	7.2	mA
LO output power				–6	–2	dBm
Comparison spurs					–65	dBc
Locking time					1	ms
Phase noise @ 1015 MHz		@ 10 kHz offset @ 100 kHz offset @ 1 MHz offset @ 10 MHz offset		–87 –100 –134 –148	–83 –94 –132 –145	dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Phase noise @ 2080 MHz		@ 10 kHz offset @ 100 kHz offset @ 1 MHz offset @ 10 MHz offset		–86.0 –102.0 –134.0 –150.0	–81.5 –94.0 –131.0 –146.5	dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Phase noise @ 2800 MHz		@ 10 kHz offset @ 100 kHz offset @ 1 MHz offset @ 10 MHz offset		–84.0 –99.5 –131.5 –148.0	–78.0 –90.0 –128.0 –146.0	dBc/Hz dBc/Hz dBc/Hz dBc/Hz
RMS phase error @ 1015 MHz		1 kHz to 10 MHz integrated bandwidth		0.75	1.10	deg
RMS phase error @ 2080 MHz		1 kHz to 10 MHz integrated bandwidth		0.85	1.10	deg
RMS phase error @ 2800 MHz		1 kHz to 10 MHz integrated bandwidth		1.0	1.2	deg

Note 1: Performance is guaranteed only under the conditions listed in this table.

Note 2: Under fully symmetric load conditions.

Evaluation Board Description

The SKY73208-11 Evaluation Board is used to test the performance of the SKY73208-11 module. An Evaluation Board schematic diagram is provided in Figure 8. An assembly drawing for the Evaluation Board is shown in Figure 9 and the layer detail is provided in Figure 10.

Circuit Design Configurations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

- Paths to ground should be made as short as possible.
- The ground pad of the SKY73208-11 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the device. Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board.
- Skyworks recommends including external bypass capacitors on the V_{DD} voltage inputs of the device.

Package Dimensions

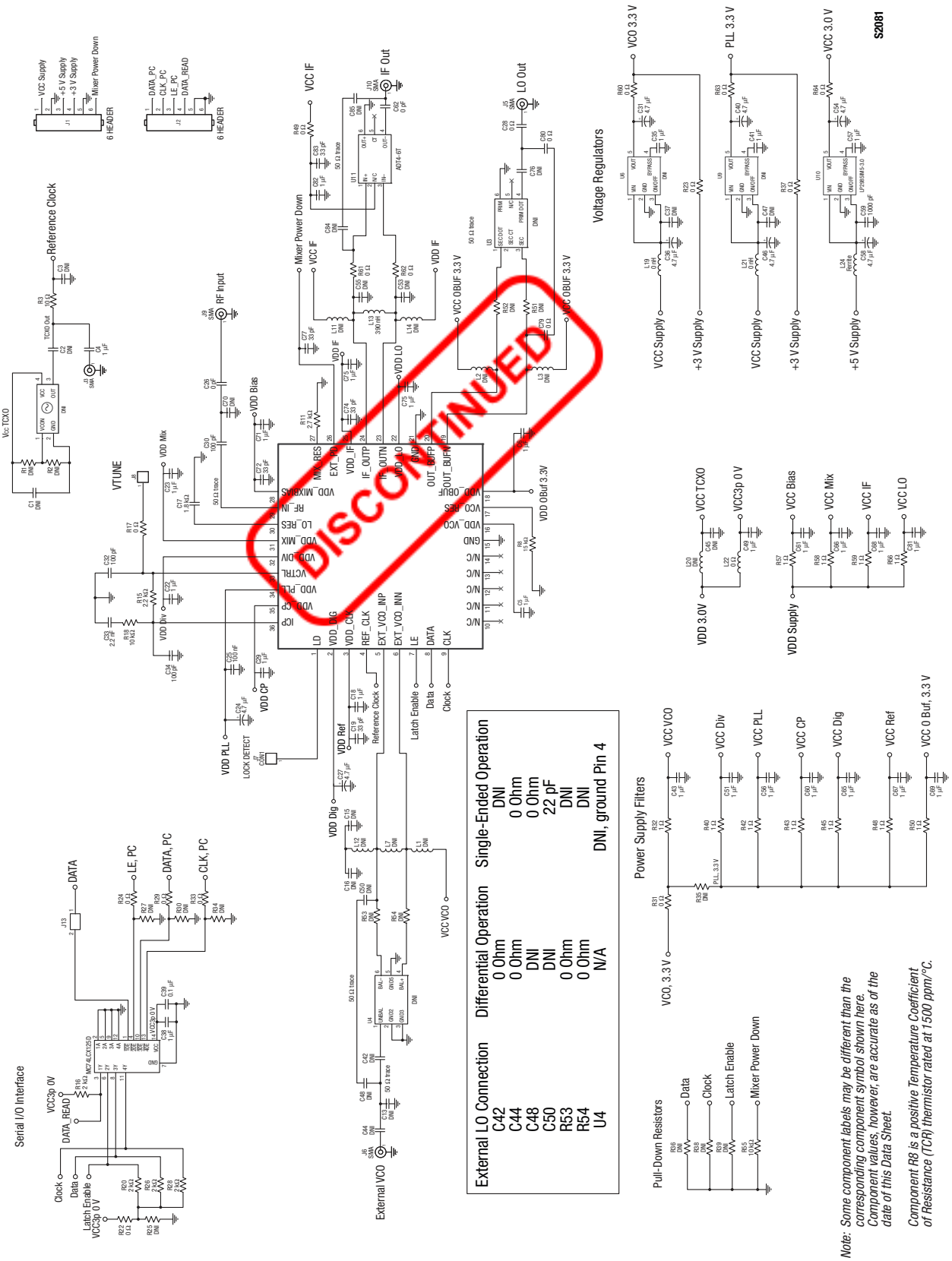
The PCB layout footprint for the SKY73208-11 is provided in Figure 11. Figure 12 shows the package dimensions, and Figure 13 provides the tape and reel dimensions.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY73208-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design & SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



Note: Some component labels may be different than the corresponding component symbol shown here. Component values, however, are accurate as of the date of this Data Sheet.

Component R8 is a positive Temperature Coefficient of Resistance (TCR) thermistor rated at 1500 ppm/°C.

Figure 8. SKY73208-11 Evaluation Board Schematic

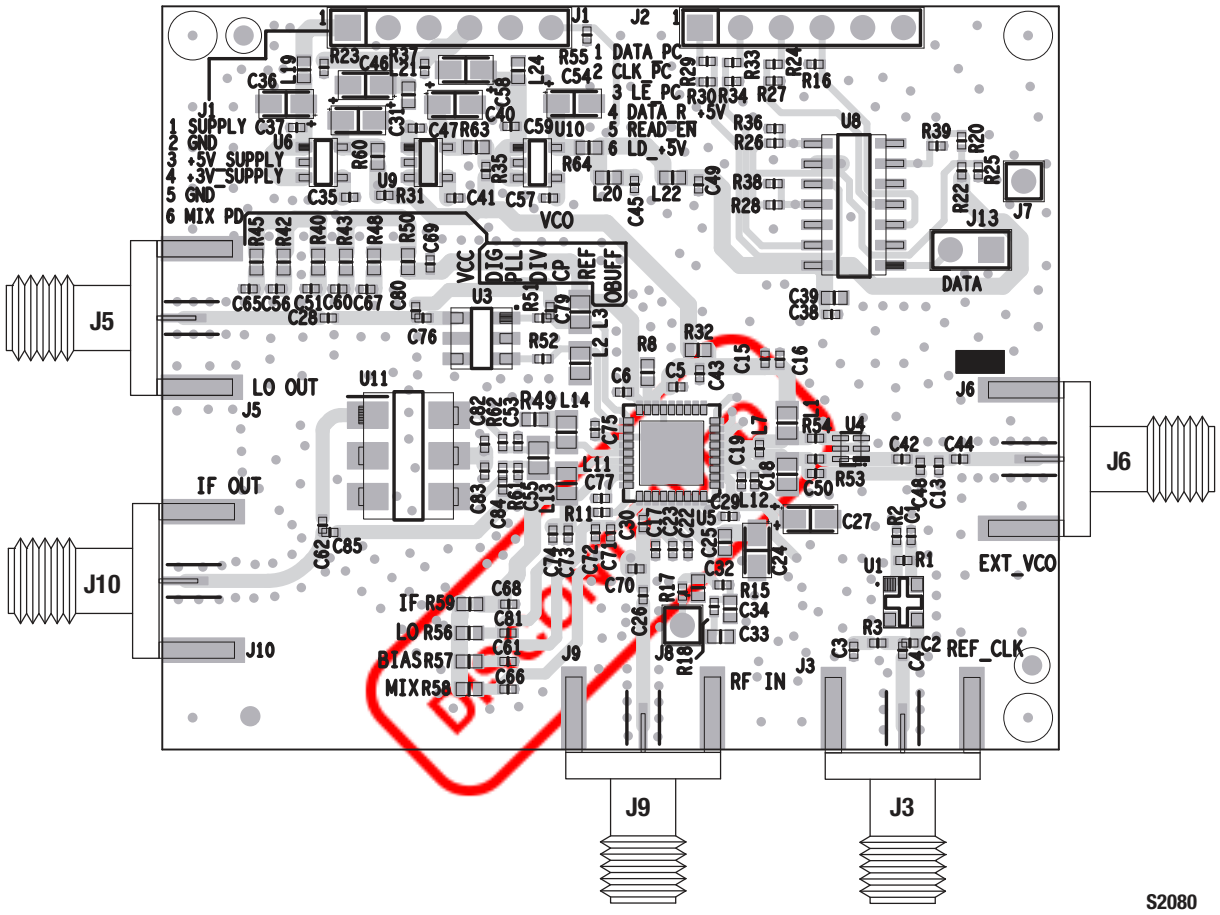


Figure 9. SKY73208-11 Evaluation Board Assembly Drawing

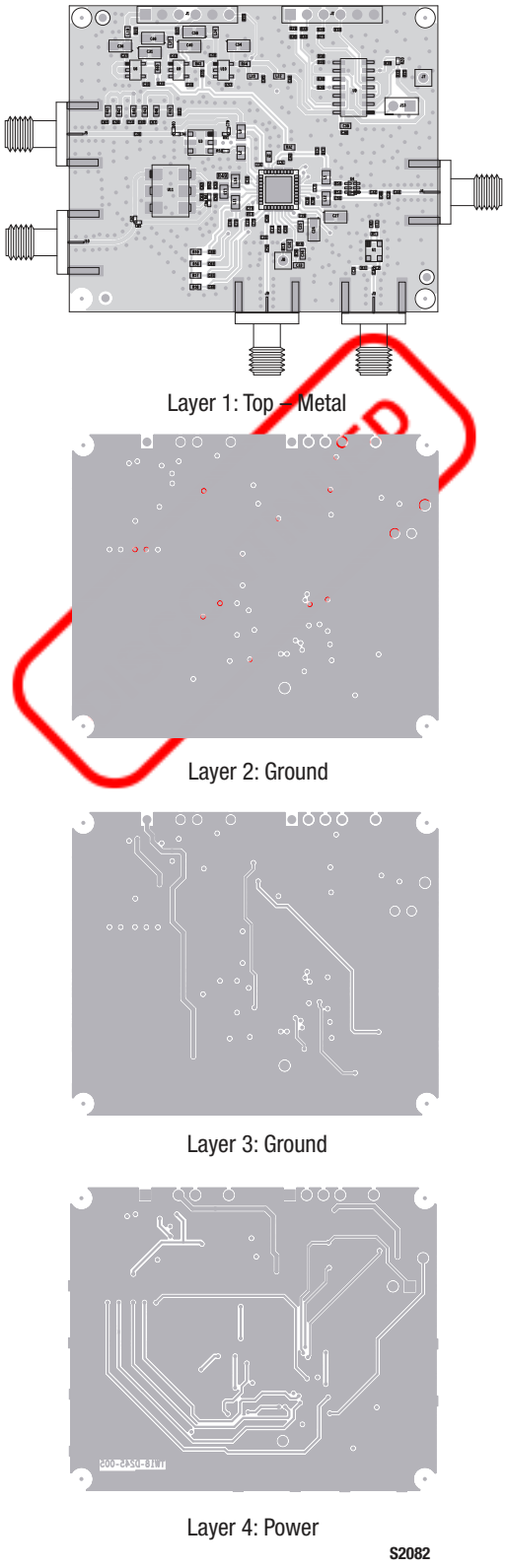
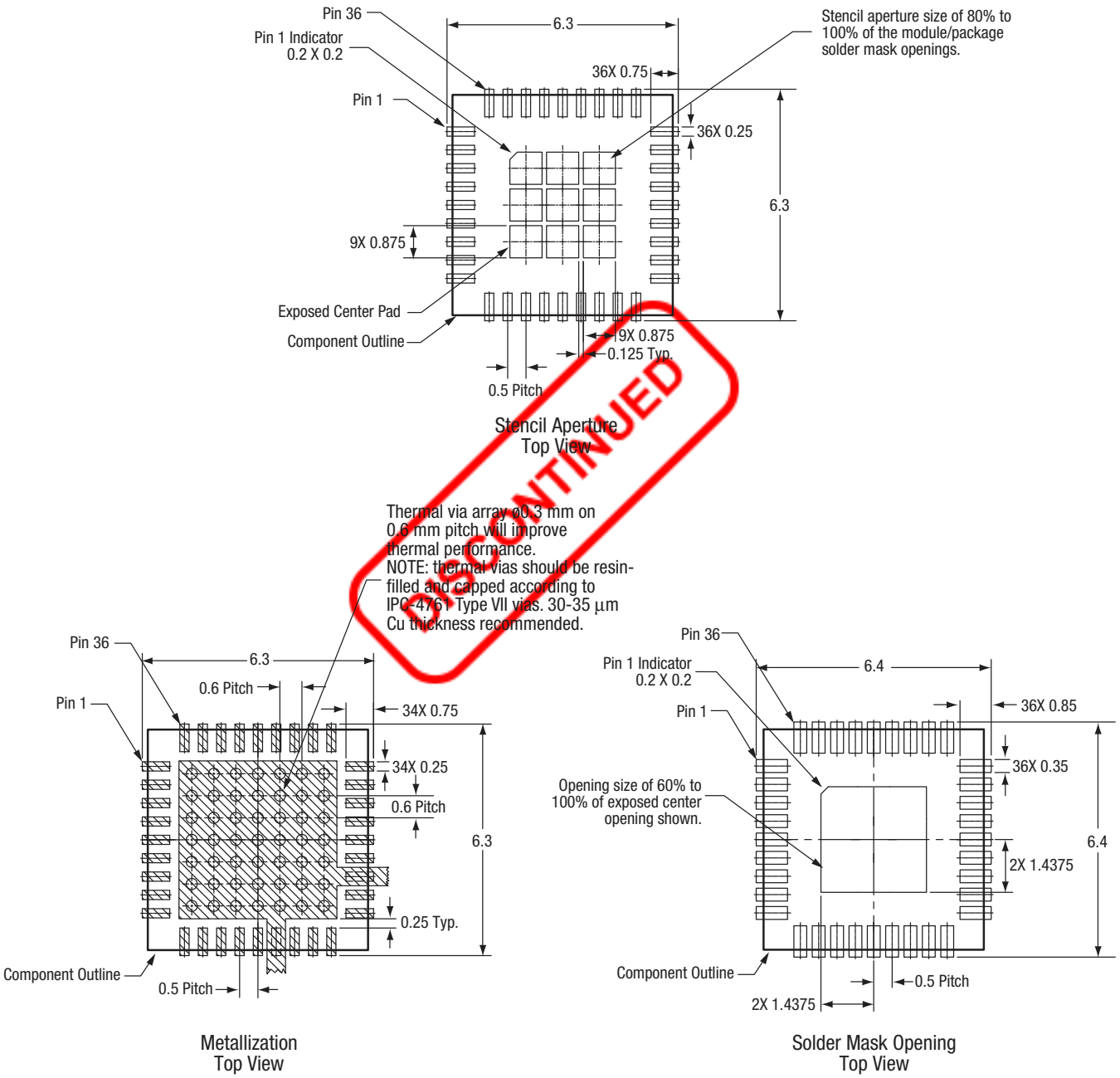


Figure 10. SKY73208-11 Evaluation Board Layer Detail



All measurements are in millimeters

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Figure 11. SKY73208-11 PCB Layout Footprint

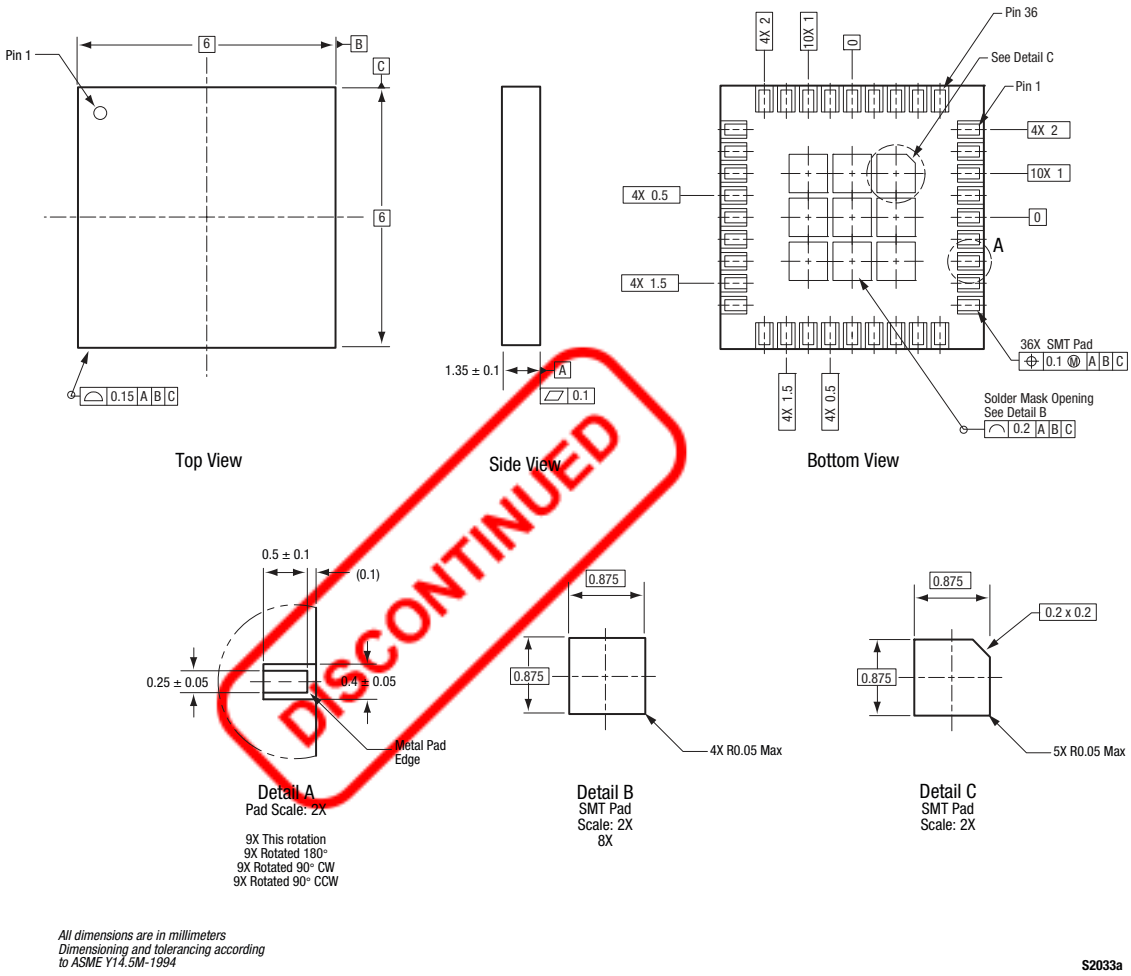
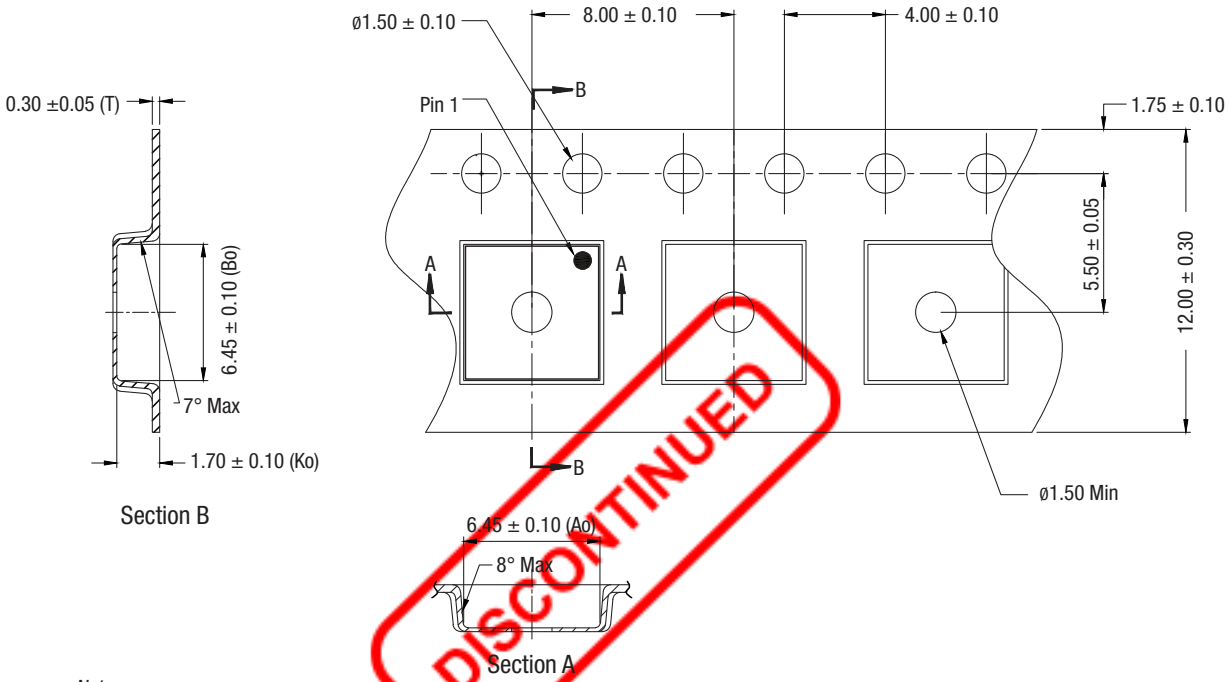


Figure 12. SKY73208-11 Package Dimensions



Notes:

1. *Carrier tape must meet all requirements of Skyworks GP01-D233 procurement spec for tape and reel shipping.*
2. *Carrier tape: black conductive polycarbonate or polystyrene.*
3. *Cover tape material: transparent antistatic polyester film.*
4. *ESD-surface resistivity shall be ≤ 1 x 10^6Ω/square per EIA, JEDEC TNR Specification.*
5. *All dimensions are in millimeters.*

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Figure 13. SKY73208-11 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY73208-11: 350 to 5000 MHz Receive Mixer with PLL and VCO	SKY73208-11	TW18-D245-003