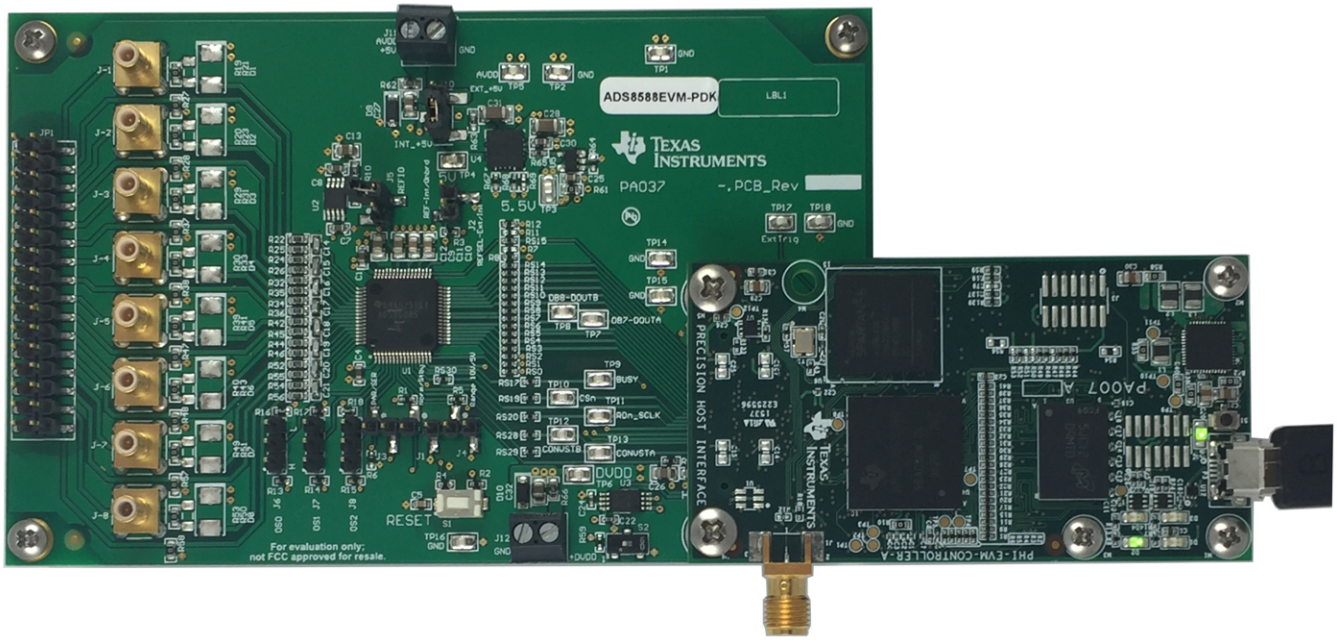
ADS8588SEVM-PDK User's Guide



This user's guide describes the characteristics, operation, and use of the ADS8588S evaluation module (EVM) performance demonstration kit (PDK). The ADS8588S is an 8-channel, simultaneous sampling, integrated data acquisition system based on a 16-bit successive approximation (SAR) analog-to-digital converter (ADC). Each input channel on the device supports true bipolar input ranges of ±10 V and ±5 V with single-supply operation. The device includes an analog front end offering a 1-MΩ, constant resistive input impedance. The ADS8588SEVM supports all the mentioned features while also providing provisions for an external reference, user-selectable oversampling ratio, and features eight input channels. The EVM-PDK eases the evaluation of ADS8588S device and devices derived from the ADS85XX family with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials using the ADS8588S device as an example throughout the document.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
ADS8588S	SBAS642
ADS8588H	SBAS843
ADS8598S	SBAS827
ADS8598H	SBAS829
REF5025	SBOS410
TPS3836K33	SLVS292
TPS7A4700	SBVS204

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1 Overview

The ADS8588SEVM-PDK is a platform for evaluating the performance of the ADS85xx family. The EVM-PDK comes with the ADS8588S SAR ADC, an 8-channel, 16-bit, ±10-V and ±5-V input range, simultaneous sampling ADC device. The evaluation kit includes the ADS8588SEVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis.

The ADS8588SEVM board includes the ADS8588S SAR ADC, all the peripheral analog circuits, and components required to extract optimum performance from the ADC.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS8588SEVM
- Supplies power to all active circuitry on the ADS8588SEVM board

Along with the ADS8588SEVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS8588SEVM-PDK Features

The ADS8588SEVM-PDK includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS85xx family of SAR ADC devices.
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS8588S ADC over a USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Windows 7® and Windows 8®, 64-bit operating systems
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, and linearity analysis. This suite also has a provision for exporting data to a text file for post-processing.

1.2 ADS8588SEVM Features

The ADS8588SEVM includes the following features:

- Onboard SMB connectors and RC input filters
- Jumper-selectable onboard precision 2.5-V voltage reference or the ADS85xx family devices internal reference
- Jumper-selectable ±10-V range or ±5-V range
- Jumper-selectable parallel, parallel-byte or serial interface
- Onboard, ultralow noise, low-dropout (LDO) regulator for excellent 5.0-V, single-supply regulation of the ADC and onboard voltage reference.

2 EVM Analog Interface

The ADS8588SEVM is designed for easy interfacing to analog sources. The Samtec™ connector provides a convenient 16-pin, dual-row, header JP1 accessing channels AIN1-AIN8 of the device. In addition, 8 SMB connectors , J-1 to J-8, provide a high quality connection to channels AIN1-AIN8. Figure 1 shows the ADS8588SEVM analog input connections and input RC filters for channels AIN1 to AIN8. Table 1 lists the analog interface connections for header JP1 and Table 2 lists the analog interface connections for the SMB connectors.

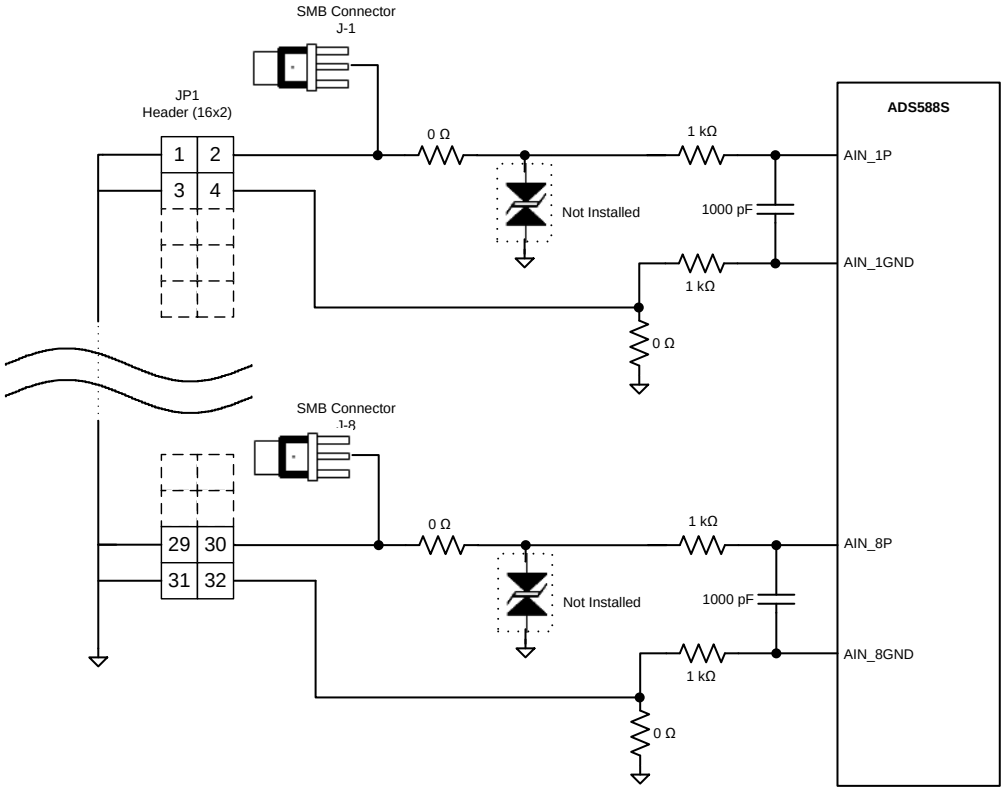

Figure 1. ADS8588SEVM Analog Input Connections for Channels AIN_1 to AIN_8

Table 1. JP1 Header Analog Interface Connections

Header Pin Number	Signal	Description
JP1.2	AIN_1P	Positive analog input for channel AIN1
JP1.4	AIN_1GND	Negative analog input for channel AIN1
JP1.6	AIN_2P	Positive analog input for channel AIN2
JP1.8	AIN_2GND	Negative analog input for channel AIN2
JP1.10	AIN_3P	Positive analog input for channel AIN3
JP1.12	AIN_3GND	Negative analog input for channel AIN3
JP1.14	AIN_4P	Positive analog input for channel AIN4
JP1.16	AIN_4GND	Negative analog input for channel AIN4
JP1.18	AIN_5P	Positive analog input for channel AIN5
JP1.20	AIN_5GND	Negative analog input for channel AIN5
JP1.22	AIN_6P	Positive analog input for channel AIN6
JP1.24	AIN_6GND	Negative analog input for channel AIN6
JP1.26	AIN_7P	Positive analog input for channel AIN7
JP1.28	AIN_7GND	Negative analog input for channel AIN7
JP1.30	AIN_8P	Positive analog input for channel AIN8
JP1.32	AIN_8GND	Negative analog input for channel AIN8

Table 2. SMB Analog Interface Connections

SMB Connector	Signal	Description
J-1	AIN_1	Analog input for channel AIN1
J-2	AIN_2	Analog input for channel AIN2
J-3	AIN_3	Analog input for channel AIN3
J-4	AIN_4	Analog input for channel AIN4
J-5	AIN_5	Analog input for channel AIN5
J-6	AIN_6	Analog input for channel AIN6
J-7	AIN_7	Analog input for channel AIN7
J-8	AIN_8	Analog input for channel AIN8

2.1 ADS8588S Internal Reference and EVM Onboard Reference

The ADS8588S device incorporates an internal 2.5-V reference. Alternatively, the user can select the onboard 2.5-V reference, REF5025 (U2). The reference voltage source is determined by setting REFSEL(pin 34) of the ADS8588S device. By default, the evaluation module is set up with the ADS8588S internal reference source, with jumper J5 open. If the onboard REF5025 2.5-V reference is desired, a shunt jumper must be placed on J5 and the external reference must be selected by navigating to the ADS8588SEVM *Configuration Settings* tab in the graphical user interface (GUI). For more information, see Section 6.1. The output of the REF5025 is filtered through a passive RC filter and connected to the REFIO pin of the ADS8588S using jumper J5. The schematic for the reference circuit is shown in Figure 2.

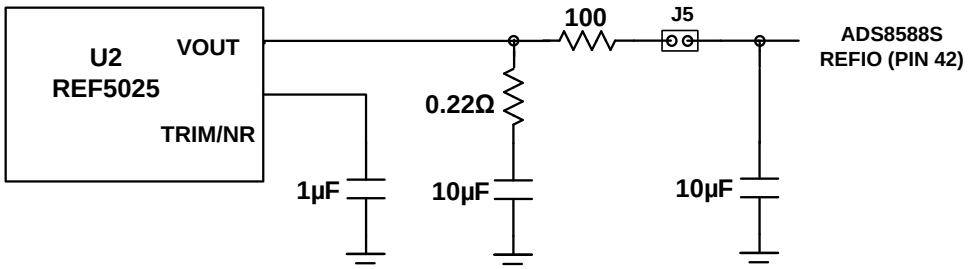

Figure 2. REF5025 2.5-V External Reference Source

3 Digital Interfaces

As noted in Section 1, the EVM interfaces with the PHI that, in turn, communicates with the computer over USB. There are two devices on the EVM with which the PHI communicates: the ADS8588S ADC (over dual SDO serial interface or a parallel interface) and the EEPROM (over I^2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS8588SEVM-PDK platform. The EEPROM is initially programmed to communicate with the ADS8588S, but can be reprogrammed for any of the supported devices in the ADS85xx device family through their respective GUI software. See Section 5.2 for more information and instructions. After the hardware is initialized, the EEPROM is no longer used.

3.1 ADS8588S Digital Interface

The ADS8588SEVM-PDK supports parallel, parallel byte and serial digital interface as detailed in the ADS8588S data sheet. The PHI controller is configured to operate at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC. The digital interface configuration can be selected by navigating to the ADS8588SEVM Interface *Configuration Settings* tab in the GUI. For more information, see Section 6.1.

Socket strip connector J9 provides the digital I/O connections between the ADS8588SEVM board and the PHI controller.

Table 3 summarizes the pin-outs for connector J9.

Table 3. Digital I/O Connections for Connector J9

Pin Number	Signal	Description
J9.6, J9.8, J9.10, J9.12, J9.14, J9.16, J9.18, J9.20,J9.22, J9.24, J9.26, J9.28, J9.30	DB15, DB14, DB13, DB12, DB10, DB9, DB8/DOUTB, DB7/DOUTA, DB6, DB5, DB4, DB3	Parallel or serial data output connections
J9.32	CSn	CS select, active low
J9.36	RD/SCLK	Active-low ready input pin in parallel and parallel byte interface, clock input pin in serial interface mode
J9.38, J9.40, J9.42	DB2, DB1, DB0	Parallel data output connections
J9.44	CONVSTB	Active high logic input to control start of conversion for second half count of device input channels
J9.46	CONVSTA	Active high logic input to control start of conversion for first half count of device input channels
J9.48	RANGE	Pin is used to select input range of device (±10 V or ±5 V)
J9.50	DVDD	3.3-V digital supply from the PHI controller board
J9.56, J9.58	I^2C Bus	I^2C bus; used only to read the EEPROM (U3) in the EVM board
J9.3, J9.60	GND	Ground connections
J9.23	BUSY	Active-high digital output indicating ongoing conversion
J9.29	REFSEL	Active-high logic input to enable the internal reference.
J9.31	FRSDATA	Active-high digital output indicating data read back from channel 1 of the devices
J9.33	RESET	Active-high logic input to reset the device
J9.37	STBY	Active-low logic input to enter device into one of the two power down modes: standby or shutdown
J9.39	PAR/SER/BYTE SEL	Logic input pin to select between parallel, serial, or parallel byte interface mode
J9.41, J943, J9.45	OS0, OS1, OS2	Oversampling mode control pins
J9.59	ID_POWER	Power supply used only to power the EEPROM (U3) in the EVM board

4 Power Supplies

The ADS8588S ADC analog supply (AVDD) is provided by a low-noise linear regulator (TPS7A4700). The regulator uses a 5.5-V supply out of a switching regulator from the PHI controller to generate a quiet and stable 5.0-V supply output. The 3.3-V supply to the digital supply of the ADS8588S is provided directly by an LDO from the PHI controller. The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper filled areas where possible between bypass capacitors and their loads to minimize inductance along the load current path.

CAUTION

When using the ADS8588SEVM in conjunction with the PHI controller, install a shunt between J10 pins 2-3 as shown in Figure 3 The PHI controller supplies the AVDD and DVDD power supplies. Do not use external power supply voltages or the device may be damaged.

CAUTION

When using the ADS8588SEVM as a stand-alone board, install a shunt between J10 pins 1-2, and supply the analog supply (AVDD) on connector J11, and the digital supply (DVDD) on connector J12. Make sure AVDD voltage is in the range between 4.75 V to 5.25 V, and make sure DVDD is in the range 2.3 V < DVDD < AVDD for proper device operation. Do not exceed the absolute maximum ratings for the ADS8588S device, or damage may occur.

5 Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for the proper operation of the ADS8588SEVM-PDK.

5.1 Default Jumper Settings

NOTE: Make sure jumpers J1-J4 and jumpers J6-J8 are in the default OPEN configuration while interfacing the ADS8588SEVM board with the PHI controller, as described in Table 4. The PHI controller controls the settings of these digital inputs functions through the EVM GUI; otherwise, the PHI controller cannot set the state of the digital inputs.

Install a shunt between J10 pins 2-3 as shown on Figure 3 to select the onboard regulated AVDD 5.0 V supply option. Figure 3 details the default jumper settings.Table 4 explains the configuration for these jumpers.

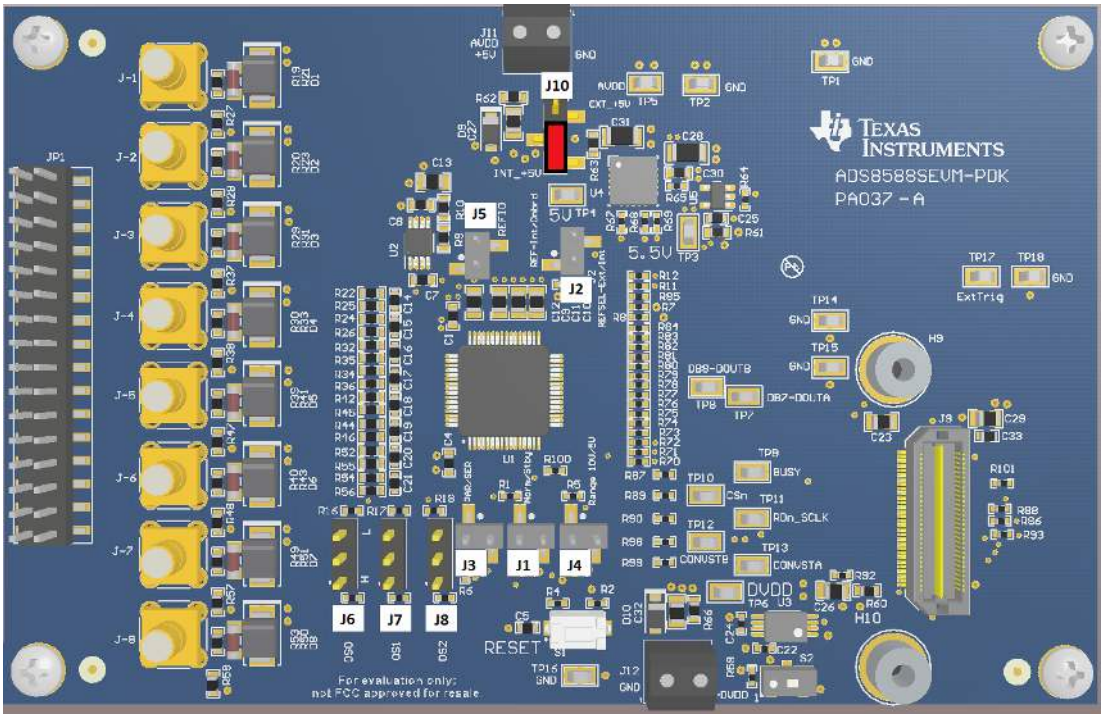

Figure 3. ADS8588SEVM Default Jumper Settings

Table 4. Default Jumper Configuration

Jumper	Function	Default Position	Description
J1	STDBY	Open	Open selects Normal mode, Closed selects STBY mode
J2	REFSEL	Open	Open selects internal reference Closed selects external reference
J3	PARn/SER	Open	Open selects Parallel Interface, Closed selects Serial Interface
J4	RANGE	Open	Open selects ±10 V range, Closed selects ±5 V range
J5	REFIO	Open	Open when using internal reference, Closed connects external on-board reference
J6	OS0	Open	1-2 Sets OS0=0, 2-3 Sets OS0=1
J7	OS1	Open	1-2 Sets OS1=0, 2-3 Sets OS1=1
J8	OS2	Open	1-2 Sets OS2=0, 2-3 Sets OS2=1
J10	AVDD Ext/Int	Closed between pins 2 and 3	2-3 Onboard regulated AVDD 5.0V supply option, 1-2 Alternative AVDD supply option from external source

5.2 EVM Graphical User Interface (GUI) Software Installation

NOTE: Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Otherwise, depending on the antivirus settings, an error message may appear or the *installer.exe* file may be deleted.

The following steps list the directions to install the software using the ADS8588S as an example. If evaluating a different supported device from the ADS85xx device family, remove U1 (the ADS8588S) from the EVM board and populate the board using the device under test (DUT). Download and install the respective DUT software GUI from the *Tools and Software* folder of the ADS8588SEVM-PDK. Administrator privileges are required on the PC to install the EVM software.

Table 5. ADS85xx Supported Devices by ADS8588SEVM

Device	Literature Number
ADS8588S	SBAS642
ADS8588H	SBAS843
ADS8598S	SBAS827
ADS8598H	SBAS829

After downloading and starting the GUI installer, accept the license agreements and follow the on-screen instructions to complete the installation, as shown in Figure 4.

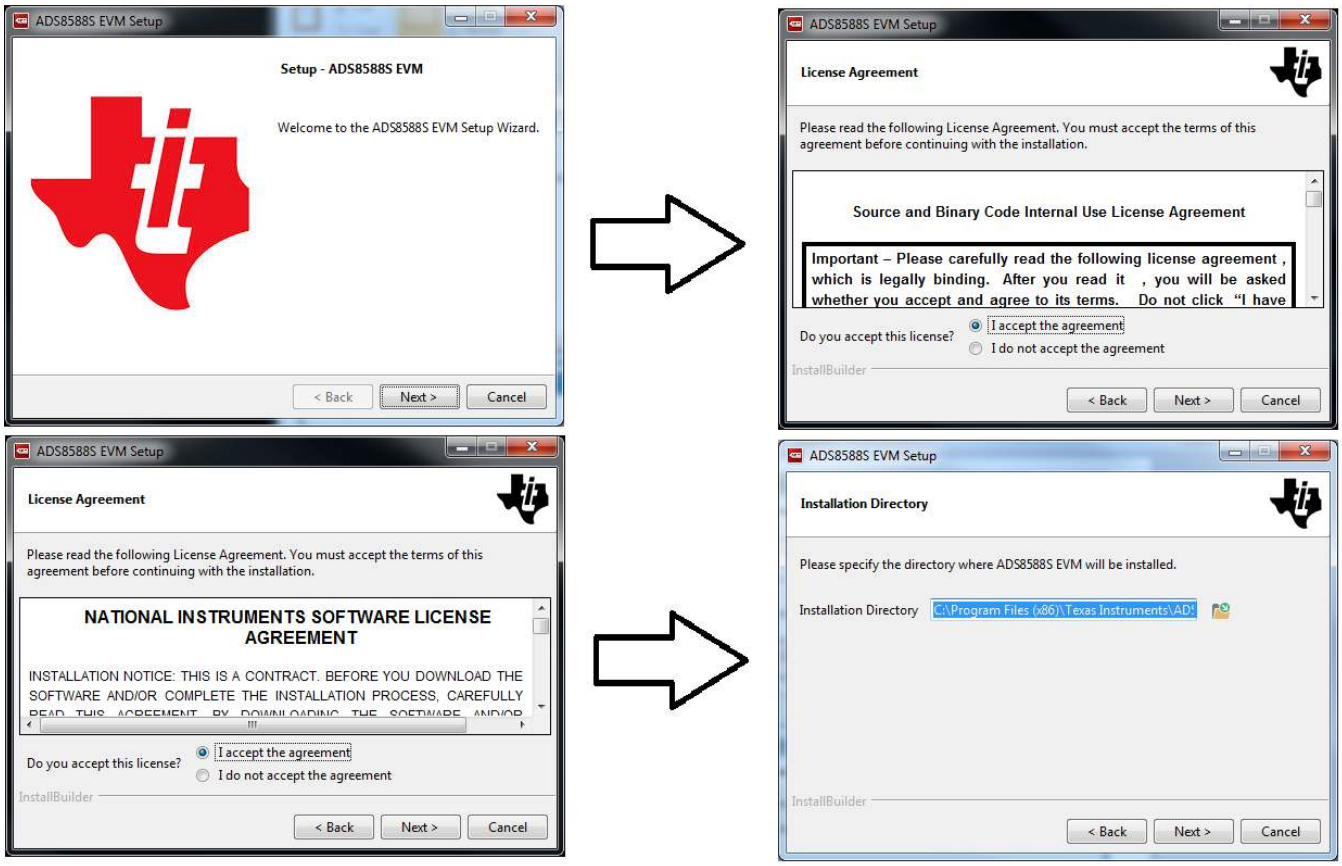

Figure 4. Software Installation Prompts

As a part of the ADS8588S EVM GUI installation, a prompt with a *Device Driver Installation* appears on the screen, as shown in Figure 5. Click *Next* to proceed.

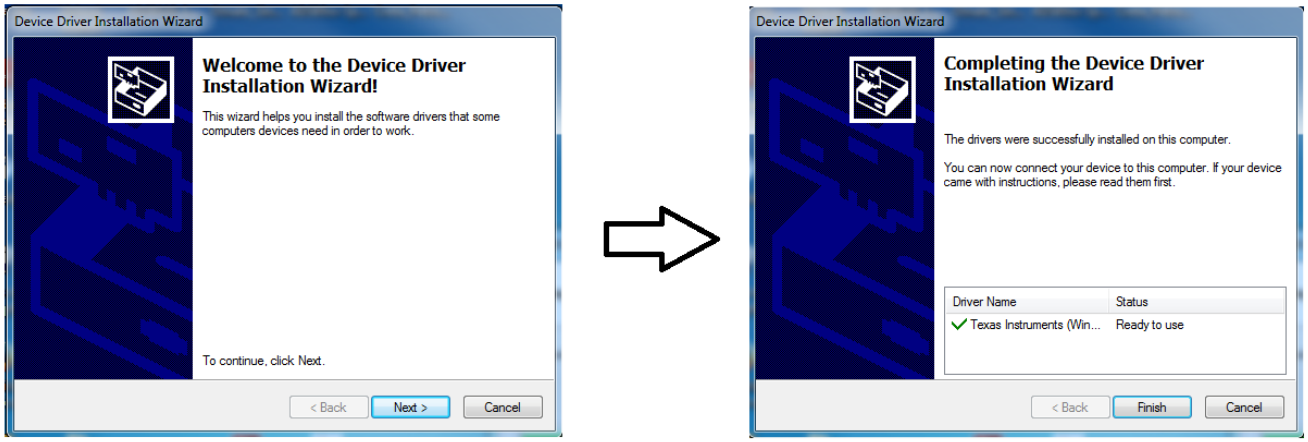

Figure 5. ADS8588S Device Driver Installation Wizard Prompts

NOTE: A notice may appear on the screen stating that Widows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS8588SEVM-PDK requires the LabVIEW™ Run-Time Engine. If not already installed, a prompt will appear for the installation of this software, as shown in Figure 6.

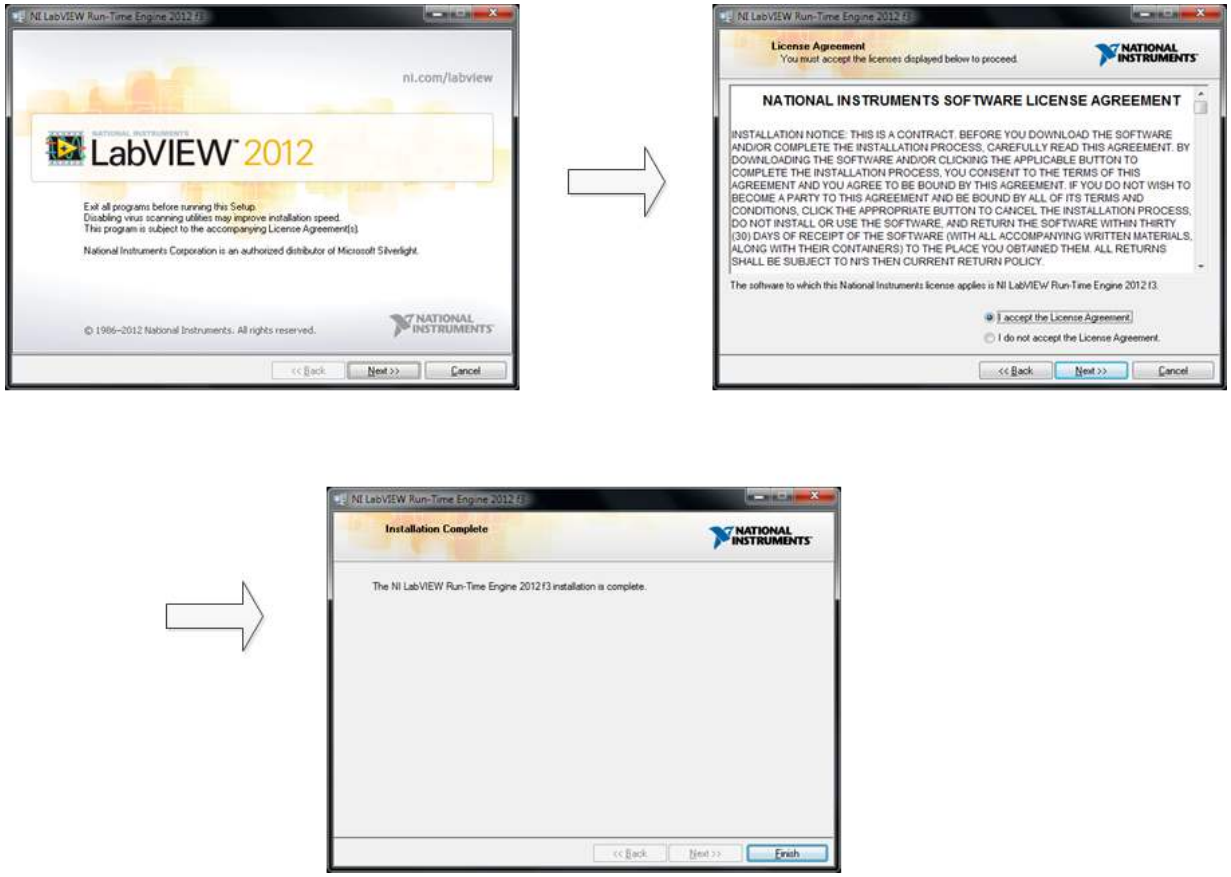

Figure 6. LabVIEW Run-Time Engine Installation

After these installations, verify that the contents of *C:\Program Files (x86)\Texas Instruments\ADS8588S EVM* is as shown in Figure 7.

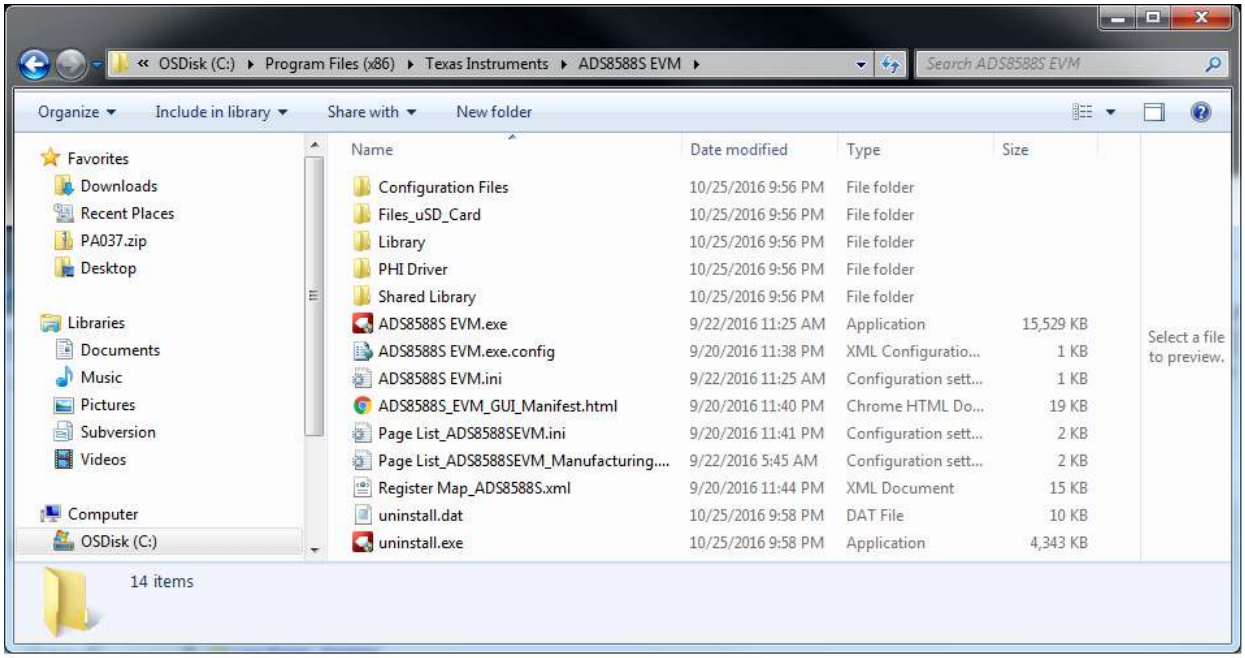

Figure 7. ADS8588S EVM Folder Post-Installation

6 Operation

The following instructions are a step-by-step guide to connecting the ADS8588S to the computer and evaluating the performance of the ADS8588S:

1. Connect the ADS8588SEVM to the PHI. Install the two screws as indicated in Figure 8.
2. Use the USB cable provided to connect the PHI to the computer.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI starts blinking to indicate that the PHI is booted up and communicating with the PC. The resulting LED indicators are shown in Figure 8.

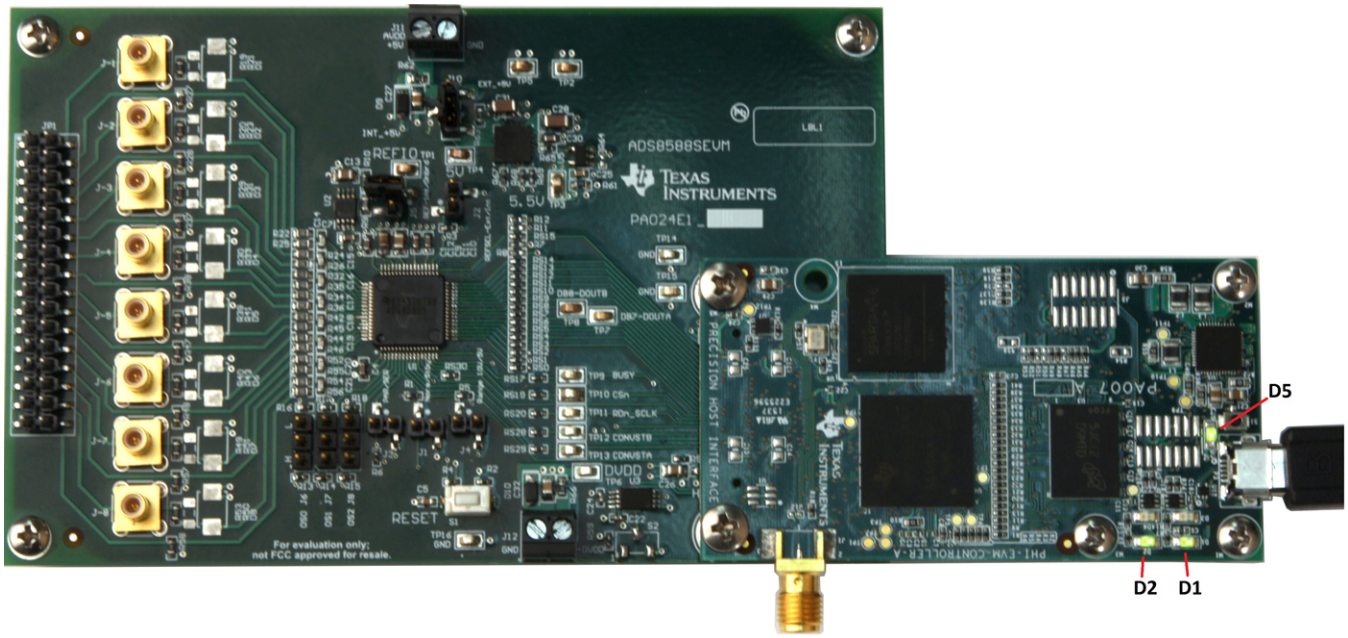

Figure 8. ADS8588SEVM-PDK Hardware Setup and LED Indicators

3. Double click the *ADS8588S EVM.exe* file to launch the EVM GUI, as shown in Figure 9.

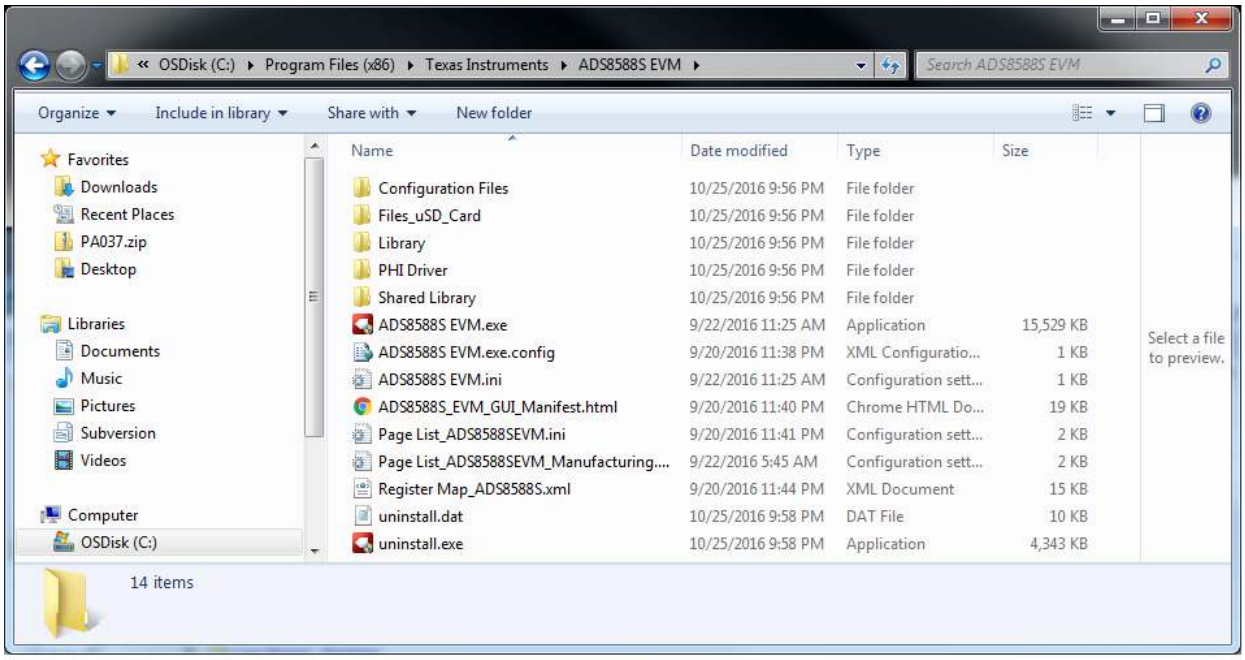

Figure 9. Launch the ADS8588SEVM GUI Software

4. If a different DUT other than the ADS8588S is evaluated, the prompt shown in Figure 10 appears. Move switch S2 to position 2-3 (to the right) to disable the EEPROM write protect. Click on the *Load EEPROM* button to reprogram the onboard EEPROM to the DUT GUI being used. Make sure the corresponding GUI to the DUT populated on the EVM board is used. If the incorrect GUI is used, compatibility issues can occur even though the GUI may seem to run correctly. After EEPROM is loaded, move switch S2 back to position 1-2 (to the left) to enable write protect.

Figure 10. Load EEPROM Prompt

NOTE: The installed GUI must correspond with the device under test (DUT) populated on the ADS8588SEVM board. If GUI does not correspond to the DUT on the EVM board, performance and parameters will not be correct even though communication is still achieved.

6.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the voltage levels and timing configuration of the ADC digital interface, the EVM GUI provide high-level control over the ADS8588S interface modes and RD/SCLK clock frequency. In addition, the EVM GUI provides control to device configuration settings such as range selection, sampling rate, reference selection, oversampling settings, and number of samples to be captured.

Figure 11 shows the *Interface Configuration* pane at the bottom left, through which various functions of the ADS8588S are exercised. These are global settings; they persist across the different GUI tools or GUI pages listed in the top left plane.

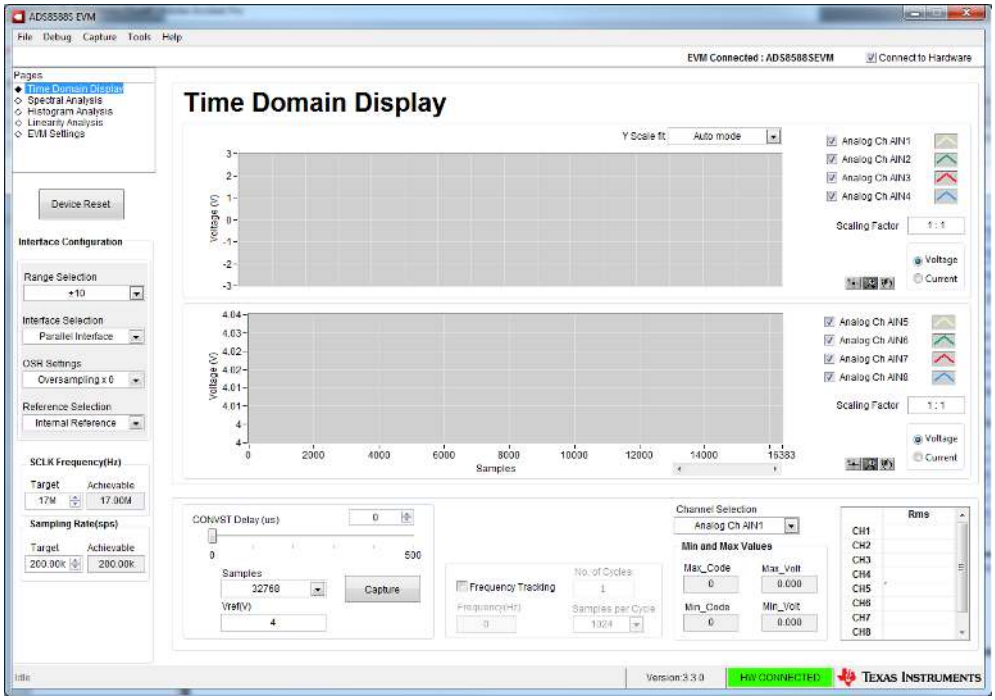

Figure 11. EVM GUI Global Input Parameters

The *Range Selection* field is used to select the input range of the device: ±10 V or ±5 V.

The drop-down menu in the *Interface Selection* field allow the choice of three interface options: parallel, parallel byte, or serial. Parallel interface communication occurs through the DB[15:0] parallel bus, parallel byte through the DB[7:0] parallel bus, and serial interface communication through a dual serial output: DB7/DOUTA and DB8/DOUTB.

The ADS8588S device supports an oversampling mode of operation using an on-chip averaging digital filter, as explained in the device datasheet. The oversampling ratio (OSR) settings drop-down menu in the EVM GUI provides selectable oversampling ratios of 2x, 4x, 8x, 16x, 32x, and 64x.

SCLK Frequency and *Sampling Rate* can also be selected on this pane, depending on the selected interface and OSR settings. Enter the targeted values for these two parameters, and the GUI considers the timing constraints of the selected interface and computes the best values that can be achieved.

Enter a *Target* value in the *SCLK Frequency (Hz)* field, and the GUI matches this frequency as closely as possible by changing the PHI PLL settings, and then displaying the *Achievable* frequency that may differ from the entered *Target* value. Similarly, adjust the ADC *Sampling Rate (sps)* by entering a *Target* value (Hz = sps). The *Achievable* ADC sampling rate can differ from the *Target* value, depending on the applied RD/SCLK frequency and selected Interface. The closest achievable match is then displayed. Therefore, this pane allows the various settings available on the ADS8588S to be tested in an iterative fashion until the best settings for the corresponding test scenario are achieved.

The *Device Reset* button in the GUI functions as a master reset to both the ADS8588S EVM and the GUI. When this button is pressed, the ADC resets to the default settings shown in Figure 11.

6.2 Time Domain Display Tool

The *Time Domain Display* tool allows visualization of the time domain conversion results given a set of analog input signals.

The ADS8588S requires two conversion control digital signals: conversion start A (CONVSTA) and conversion start B (CONVSTB), as explained in the device-specific data sheet. CONVSTA is used to simultaneously sample and initiate the conversion of the first half count of the ADS8588S input channels (channels 1-4). CONVSTB is used for the latter half count of the device input channels (channels 5-8). By default, the PHI controller and EVM software trigger the CONVSTA and CONVSTB signals at the same time, producing a simultaneous conversion on all eight channels. Alternatively, a delay between CONVSTA and CONVSTB can be programmed by using the *CONVST Delay* field in the GUI. The achievable ADC sampling rate may differ from the target value, depending on the applied CONVSTA/B delay, and the closest achievable match is displayed and executed.

The GUI *Time Domain Display* shows two time domain voltage plots: the top time domain plot shows the conversion results for channels 1-4, and channels 4-8 conversion results are shown in the bottom display. The sample indices are on the x-axis and there are two y-axes showing the corresponding converted analog voltages. Any combination of desired channels can be selected using the *Analog CH AINx* selection buttons at the top-right side of the display.

When the *Capture* button is pressed, the software captures a contingent number of samples that are selected in the *Samples* field, as shown in Figure 12. In addition, the bottom-right side of the GUI provides information about the converted signals, such as the selected channel maximum and minimum code, maximum and minimum voltage, and the calculated RMS voltage value for the captured signal on each channel.

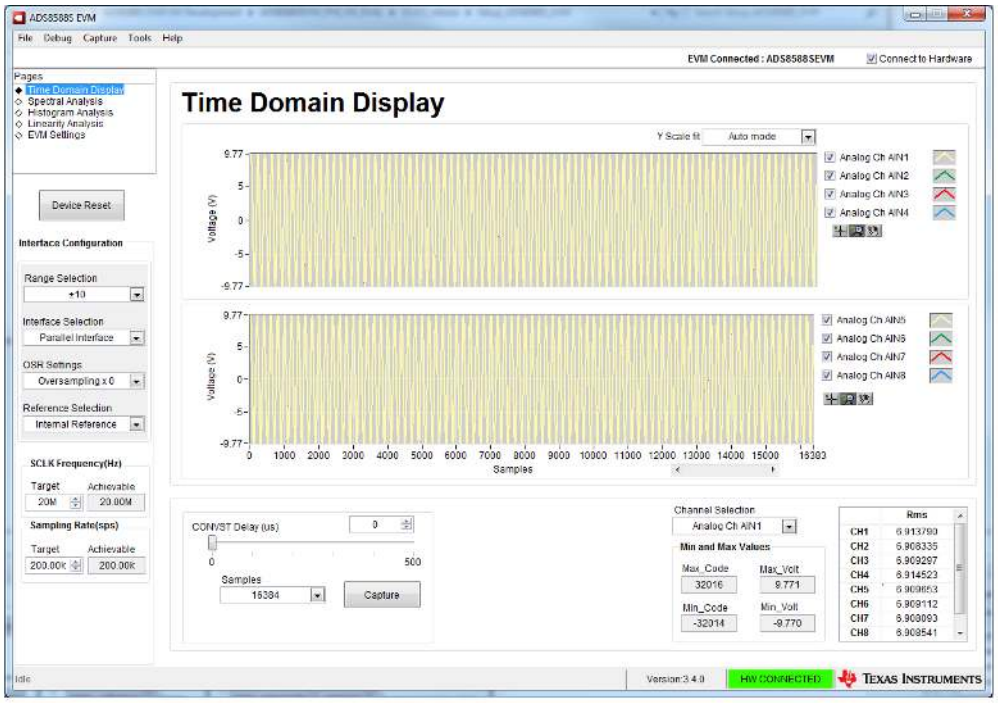

Figure 12. Time Domain Display

6.3 Spectral Analysis Tool

The spectral analysis tool is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of ADS8588S SAR ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting.

For dynamic performance evaluation, the external differential source must have better specifications than the ADS8588S device in order to make sure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements mentioned in Table 6.

Table 6. External Source Requirements for Evaluation of the ADS8588S

Specification Description	Specification Value
Signal frequency	1 kHz (OSR = 0)
External source type	Single ended
External source common-mode	0 V
Maximum noise	35 μV_{RMS}
Maximum SNR	100 dB
Maximum THD	–110 dB

For 1-kHz SNR and ENOB evaluation at a maximum throughput of 200 kSPS, the optimal number of samples is 32768. More samples brings the noise floor so low that the external source phase noise can dominate the SNR and ENOB calculations. The spectral analysis tool is shown in Figure 13.

Figure 13. Spectral Analysis Tool

Finally, the FFT tool includes windowing options that are required to mitigate the effects of noncoherent sampling (a discussion that is beyond the scope of this document). The 7-Term Blackman Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window), and is not recommended.

6.4 Histogram Analysis Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate *effective resolution*, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC, is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

The histogram corresponding to a dc input is displayed on clicking on the *Capture* button, as shown in Figure 14.

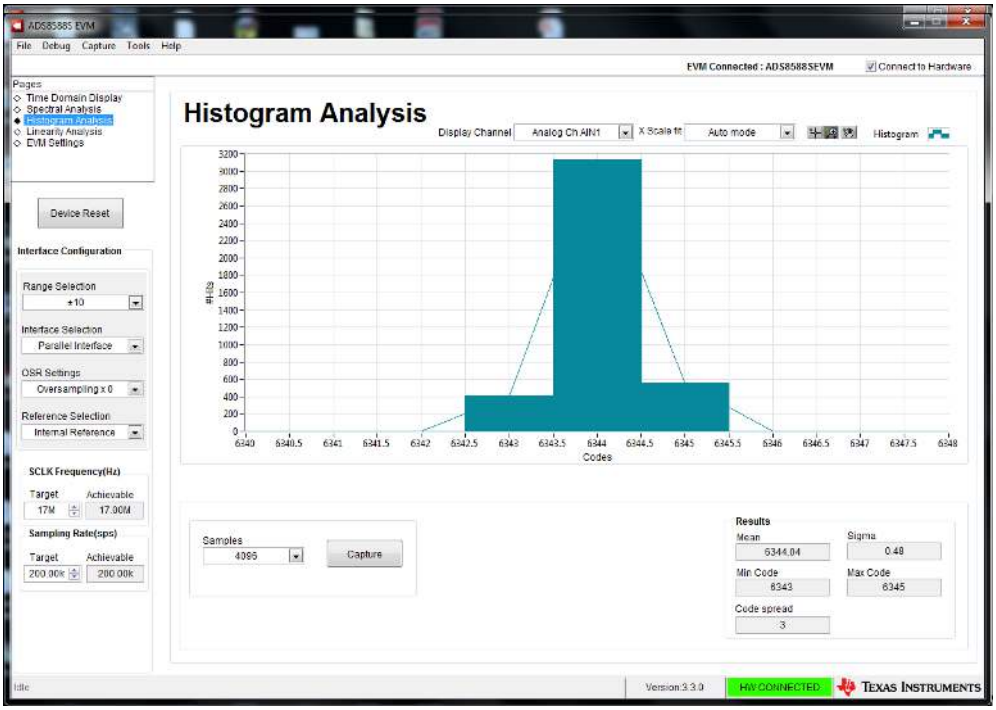

Figure 14. Histogram Analysis Tool

6.5 Linearity Analysis Tool

The linearity analysis tool measures and generates the performance DNL and INL plots over code for the ADS8588S. A 1-kHz sinusoidal input signal is required, which is slightly saturated (100 mV to 200 mV outside the full-scale range) at each input with very low distortion. The external source linearity must be better than the ADC linearity. The measured system performance must reflect the linearity errors of the ADC and must not be limited by the performance of the signal source. To make sure that the DNL and INL of the ADC are correctly measured, the external source must meet the requirements in Table 7.

Table 7. External Source Requirements for ADS8588S Evaluation

Specification Description	Specification Value
Signal frequency	1 kHz
External source type	Single ended, referred to GND
External source common mode	0 V
Signal Amplitude	10.2 Vp for ±10-V range; 5.1 Vp for for ±5-V range
Maximum noise	35 μV_{RMS}
Maximum SNR	100 dB
Maximum THD	–110 dB

The *number-of-hits* setting depends on the external noise source. For a 100-dB SNR external source with approximately 30 µVrms of noise, the total number of hits must be 256. The linearity analysis tool is shown in Figure 15.

NOTE: This analysis can take a couple of minutes to run; therefore, the evaluation board must remain undisturbed during the complete duration of the analysis.

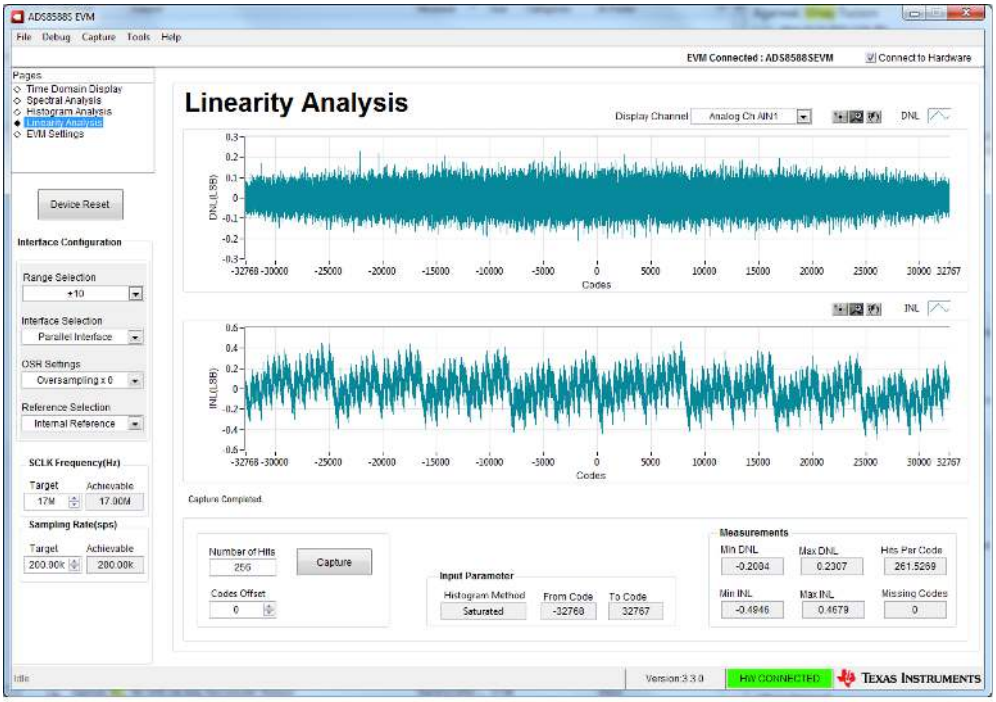

Figure 15. Linearity Analysis Tool

7 Bill of Materials, PCB Layout, and Schematics

This section contains the ADS8588S EVM bill of materials (BOM), printed circuit board (PCB) layout, and the EVM schematics.

7.1 Bill of Materials

Table 8 lists ADS8588S EVM BOM.

Table 8. ADS8588S EVM Bill of Materials

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
PA037	1	N/A	Any	Printed Circuit Board for Evaluation of ADS8588S
PHI-EVM-CONTROLLER (Edge# 6591636 rev. B)	1	N/A	Texas Instruments	USB Controller Board for ADC EVMs (Kit Item)
C1608X7R1C105K	7	C1, C2, C3, C4, C7, C8, C30	TDK	CAP, CERM, 1 µF, 16 V, ± 10%, X7R, 0603
06035A102KAT2A	10	C5, C14, C15, C16, C17, C18, C19, C20, C21, C33	AVX	CAP, CERM, 1000 pF, 50 V, ± 10%, C0G/NP0, 0603
GRM21BR71A106KE51L	9	C6, C9, C12, C13, C23, C26, C27, C29, C32	MuRata	CAP, CERM, 10 µF, 10 V, ± 10%, X7R, 0805
0805YD105KAT2A	2	C10, C11	AVX	CAP, CERM, 1 µF, 16 V, ± 10%, X5R, 0805
C1005X7R1H104K	2	C22, C24	TDK	CAP, CERM, 0.1 µF, 50 V, ± 10%, X7R, 0402
C0603C104J3RAC	1	C25	Kemet	CAP, CERM, 0.1 µF, 25 V, ± 5%, X7R, 0603
C3216X5R1E476M160AC	2	C28, C31	TDK	CAP, CERM, 47 µF, 25 V, ± 20%, X5R, 1206
MMSZ4690T1G	2	D9, D10	ON Semiconductor	Diode, Zener, 5.6 V, 500 mW, SOD-123
PMSSS 440 0025 PH	4	H1, H2, H3, H4	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
1891	4	H5, H6, H7, H8	Keystone	Hex Standoff, #4-40, Aluminum, 1/4"
9774050360R	2	H9, H10	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM
RM3X4MM 2701	2	H14, H15	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
TSM-102-01-L-SV	5	J1, J2, J3, J4, J5	Samtec	Header, 100 mil, 2x1, Gold with Tin Tail, SMT
TSW-103-07-G-S	3	J6, J7, J8	Samtec	Header, 100 mil, 3x1, Gold, TH
QTH-030-01-L-D-A	1	J9	Samtec	Header(Shrouded), 19.7 mil, 30x2, Gold, SMT
TSM-103-01-L-SV	1	J10	Samtec	Header, 100 mil, 3x1, Gold, SMT
ED555/2DS	2	J11, J12	On-Shore Technology	Terminal Block, 6A, 3.5 mm Pitch, 2-Pos, TH
131-3701-261	8	J-1, J-2, J-3, J-4, J-5, J-6, J-7, J-8	Emerson Network Power	Connector, SMB,Vertical RCP 0-4GHz, 50 Ω, TH
TSM-116-01-T-DV-P	1	JP1	Samtec	Header, 100 mil, 16x2, Tin, SMT
CRCW04025K10JNED	7	R1, R2, R8, R12, R13, R14, R15	Vishay-Dale	RES, 5.1 k, 5%, 0.063 W, 0402
CRCW040210K0JNED	7	R3, R4, R6, R16, R17, R18, R59	Vishay-Dale	RES, 10 k, 5%, 0.063 W, 0402
CRCW0402100KFKED	1	R5	Vishay-Dale	RES, 100 k, 1%, 0.063 W, 0402
RT0603BRD07100RL	1	R9	Yageo America Panasonic Vishay-Dale	RES, 100, 0.1%, 0.1 W, 0603
ERJ-3RQFR22V	1	R10	Panasonic	RES, 0.22, 1%, 0.1 W, 0603

Table 8. ADS8588S EVM Bill of Materials (continued)

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
CRCW06030000Z0EA	17	R19, R20, R27, R28, R29, R30, R37, R38, R39, R40, R47, R48, R49, R50, R57, R58, R61	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603
RG1608P-102-B-T5	16	R22, R24, R25, R26, R32, R34, R35, R36, R42, R44, R45, R46, R52, R54, R55, R56	Susumu Co Ltd	RES, 1.00 k, 0.1%, 0.1 W, 0603
CRCW06035R11FKEA	3	R60, R62, R66	Vishay-Dale	RES, 5.11, 1%, 0.1 W, 0603
ERJ-3RSFR10V	1	R63	Panasonic	RES, 0.1, 1%, 0.1 W, 0603
CRCW04020000Z0ED	4	R64, R65, R67, R68	Vishay-Dale	RES, 0, 5%, 0.063 W, 0402
CRCW040249R9FKED	32	RS0, RS1, RS2, RS3, RS4, RS5, RS6, RS7, RS8, RS9, RS10, RS11, RS12, RS13, RS14, RS15, RS16, RS17, RS18, RS19, RS20, RS21, RS22, RS23, RS24, RS25, RS26, RS27, RS28, RS29, RS30, RS31	Vishay-Dale	RES, 49.9, 1%, 0.063 W, 0402
EVQPNF04M	1	S1	Panasonic	Switch, Tactile, SPST-NO, 0.05A, 12 V, SMD
CAS-120TA	1	S2	Copal Electronics	Switch, Slide, SPDT 100 mA, SMT
881545-2	2	SH-J1, SH-J2	TE Connectivity	Shunt, 100 mil, Gold plated, Black
5015	18	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18	Keystone	Test Point, Miniature, SMT
ADS8588SIPMR	1	U1	Texas Instruments	8 channel, 16 bit, ±10 V Simultaneous Sampling SAR ADC with Single Supply Operation, PM0064A
REF5025IDGKT	1	U2	Texas Instruments	Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125°C, 8-pin MSOP(DGK), Green (RoHS & no Sb/Br)
BR24G32FVT-3AGE2	1	U3	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
TPS7A4700RGWR	1	U4	Texas Instruments	36-V, 1-A, 4.17-uVRMS, RF LDO Voltage Regulator, RGW0020A
TPS3836K33DBVR	1	U5	Texas Instruments	NanoPower Supervisory Circuits, DBV0005A
SMBJ14CA	0	D1, D2, D3, D4, D5, D6, D7, D8	Littelfuse	Diode, TVS, Bi, 14 V, 600 W, SMB
CRCW04025K10JNED	0	R7, R11	Vishay-Dale	RES, 5.1 k, 5%, 0.063 W, 0402
MMA02040C1000FB300	0	R21, R23, R31, R33, R41, R43, R51, R53	Vishay/Beyschlag	RES, 100, 1%, 0.4 W, AEC-Q200 Grade 0, 1.4x3.6 mm
CRCW04020000Z0ED	0	R69	Vishay-Dale	RES, 0, 5%, 0.063 W, 0402

7.2 PCB Layout

Figure 17 through Figure 21 illustrate the EVM PCB layout.

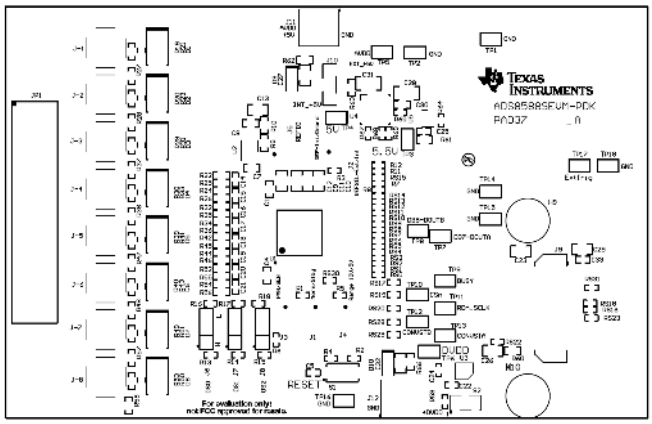

Figure 16. ADS8588S EVM PCB: Top Overlay

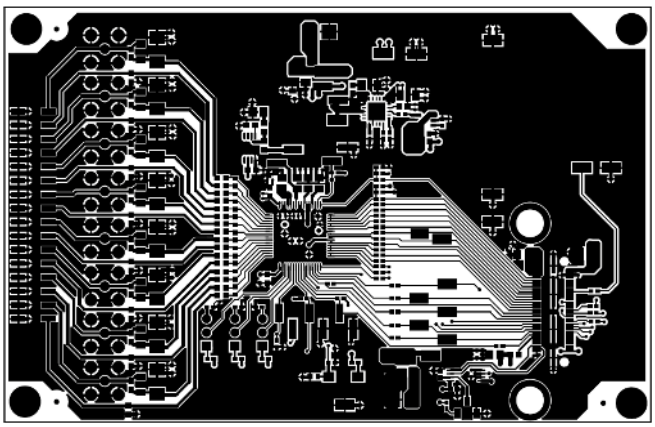

Figure 17. ADS8588S EVM PCB Layer 1: Top Layer

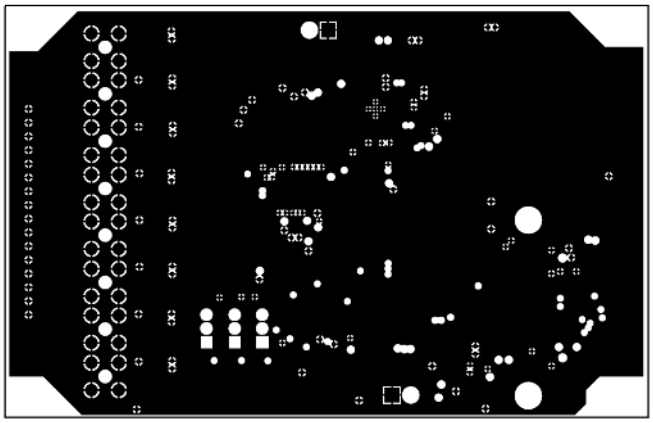

Figure 18. ADS8588S EVM PCB Layer 2: GND Plane

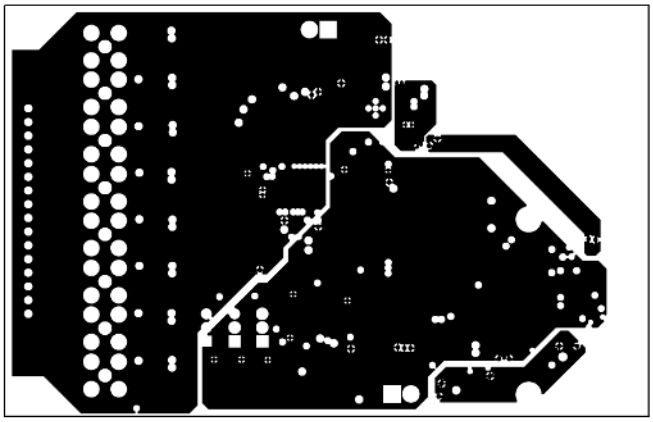

Figure 19. ADS8588S EVM PCB Layer 3: Power Planes

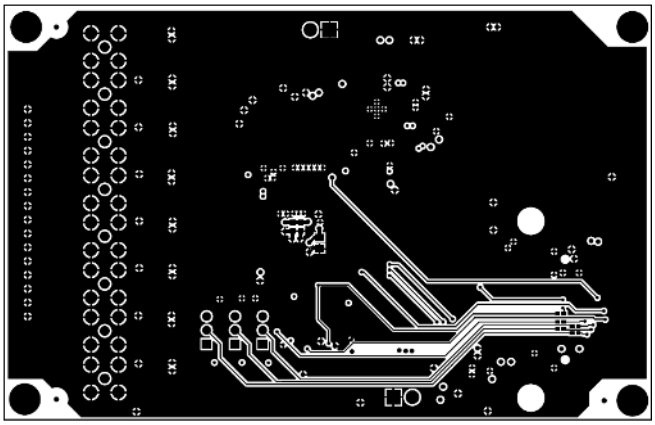

Figure 20. ADS8588S EVM PCB Layer 4: Bottom Layer

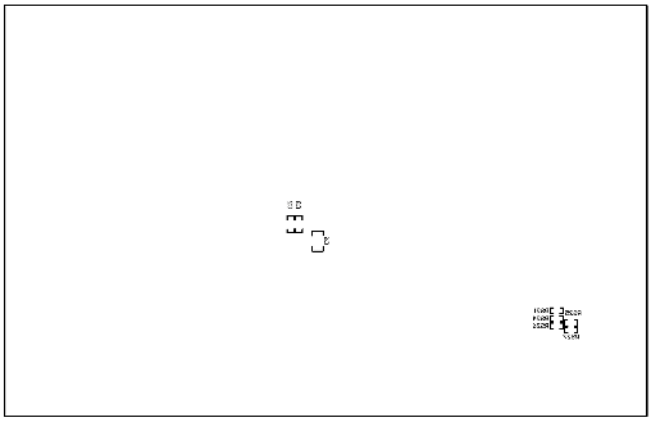

Figure 21. ADS8588S EVM PCB: Bottom Overlay

7.3 Schematics

Figure 22 through Figure 22 illustrate the EVM schematics.

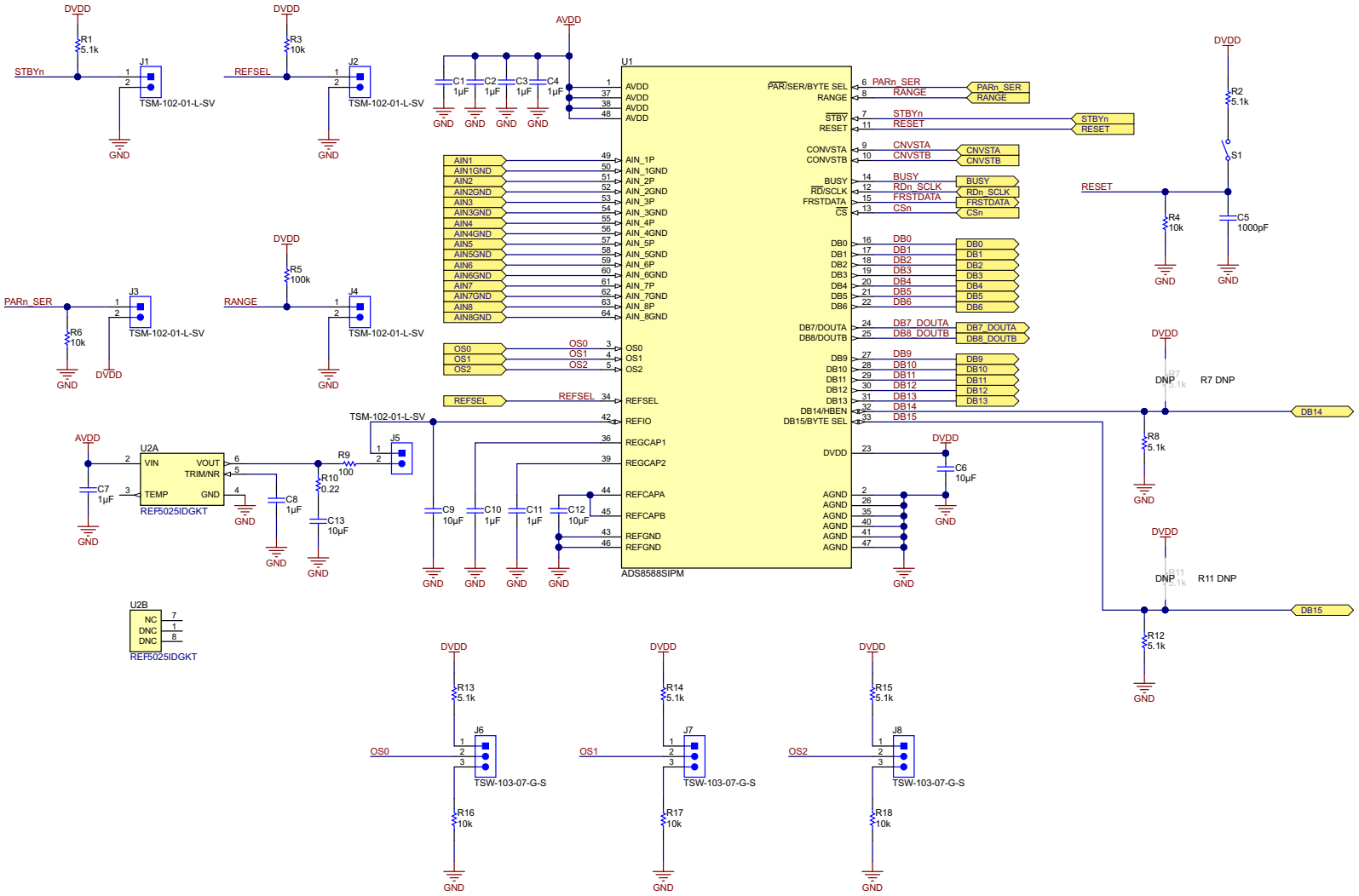

Figure 22. ADS8588EVM-PDK Schematic

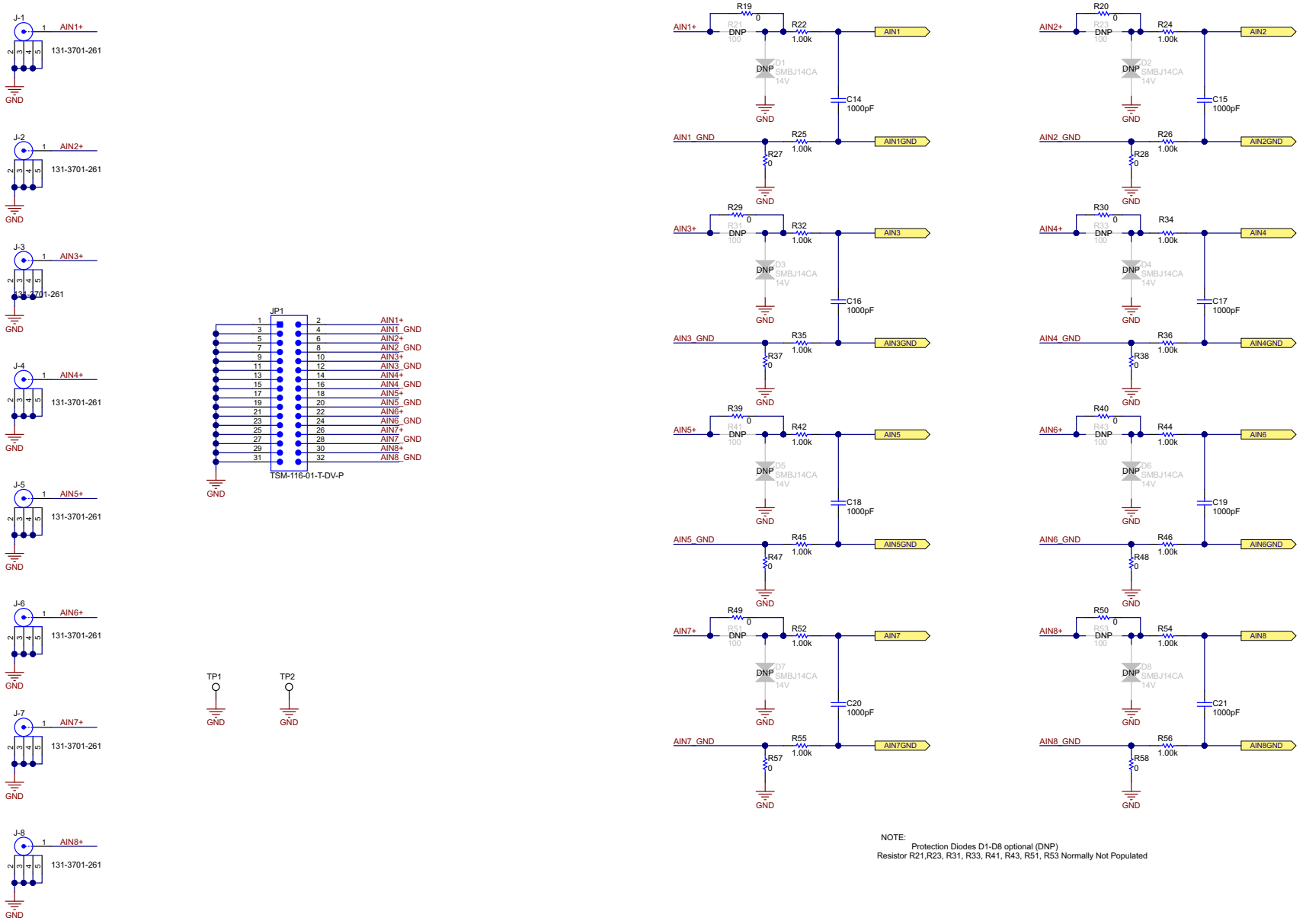

Figure 23. ADS8588EVM-PDK Schematic

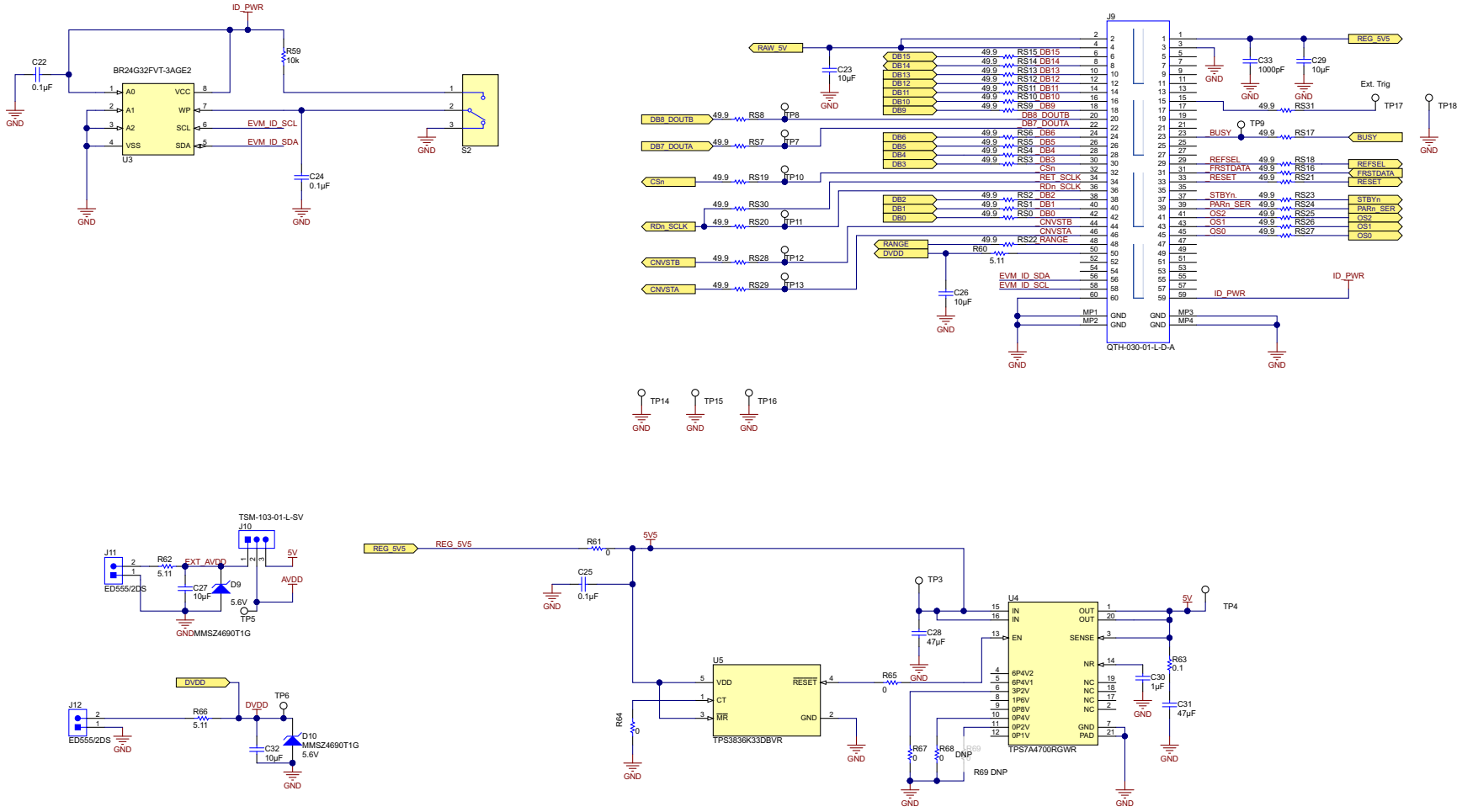

Figure 24. ADS8588EVM-PDK Schematic

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (August 2017) to B Revision **Page**

- Added new related devices to Table 1 1
- Added new supported devices to Table 5 10

Changes from Original (November 2016) to A Revision **Page**

- Changed user's guide to clarify the use of multiple devices in the ADS85xx family 1
- Changed ADS8588S to ADS8588SEVM in third bullet of section 1 4
- Changed AIN0 to AIN1 in first paragraph of section 2 5
- Changed EPROM to EEPROM in first paragraph of section 3 7
- Changed first paragraph of section 5.2 to include GUI installation for ADS85xx family of devices 10
- Added Table 5 to list supported devices 10
- Added new step 4 to section 6 instructions; describing connection of EVM to computer 14
- Added missing figure number and caption for Figure 15 19

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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