CS5106

Multi-Feature, Synchronous plus Auxiliary PWM Controller

The CS5106 is a fixed frequency, current mode controller with one single NFET driver and one dual FET, synchronous driver. The synchronous driver allows for increased efficiency of the main isolated power stage and the single driver allows the designer to develop auxiliary supplies for controller power as well as secondary side house keeping. In addition, because the synchronous drivers have programmable FET non−overlap, the CS5106 is an ideal controller for soft−switched converter topologies.

The CS5106 is specifically designed for isolated topologies where speed, flexibility, reduced size and reduced component count are requirements. The controller contains the following features: Undervoltage Shutdown, Overvoltage Shutdown, Programmable Frequency, Programmable Synchronous Non−Overlap Time, Master/Slave Clocking with Frequency Range Detection, Enable, Output Undervoltage Protection with Timer, 20 mA 5.0 V Output, 80 ns PWM propagation delay, and Controlled Hiccup Mode.

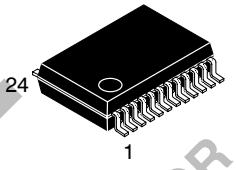
The CS5106 has junction temperature and supply ranges of −40°C to 125°C and 9.0 V to 16 V respectively and is available in the 24 lead SSOP package.

Features

- Programmable Fixed Frequency
- Programmable FET Non−Overlap
- Enable Lead
- 12 V Fixed Auxiliary Supply Control
- Under and Overvoltage Shutdown
- Output Undervoltage Protection with Timer
- Master/Slave Clock Sync Capability
- Sync Frequency Range Detection
- 80 ns PWM Propagation Delay
- 20 mA 5.0 V Reference Output
- Small 24 Lead SSOP Package
- Controlled Hiccup Mode

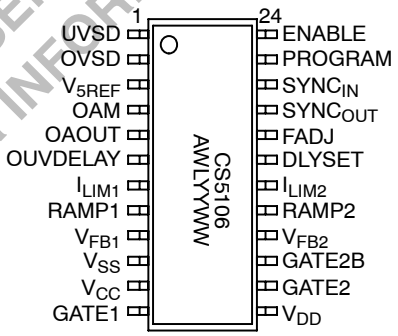
ON Semiconductor™

http://onsemi.com



SSOP−24
SW SUFFIX
CASE 940D

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS5106LSW24	SSOP−24	59 Units/Rail
CS5106LSWR24	SSOP−24	2000 Tape & Reel

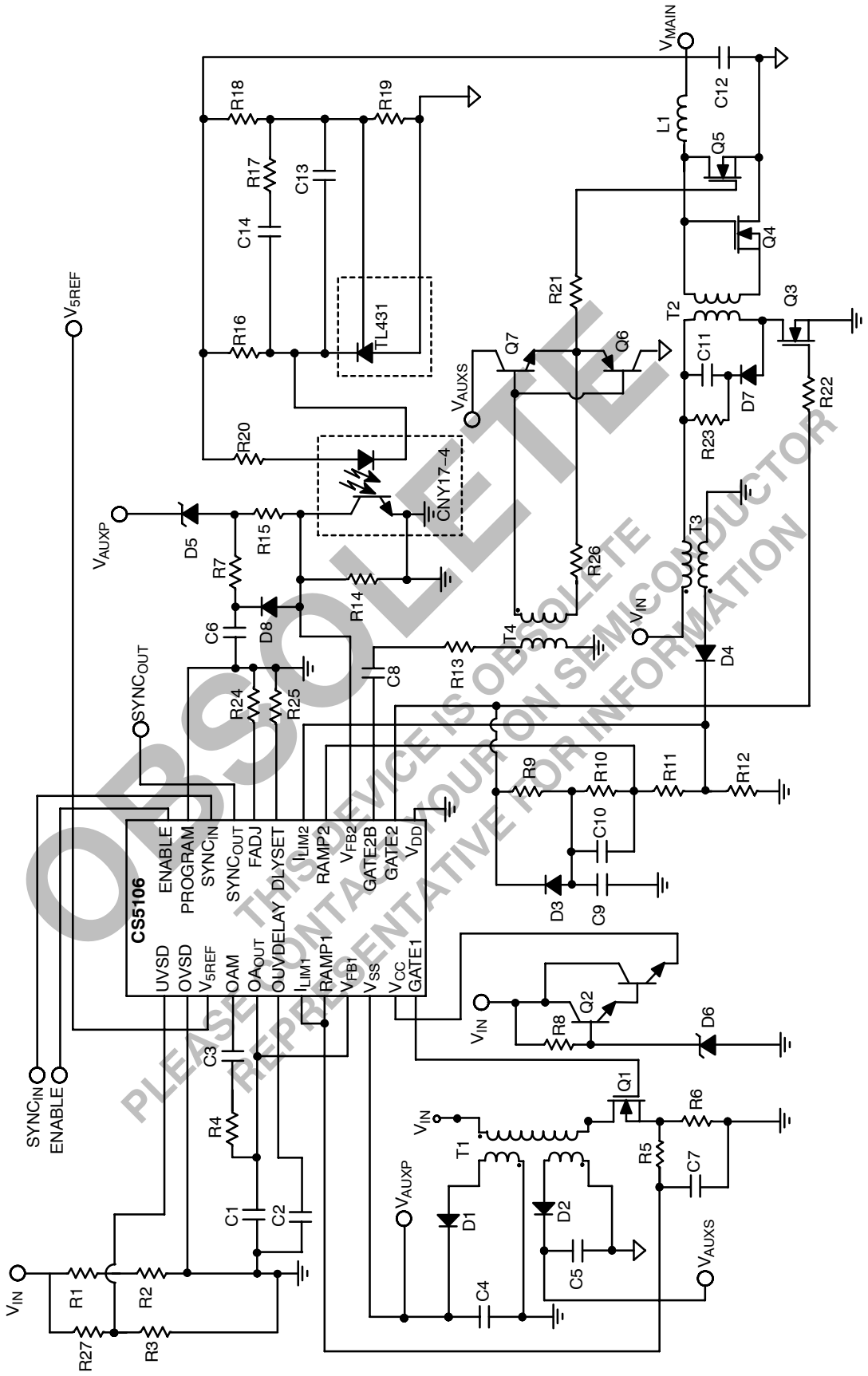


Figure 1. Application Diagram, 48 V to 3.3 V Forward Converter with Synchronous Rectifiers

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature, T_J	150	°C
Operating Temperature Range, T_A	−40 to 85	°C
Storage Temperature Range, T_S	−65 to +150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
Undervoltage Shutdown Input	UVSD	6.0 V	−0.3 V	1.0 mA	N/A
Overvoltage Shutdown Input	OVSD	6.0 V	−0.3 V	1.0 mA	N/A
5.0 V Reference Output	V_{5REF}	6.0 V	−0.3 V	150 mA	25 mA
Error Amp Minus Input	OAM	6.0 V	−0.3 V	250 μA	1.2 mA
Error Amp Output	OAOUT	6.0 V	−0.3 V	300 μA	100 mA
Output Overcurrent Timer Capacitor	OUVDELAY	6.0 V	−0.3 V	15 μA	N/A
Auxiliary Primary Side Current Limit Input	I_{LIM1}	6.0 V	−0.3 V	10 μA	N/A
Auxiliary Primary Side Current Ramp Input	RAMP1	6.0 V	−0.3 V	10 μA	N/A
Auxiliary Voltage Feedback Input	V_{FB1}	6.0 V	−0.3 V	5.0 μA	100 μA
Bootstrapped Power Input	V_{SS}	20 V	−0.3 V	2.0 μA	0.5 A Peak, 300 mA DC
Main Power Input	V_{CC}	20 V	−0.3 V	See Note 2	0.5 A Peak, 300 mA DC
Auxiliary FET Driver Output	GATE1	20 V	−0.3 V	0.5 A Peak, 100 mA DC	0.5 A Peak, 100 mA DC
Ground	GND	0 V	0 V	0.5 A Peak	N/A, 300 mA DC
Synchronous FET Driver Output	GATE2	20 V	−0.3 V	0.5 A Peak, 100 mA DC	0.5 A Peak, 100 mA DC
Synchronous FET Driver Output B	GATE2B	20 V	−0.3 V	0.5 A Peak, 100 mA DC	0.5 A Peak, 100 mA DC
Synchronous Voltage Feedback Input	V_{FB2}	6.0 V	−0.3 V	10 μA	100 μA
Synchronous Primary Side Current Ramp Input	RAMP2	6.0 V	−0.3 V	10 μA	N/A
Synchronous Primary Side Current Limit Input	I_{LIM2}	6.0 V	−0.3 V	10 μA	N/A
Gate Non−Overlap Programming Input	DLYSET	2.5 V	−0.3 V	125 μA	N/A
Frequency Programming Input	FADJ	2.5 V	−0.3 V	125 μA	N/A
Clock Master Output	$SYNC_{OUT}$	6.0 V	−0.3 V	50 mA	100 mA
Clock Slave Input	$SYNC_{IN}$	6.0 V	−0.3 V	N/A	1.0 mA
Enable Programming Input	PROGRAM	16 V	−0.3 V	30 μA	N/A
Enable Input	ENABLE	16 V	−0.3 V	300 μA	N/A

2. Current out of V_{CC} is not limited. Care should be taken to prevent shorting V_{CC} to Ground.

ELECTRICAL CHARACTERISTICS (T_J = −40°C to 125°C, V_{SS} = 9.0 to 16 V, V_{5REF} I_{LOAD} = 2.0 mA, $SYNC_{OUT}$ Free Running, unless otherwise specified. For All Specs: UVSD = 6.0 V, OVSD = 0 V, ENABLE = 0 V, $I_{LIM(1,2)}$ = 0, $V_{FB(1,2)}$ = 3.0 V, R_{FADJ} = R_{DLYSET} = 27.4 kΩ.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{SS} Supply Current					
V_{SS} Supply Current	Measure current into V_{SS} when V_{5REF} I_{LOAD} = 0 mA. 9.0 V ≤ V_{SS} ≤ 13 V.	–	16	23	mA
	Measure current into V_{SS} when V_{5REF} I_{LOAD} = 0 mA. 13 V < V_{SS} ≤ 16 V.	–	16	25	mA
	Measure current into V_{SS} when V_{5REF} I_{LOAD} = 0 mA. 16 V < V_{SS} ≤ 20 V.	–	16	30	mA
Low V_{CC} Supply Current					
Low V_{CC} Supply Current	Float V_{SS}. Set V_{CC} = 7.0 V & measure V_{CC} current while V_{5REF} I_{LOAD} = 0 mA.	–	1.5	3.5	mA
V_{SS} to V_{CC} Diode					
Diode ON Voltage	Measure V_{SS} − V_{CC}	0.2	0.75	1.0	V
Reference					
5.0 V Internal Voltage Reference	Measure V_{REF} voltage when I_{REF} = 0 and I_{REF} = 20 mA	4.85	5.0	5.15	V
V_{REF}OK Threshold	Adjust V_{REF} from 4.8 V−4.0 V until PWM1,2 goes low.	4.3	4.55	4.7	V
Low V_{CC} Lockout					
V_{CC} Turn−on Threshold Voltage	V_{CC} increasing until I_{CC} > 3.5 mA V_{5REF} I_{LOAD} = 0 mA	7.0	7.25	7.5	V
V_{CC} Turn−off Threshold Voltage	V_{CC} decreasing until I_{CC} < 3.5 mA V_{5REF} I_{LOAD} = 0 mA	6.3	6.7	7.1	V
Hysteresis	Turn−on − Turn−off	0.40	0.55	0.70	V
Clock					
Operating Frequency1	Measure frequency from $SYNC_{OUT}$.	485	512	540	kHz
$SYNC_{IN}$ Input Impedance	Measure input impedance.	7.0	15	–	kΩ
$SYNC_{OUT}$ Output Low Voltage	R_{LOAD} = 2.0 kΩ to V_{5REF}	–	1.0	1.5	V
$SYNC_{OUT}$ Output High Voltage	R_{LOAD} = 2.0 kΩ to GND	3.5	4.2	–	V
$SYNC_{IN}$ Detect Frequency	Verify $SYNC_{OUT}$ = $SYNC_{IN}$, R_{LOAD} = 2.0 kΩ to GND	425	–	555	kHz
Max. Low SYNC Rej. Frequency	Verify $SYNC_{OUT}$ = FCLK when R_{LOAD} = 2.0 kΩ to GND	–	–	340	kHz
Min. High SYNC Rej. Frequency	Verify $SYNC_{OUT}$ = FCLK when R_{LOAD} = 2.0 kΩ to GND	690	–	–	kHz
$SYNC_{IN}$ Input Threshold Voltage	Functional Testing Verify FCLK from 1.0 V to 2.8 V	0.9	1.85	2.9	V
Main PWM Clock Pulse Width	(GBD) − CLPH1 One Shot Pulse Width	80	100	120	ns
Aux PWM Clock Pulse Width	(GBD) − CLPH2 One Shot Pulse Width	80	100	120	ns

ELECTRICAL CHARACTERISTICS (continued) (T_J = −40°C to 125°C, V_{SS} = 9.0 to 16 V, V_{5REF} I_{LOAD} = 2.0 mA, $SYNC_{OUT}$ Free Running, unless otherwise specified. For All Specs: UVSD = 6.0 V, OVSD = 0 V, ENABLE = 0 V, $I_{LIM(1,2)}$ = 0, $V_{FB(1,2)}$ = 3.0 V, R_{FADJ} = R_{DLYSET} = 27.4 kΩ.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Bias Supply Error Amplifier					
Output Low Voltage	V_{SS} > 12.6 V. Measure OAOUT voltage when sinking 1.0 mA.	–	43	85	mV
Output High Voltage	V_{SS} < 11.4 V. Measure OAOUT voltage when sourcing 150 μA.	4.55	4.75	–	V
Output High Source Current	V_{SS} < 11.4 V. Measure OAOUT source current when OAOUT = 0.5 V	150	225	300	μA
Output Low Sink Current	V_{SS} > 12.6 V. Measure OAOUT sink current when OAOUT = 2.5 V.	3.0	20	50	mA
V_{SS} Set Point	Adjust V_{SS} until OAOUT goes low.	11.6	12.25	12.8	V
Large Signal Gain	(GBD)	15	–	–	V/mV
Unity Gain Bandwidth	(GBD)	–	1.0	–	MHz
Common Mode Input Range	(GBD)	1.0	–	2.0	V
V_{SS} Voltage					
V_{SS} Reset Voltage	Toggle ENABLE between GND & V_{CC}, then adjust V_{SS} from 2.0 V–0.8 V until OAOUT goes high.	1.0	1.4	1.8	V
Undervoltage Lockout					
UVSD Turn–On Threshold Voltage	Adjust UVSD from 4.7 V–5.3 V until GATE1,2 goes high.	4.8	5.0	5.1	V
UVSD Turn–Off Threshold Voltage	Adjust UVSD from 5.1 V–4.3 V until GATE1,2 goes low.	4.45	4.7	4.95	V
Hysteresis	Turn–on – Turn–off	0.2	0.27	0.4	V
UVSD Input Bias Current	Set UVSD = 0 V. Measure Current out of UVSD lead.	–	0.2	0.5	μA
Overvoltage Lockout					
OVSD Threshold Voltage	Adjust OVSD from 4.7 V–5.3 V until GATE1,2 goes low.	4.85	5.0	5.15	V
OVSD Input Bias Current	Set OVSD = 0 V. Measure Current out of OVSD lead.	–	0.2	0.5	μA
ENABLE & PROGRAM					
ENABLE Lead Output Current	Measure current out of ENABLE when ENABLE = 0 V	100	266	500	μA
PROGRAM Lead Output Current	Measure current out of PROGRAM when PROGRAM = 0 V	20	60	100	μA
PROGRAM Threshold Voltage	ENABLE = GND. Adjust PROGRAM from 1.0 V–1.8 V until GATE1,2 goes high.	1.2	1.4	1.6	V
ENABLE Threshold Voltage	PROGRAM = GND. Adjust ENABLE from 1.0 V–1.8 V until GATE1,2 goes high.	1.2	1.4	1.6	V

ELECTRICAL CHARACTERISTICS (continued) (T_J = −40°C to 125°C, V_{SS} = 9.0 to 16 V, V_{5REF} I_{LOAD} = 2.0 mA, $SYNC_{OUT}$ Free Running, unless otherwise specified. For All Specs: UVSD = 6.0 V, OVSD = 0 V, ENABLE = 0 V, $I_{LIM(1,2)}$ = 0, $V_{FB(1,2)}$ = 3.0 V, R_{FADJ} = R_{DLYSET} = 27.4 kΩ.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Undervoltage Delay					
OUVDELAY Charging Current	Set OUVDELAY = 1.0 V, V_{FB1} = 4.4 V Measure OUVDELAY I_{CHARGE}.	7.5	10	12.5	μA
OUVDELAY Latch−off Voltage	Toggle ENABLE between GND & V_{CC}, then adjust OUVDELAY from 4.7 V−5.3 V until GATE1,2, goes low.	4.8	5.0	5.2	V
OUVDELAY Set Current	OUVDELAY = VOCLO + 50 mV. Measure current into OUVDELAY.	−	0.5	1.0	mA
V_{FB1} Charge Threshold	V_{SS} = 1.0 V. Toggle ENABLE between GND & V_{CC}, adjust V_{FB1} from 3.8 V−4.6 V until GATE1,2 goes low.	4.05	4.22	4.4	V
V_{FB2} Charge Threshold	V_{SS} = 1.0 V. Toggle ENABLE between GND & V_{CC}, adjust V_{FB2} from 3.8 V−4.6 V until GATE1,2 goes low.	3.9	4.15	4.35	V
Current Limit Circuits					
I_{LIM1} Current Limit Threshold Voltage	Adjust I_{LIM1} from 1.0 V−1.3 V until GATE1 goes low.	1.16	1.24	1.3	V
I_{LIM1} Short Circuit Threshold Voltage	Adjust I_{LIM1} from 1.30 V−1.50 V until GATE1 skips 2−cycles with reference to $SYNC_{OUT}$.	1.35	1.44	1.51	V
I_{LIM1} Input Bias Current	Set I_{LIM1} = 0 V. Measure current out of I_{LIM1} lead.	−	0.5	5.0	μA
I_{LIM2} Current Limit Threshold Voltage	Adjust I_{LIM2} from 1.0 V−1.3 V until GATE2 goes low.	1.16	1.24	1.3	V
I_{LIM2} Short Circuit Threshold Voltage	Adjust I_{LIM2} from 1.30 V−1.50 V until GATE2 skips 2−cycles with reference to $SYNC_{OUT}$.	1.35	1.44	1.51	V
I_{LIM2} Input Bias Current	Set I_{LIM2} = 0 V. Measure current out of I_{LIM2} lead.	−	0.5	5.0	μA
Voltage Feedback Control					
RAMP1 Offset Voltage	V_{FB1} = 0 V. Adjust RAMP1 from 0 V−0.3 V until GATE1 goes low. Measure V_{RAMP1}.	0.08	0.13	0.2	V
RAMP1 Input Bias Current	Set RAMP1 = 0 V. Measure Current out of RAMP1 lead.	−	0.5	5.0	μA
RAMP2 Offset Voltage	V_{FB2} = 0 V. Adjust RAMP2 from 0 V−3.0 V until GATE2 goes low. Measure V_{RAMP2}.	0.08	0.13	0.2	V
RAMP2 Input Bias Current	Set RAMP2 = 0 V. Measure Current out of RAMP2 lead.	−	0.5	5.0	μA
V_{FB1} Input Impedance	Measure input impedance.	60	120	220	kΩ
V_{FB2} Input Impedance	Measure input impedance.	60	120	220	kΩ

ELECTRICAL CHARACTERISTICS (continued) (T_J = −40°C to 125°C, V_{SS} = 9.0 to 16 V, V_{5REF} I_{LOAD} = 2.0 mA, $SYNC_{OUT}$ Free Running, unless otherwise specified. For All Specs: UVSD = 6.0 V, OVSD = 0 V, ENABLE = 0 V, $I_{LIM(1,2)}$ = 0, $V_{FB(1,2)}$ = 3.0 V, R_{FADJ} = R_{DLYSET} = 27.4 kΩ.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Gate1, 2, 2B, Output Voltages	**V_{SS} = 12 V. V_{CC} = V_{SS} − V_{DON}**				
GATE1 Low State	PROGRAM = 0 V. Measure GATE1 voltage when sinking 1.0 mA.	–	0.15	0.8	V
GATE2 Low State	PROGRAM = 0 V. Measure GATE2 voltage when sinking 1.0 mA.	–	0.18	0.8	V
GATE2B Low State	PROGRAM = 0 V. Measure GATE2B voltage when sinking 1.0 mA.	–	0.18	0.8	V
GATE2B High State	Measure V_{CC} − GATE2B voltage when sourcing 1.0 mA.	–	1.65	2.0	V
GATE2 High State	Measure V_{CC} − GATE2 voltage when sourcing 1.0 mA.	–	1.65	2.0	V
GATE1 High State	Measure V_{CC} − GATE1 voltage when sourcing 1.0 mA.	–	1.65	2.0	V
Propagation Delays					
I_{LIM1} Delay to Output GATE1	Measure delay from I_{LIM1} going high to GATE1 going low.	–	80	120	ns
I_{LIM2} Delay to Output GATE2	Measure delay from I_{LIM2} going high to GATE2 going low.	–	80	100	ns
RAMP1 Delay to Output GATE1	Measure delay from RAMP1 going high to GATE1 going low.	–	80	115	ns
RAMP2 Delay to Output GATE2	Measure delay from RAMP2 going high to GATE2 going low.	–	80	100	ns
GATE2, 2B Non−Overlap Delay					
GATE2 Turn−on Delay from GATE2B	Measure delay from GATE2B going low @ 1.7 V to GATE2 going high @ 1.7 V.	20	45	70	ns
GATE2B Turn−on Delay from GATE2	Measure delay from GATE2 going low @ 1.7 V to GATE2B going high @ 1.7 V.	20	45	70	ns
GATE1, 2, 2B Rise & Fall Times	**V_{SS} = 12 V, V_{CC} = V_{SS}−V_{DON}**				
GATE1 Rise Time	Measure GATE1 Rise Time from 90% to 10%. C_{LOAD} = 150 pF.	–	50	80	ns
GATE1 Fall Time	Measure GATE1 Fall Time from 10% to 90%. C_{LOAD} = 150 pF.	–	30	60	ns
GATE2 Rise Time	Measure GATE2 Rise Time from 90% to 10%. C_{LOAD} = 50 pF.	–	50	80	ns
GATE2 Fall Time	Measure GATE2 Fall Time from 10% to 90%. C_{LOAD} = 50 pF.	–	15	30	ns
GATE2B Rise Time	Measure GATE2B Rise Time from 90% to 10%. C_{LOAD} = 50 pF.	–	50	80	ns
GATE2B Fall Time	Measure GATE2B Rise Time from 10% to 90%. C_{LOAD} = 50 pF.	–	15	30	ns

PACKAGE PIN DESCRIPTION

PACKAGE PIN # SSOP−24	PIN SYMBOL	FUNCTION
1	UVSD	Undervoltage shutdown lead. Typically this lead is connected through a resistor divider to the main high voltage (V_{IN}) line. If the voltage on this lead is less than 5.0 V then a fault is initiated such that GATE1, GATE2 and GATE2B go low.
2	OVSD	Overvoltage shutdown lead. Typically this lead is connected through a resistor divider to the main high voltage (V_{IN}) line. If the voltage on this lead exceeds 5.0 V then a fault is initiated such that GATE1, GATE2 and GATE2B go low.
3	V_{5REF}	5.0 V reference output lead. Capable of 20 mA nominal output. If this lead falls to 4.5 V, a fault is initiated such that GATE1, GATE2 and GATE2B go low.
4	OAM	Auxiliary error amplifier minus input. This lead is compared to 1.2 V nominal on the auxiliary error amp plus lead and represents the V_{SS} voltage divided by ten.
5	OAOUT	Auxiliary error amplifier output lead. Source current 300 μA max.
6	OUVDELAY	Output undervoltage timing capacitor lead. If the controlled output voltages of either the main or the auxiliary supply are such that either V_{FB1} or V_{FB2} is greater that 4.1 V nominal, then capacitor from OUVDELAY to ground will begin charging. If the over voltage duration is such that the OUVDELAY voltage exceeds 5.0 V, then a fault will be initiated such that GATE1, GATE2 and GATE2B will go low.
7	I_{LIM1}	Pulse by pulse over current protection lead for the auxiliary PWM. A voltage exceeding 1.2 V nominal on I_{LIM1} will cause GATE1 to go low. A voltage exceeding 1.4 V nominal on I_{LIM1} will cause GATE1 to go low for at least two clock cycles.
8	RAMP1	Current Ramp Input Lead for the Auxiliary PWM. A voltage which is linear with respect to current in the primary side of the auxiliary transformer is usually represented on this lead. A voltage exceeding V_{FB1} − 0.13 on RAMP1 will cause GATE1 to go low.
9	V_{FB1}	Voltage Feedback Lead for the Auxiliary PWM. A voltage which represents the auxiliary power supply output voltage is fed to this lead. A voltage less than RAMP1+0.13 on V_{FB1} will cause GATE1 to go low.
10	V_{SS}	V_{SS} power/feedback input lead. See V_{CC} for description of power operation. In addition, this lead is fed to a divide by ten resistor divider and compared to 1.2 V nominal at the positive side of the error amplifier.
11	V_{CC}	V_{CC} power input lead. This input runs off a Zener referenced supply until $V_{SS} > V_{CC}$. Then an internal diode which runs between V_{SS} and V_{CC} turns on and all main power is derived from V_{SS}.
12	GATE1	Auxiliary PWM gate drive lead. This output normally drives the FET which drives the auxiliary transformer.
13	GND	Ground lead.
14	GATE2	Synchronous PWM gate drive lead. This output normally drives the FET which drives the main transformer.
15	GATE2B	Synchronous PWM gate drive lead. This output normally drives the FET for the gate drive transformer used for synchronous rectification.
16	V_{FB2}	Voltage feedback lead for the synchronous PWM. A voltage which represents the main power supply output voltage is fed to this lead. A voltage less than RAMP2+0.13 on V_{FB2} will cause GATE2 to go low and GATE2B to go high.
17	RAMP2	Current ramp input lead for the synchronous PWM. A voltage which is linear with respect to current in the primary side of the main transformer is usually represented on this lead. A voltage exceeding V_{FB2} − 0.13 on RAMP2 will cause GATE2 to go low and GATE2B to go high.
18	I_{LIM2}	Pulse by pulse over current protection lead for the synchronous PWM. A voltage exceeding 1.2V nominal on I_{LIM2} will cause GATE2 to go low and GATE2B to go high. A voltage exceeding 1.4 V nominal on I_{LIM2} will cause GATE2 to go low and GATE2B to go high for at least two clock cycles.
19	DLYSET	GATE2, GATE2B non−overlap time adjustment lead. A 27 kΩ resistor from DLYSET to ground sets the non−overlap time to 45 ns nominal.

PACKAGE PIN # SSOP–24	PIN SYMBOL	FUNCTION
20	FADJ	Frequency adjustment lead. A 27 kΩ resistor from FADJ to ground sets the clock frequency to 512 kHz nominal.
21	$SYNC_{OUT}$	Clock output lead. This is a 50% duty cycle, 1.0 V to 5.0 V pulse whose rising edge is in phase with GATE1. This signal can be used to synchronize other power supplies.
22	$SYNC_{IN}$	Clock synchronization lead. The internal clock frequency can be adjusted +10%, −15% by the onset of positive edges of an external clock occurring on the $SYNC_{IN}$ lead. If the external clock frequency is outside the internal clock frequency by +25%, −35% the external clock is ignored and the internal clock free runs.
23	PROGRAM	ENABLE programming input. See ENABLE for programming states. PROGRAM has at least 20 μA min. of available source current.
24	ENABLE	PWM enable input. If PROGRAM is HIGH then a LOW on ENABLE will allow GATE1, GATE2 and GATE2B to switch. If PROGRAM is LOW then a HIGH on ENABLE will allow GATE1, GATE2 and GATE2B to switch. If ENABLE is left floating, it will pull up to a HIGH level. ENABLE has at least 100 μA (min) of available source current.

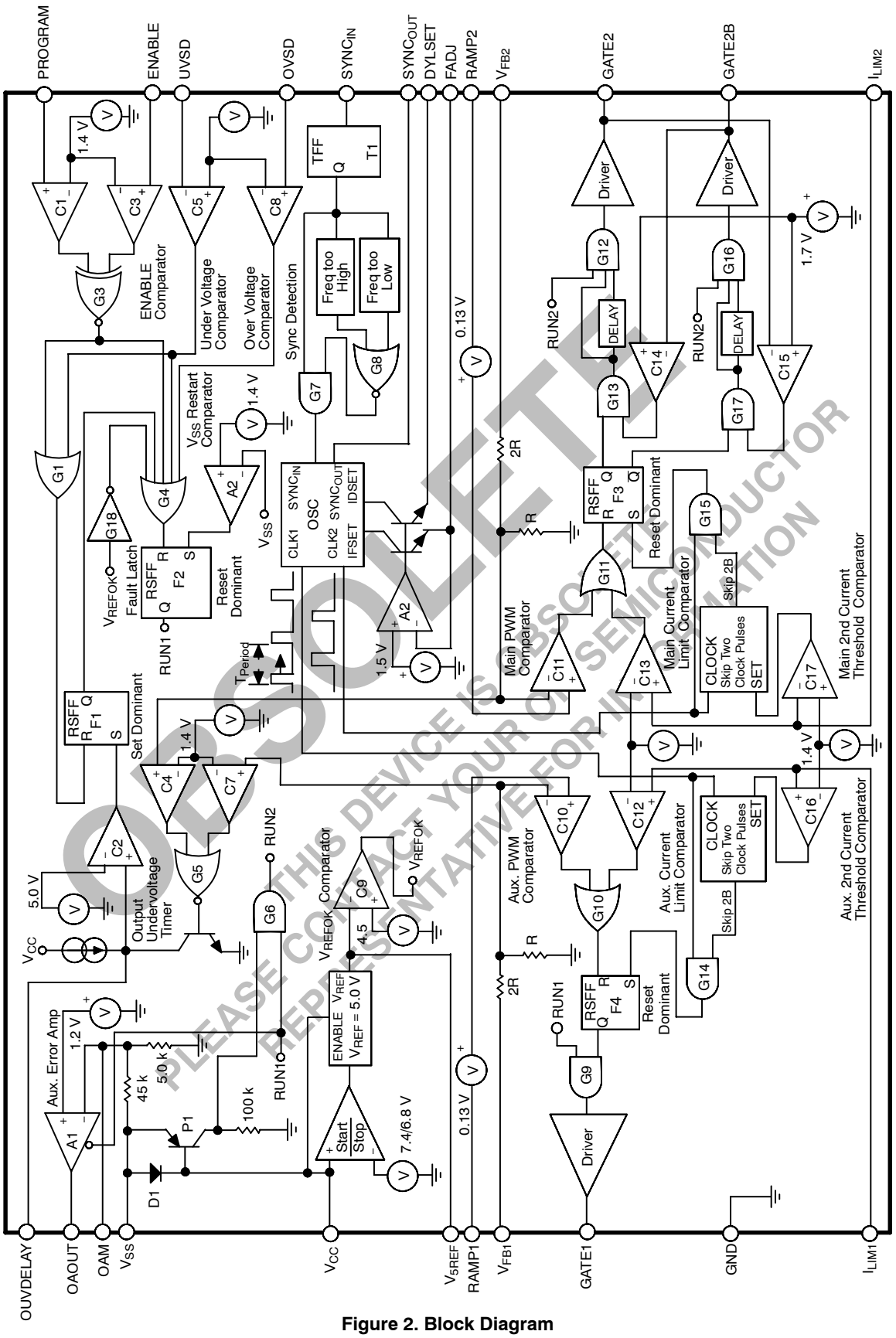


Figure 2. Block Diagram

THEORY OF APPLICATION

THEORY OF OPERATION

Powering the IC

The IC has one supply, V_{CC}, and one Ground lead. If V_{SS} is used for a bootstrapped supply the diode between V_{SS} and V_{CC} is forward biased, and the IC will derive its power from V_{SS}. The internal logic monitors the supply voltage, V_{CC}. During abnormal operating conditions, all GATE drivers are held in a low state. The CS5106 requires 1.5 mA nominal of startup current.

Startup

Assume the part is enabled and there are no over voltage or under voltage faults present. Also, assume that all auxiliary and main regulated output voltages start at 0 V. An 8.0 V, Zener referenced supply is typically applied to V_{CC}. When V_{CC} exceeds 7.5 V, the 5.0 V reference is enabled and the OSC begins switching. If the V_{5REF} lead is not excessively loaded such that V_{5REF} < 4.5 V nominal, 'V_{REF}OK' goes 'high' and 'RUN1' will go 'high', releasing GATE1 from its low state. After GATE1 is released, it begins switching according to conditions set by the auxiliary control loop and the auxiliary supply, V_{SS} begins to rise. When V_{SS} > V_{CC} + V(D1), P1 turns on and 'RUN2' goes 'high', releasing GATE2 and GATE2B from their low state. GATE2 and GATE2B begin switching according to conditions set by the main control loop and the main regulated output begins to rise. See startup waveforms in Figure 3.

Soft Start

Soft Start for the auxiliary power supply is accomplished by placing a capacitor between OAOUT and Ground. The error amplifier has 200 μA of nominal of source current and is ideal for setting up a Soft Start condition for the auxiliary regulator. Care should be taken to make sure that the Soft Start timing requirements are not in conflict with any transient load requirements for the auxiliary supply as large capacitors on OAOUT will slow down the loop response. Also, the Soft Start capacitor must be chosen such that during start or restart, both outputs will come into regulation before the OUVDELAY timer trips. Soft Start for the main supply is accomplished by charging Soft Start capacitor C6 through D5 and R7 at start up. After the main supply has come into regulation C6 continues to charge and is disconnected from the feedback loop by D8.

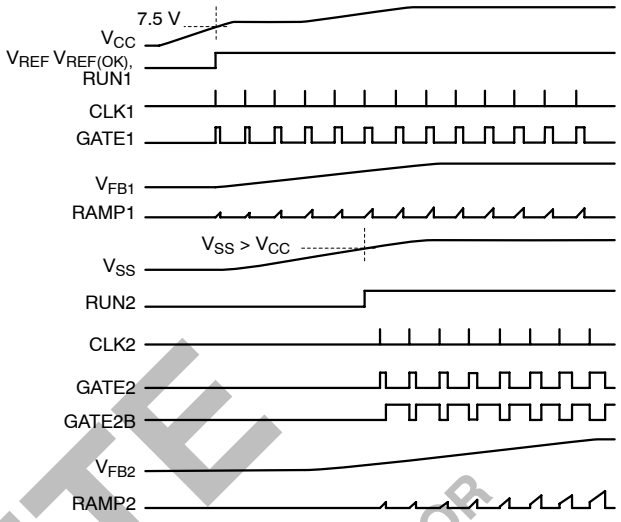


Figure 3. Startup Waveforms

Voltage and Current Ramp PWM Comparator Inputs ($V_{FB1,2}$ and RAMP1,2 leads)

C10 and C11 are the PWM comparators for the auxiliary and main supplies. The feedback voltage (V_{FB}) is divided by three and compared with a linear, voltage representation of the current in the primary side of the transformer (RAMP). When the output of the feedback comparator goes 'high', a reset signal is sent to the PWM flip−flop and the GATE driver is driven 'low'. A 130 mV offset on the RAMP leads allows the drivers to go to 0% duty cycle in the presence of light loads.

Feedback Voltage for GATE1 Driver (V_{FB1})

Typically the output of the auxiliary error amplifier (A1) is tied to V_{FB1}. The V_{SS} output is programmed to 12 V by a 10:1 resistive divider on the negative input of the error amplifier and a fixed 1.2 V reference on the positive input of the error amplifier.

Pulse by Pulse Over Current Protection and Hiccup Mode ($I_{LIM1,2}$ leads)

C12 and C13 are the pulse by pulse current limit comparators for the auxiliary and main supplies. When the current in the primary side of the transformer increases such that the voltage across the current sense resistor exceeds 1.2 V nominal, the output of the current limit comparator goes

'high' and a reset signal is sent to the PWM flip−flop and the GATE driver is driven 'low'.

C16 and C17 are the second threshold, pulse by pulse current limit comparators for the auxiliary and main supplies. If the current in the primary side of the transformer increases so quickly that the current sense voltage is not limited by C12 or C13 and the voltage across the current sense resistor exceeds 1.4 V, the second threshold comparator will trip a delay circuit and force the GATE driver stage to go low and stay low for the next two clock cycles.

Undervoltage and Overvoltage Thresholds

C5 and C8 are the undervoltage and overvoltage detection comparators. Typically, these inputs are tied across the middle resistor in a three resistor divider with the top resistor to V_{IN} and bottom resistor to Ground. The under voltage comparator has 200 mV of built in hysteresis with respect to a direct input on the UVSD lead. The under voltage comparator has its positive input referenced to 5.0 V while the over voltage comparator has its negative input referenced to 5.0 V. The output of both comparators are ORed at (G4) with the over current and enable inputs. The output of G4 feeds the input to the fault latch (F2).

PROGRAM and ENABLE Leads

The PROGRAM lead controls the polarity of the ENABLE lead. If the PROGRAM lead is 'high' or floating, the GATE outputs will go low if the ENABLE input is tied 'high' or floating. If the PROGRAM lead is tied low, the GATE outputs will go low if the ENABLE input is tied 'low'. If the part is then enabled after switching the outputs low, the part will restart according to the procedure outlined in the "Startup" section.

FAULT Logic

If a V_{REF}, UVSD or OVSD fault occurs at any time, G4 resets the fault latch (F2). RUN1 goes low and all gate drivers cease switching and return to their 'low' state. When RUN1 goes low, the output of the auxiliary op−amp (A1) discharges the Soft Start capacitor and holds it low while RUN1 is low. If the fault condition is removed before the OUVDELAY timer is tripped, the IC will restart the power supplies when V_{SS} < 1.4 V. If the OUVDELAY timer trips, the power supply must be restarted as explained in the following section.

Output Undervoltage Delay Timer for the Main and Auxiliary Regulated Outputs

C7 and C4 are the output under voltage monitor comparators for the auxiliary and main supplies. If a regulated output drops such that its associated V_{FB} voltage exceeds 4.1 V, the output undervoltage monitor comparator goes 'high' and the OUVDELAY capacitor begins charging from 0 V. A timing relation is set up by a 10 μA nominal current source, the OUVDELAY capacitor and a 5.0 V fault threshold at the input of C2 (see Figure 4). If any regulated output drops and stays low for the entire charge time of the OUVDELAY capacitor, a fault is triggered and all GATE drivers will go into a low state.

Once this fault is triggered, the IC will restart the power supplies only if the OUVDELAY fault is reset and ENABLE or UVSD is toggled while V_{SS} < 1.4 V. To reset the OUVDELAY fault, both the V_{FB} inputs must be less than 4.1 V. In the application circuit shown, V_{FB1} is brought low by OAOUT when RUN1 stops the oscillators. V_{FB2} is brought low when V_{AUXP} bleeds down and the V_{FB2} opto−isolator is no longer powered.

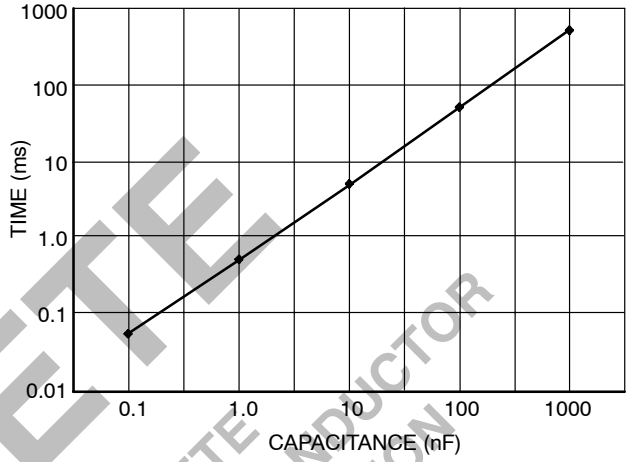


Figure 4. OUVDELAY Time vs. OUVDELAY Capacitance

FADJ and DLYSET Leads

Amplifier A2 and transistor N3 create a current source follower whose output is FADJ. An external resistor from FADJ to ground completes the loop. The voltage across the resistor is set by a buffered, trimmed, precision reference. In this fashion, an accurate current is created which is used to charge and discharge an internal capacitor thereby creating an oscillator with a tight frequency tolerance. For FADJ resistor value selection, see Figure 5. Transistor N2 is in parallel with N3 and is used to created an independent current across the resistor from DLYSET to ground. This current is used to program the GATE non−overlap delay blocks in the main PWM drivers. For DLYSET resistor value selection, see Figure 6.

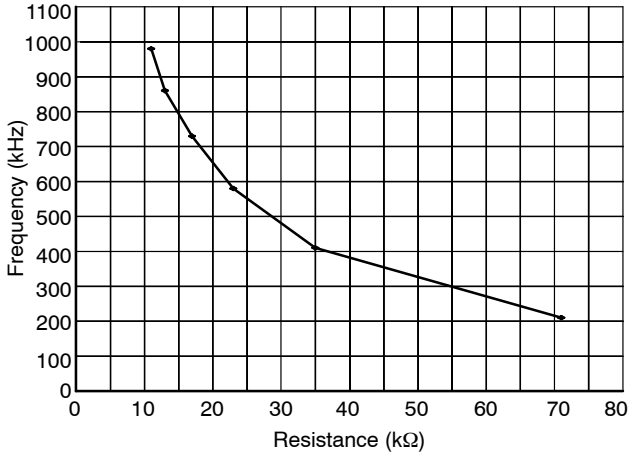


Figure 5. $SYNC_{OUT}$ Frequency vs. FADJ Resistors

Figure 6. GATE Non−Overlap Time vs. DLYSET Resistance

Oscillator

The oscillator generates two clock signals which are 180 degrees out of phase with respect to time. One clock signal feeds the main driver and the other feeds the auxiliary driver. Because the drivers are never turned on at the same time, ground noise and supply noise is minimized. The clock signals are actually 100 ns pulse spikes. These spikes create a narrow driver turn−on window. This narrow window prevents the driver from spurious turn on in the middle of a clock cycle. The oscillator can be synchronized by an external clock (slave) or drive the clocks of other controllers (master). See Figure 7 for the relationship between SYNC, CLK, and GATE waveforms.

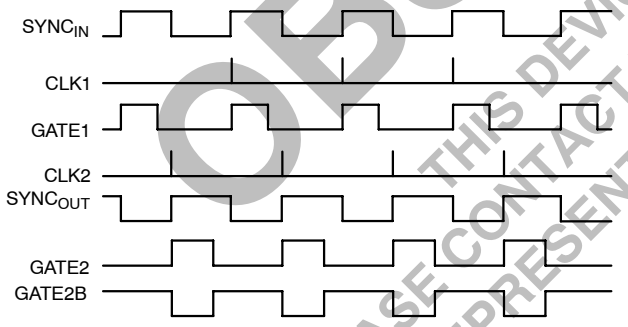


Figure 7. SYNC, GATE and CLOCK Waveforms

$SYNC_{IN}$ and $SYNC_{OUT}$ Leads

Multiple supplies can be synchronized to one supply by using the SYNC leads. The $SYNC_{IN}$ and $SYNC_{OUT}$ pulses are always 180 degrees out of phase. The $SYNC_{IN}$ input is always in phase with the clock signal for the main driver and the $SYNC_{OUT}$ output is always in phase with the clock signal for the auxiliary driver. If the IC is being used as a slave, the incoming frequency must be within +10%, −20% of the programmed frequency set by its own FADJ resistor. If the frequency on the $SYNC_{IN}$ lead is outside the internal frequency by +25%, −35%, the $SYNC_{IN}$ input will be ignored. If the SYNC signal stops while the power supplies are in synchronized operation, the synchronized supplies will stop and restart free running. If the $SYNC_{IN}$ signal drifts out of frequency specification while the power supplies are in synchronized operation, the synchronized supplies will begin to free run without restarting.

Slope Compensation

DC−DC converters with current mode control require slope compensation to avoid instability at duty cycles greater than 50%. A slope is added to the current sense waveform (or subtracted from the voltage waveform) that is equal to a percentage (75% typical) of the down slope of the inductor current. In the application diagram shown, the bootstrap (flyback) transformer inductance can be chosen so that the duty cycle never exceeds 50% and therefore does not require slope compensation. The buck indicator in the forward converter would typically be chosen to work in continuous conduction mode with a maximum duty cycle of 50−60% and would require slope compensation. Slope compensation is accomplished as follows: R9 and C9 form a ramp waveform rising each time GATE 2 turns on. C9 is discharged through D3 to the same level each cycle regardless of duty cycle. R10 and R11 are chosen to control the amount of slope compensation. C10 provides filtering for noise and turn−on spikes. To calculate the required slope compensation, calculate the buck indicator down current and the corresponding voltage slope at the current sense resistor − R12.

The buck inductor down slope is:

$$\text{Inductor\_Slope} = \frac{V_{OUT} + V_{Q5}}{L1(\mu H)}\left(\frac{A}{\mu s}\right)$$

The equivalent down slope at the current sense resistor for this application circuit is:

$$\text{Slope @ R12} = \text{Inductor\_Slope} \times \frac{NS_{T2}}{NP_{T2}} \times \frac{NP_{T3}}{NS_{T3}} \times R12\left(\frac{V}{\mu s}\right)$$

After choosing R9 and C9 to generate a ramp with a time constant of about 5 times the oscillator period, R10 and R11 can be chosen for the voltage at RAMP2 to be 1.75 of the voltage across R12.

Synchronous Rectification

Synchronous rectification was chosen to reduce losses in the forward converter. Improvements in efficiency will be most significant in low voltage, medium and high current converters where improvement in conduction loss offsets any added losses for gate drive.

In the application circuit Q4 is turned on and off by the forward transformer. Q5 is turned on and off through pulse transformer T4 and the gate driver formed by Q6 and Q7. Because Q4 and Q5 are driven through different types of components, differences in propagation delay must be considered. The DLYSET resistor should be chosen to avoid shoot−through or excessive off time.

Gate Drive Capability

All GATE drive outputs have nominal peak currents of 0.5A. See Figures 8 and 9 for typical rise and fall times.

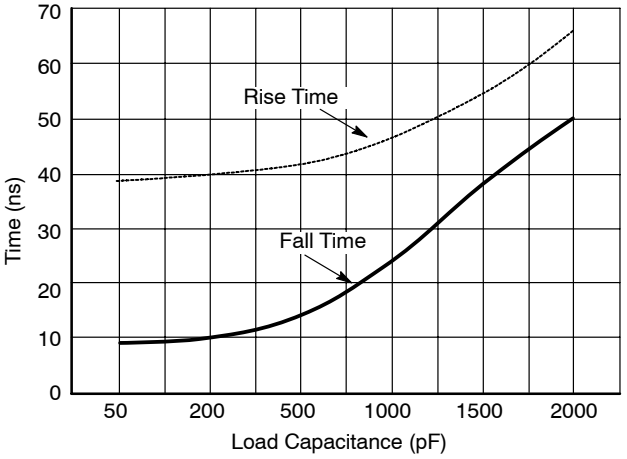


Figure 8. Typical GATE2, 2B Switching Times

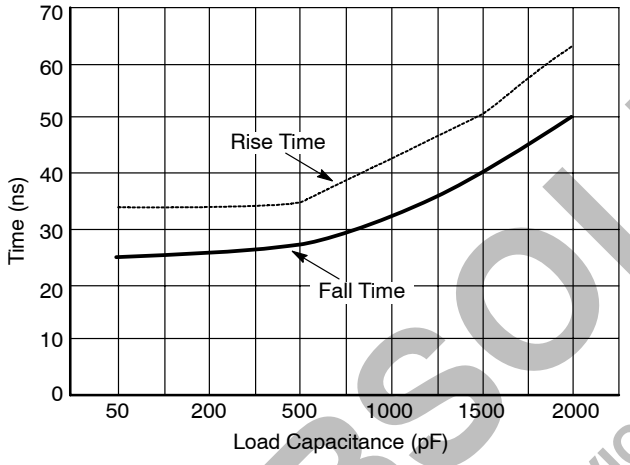


Figure 9. Typical GATE1 Switching Times

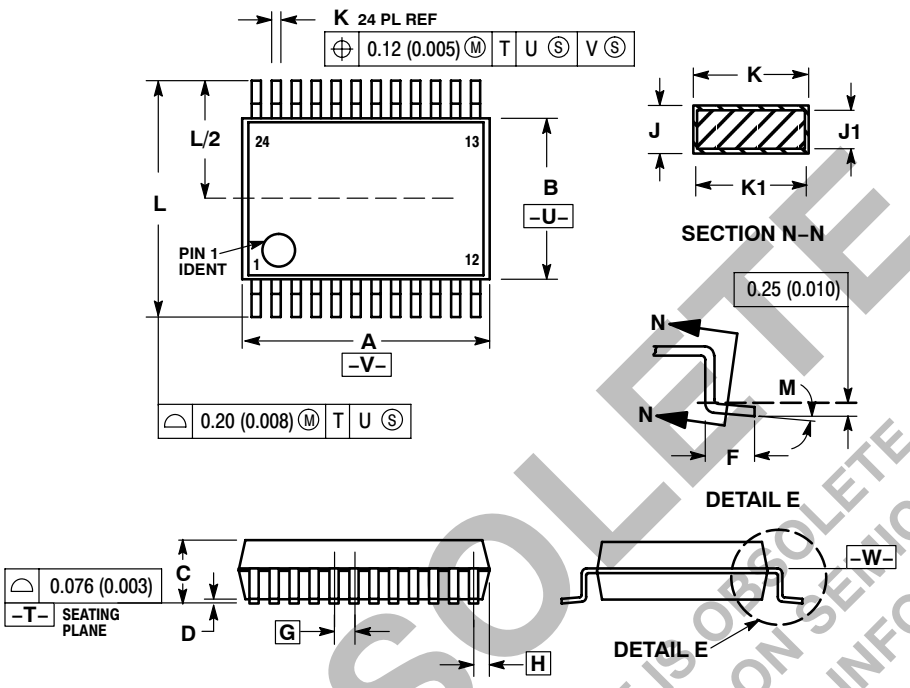
Design Considerations

The circuit board should utilize high frequency layout techniques to avoid pulse width jitter and false triggering of high impedance inputs. Ground plane(s) should be employed. Signal grounds and power grounds should be run separately. Portions of the circuit with high slew rates or current pulses should be segregated from sensitive areas. Shields and decoupling capacitors should be used as required.

Special care should be taken to prevent coupling between the SYNC leads and the surrounding leads. Depending on the circuit board layout and component values, decoupling capacitors or reduction in resistor values might be required to reduce noise pick−up on the FADJ and DLYSET resistors. Decoupling capacitors or active pull−up/down might be required to prevent false triggering of the ENABLE and PROGRAM leads.

PACKAGE DIMENSIONS

SSOP−24
SW SUFFIX
CASE 940D−03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.07	8.33	0.317	0.328
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.024
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

PACKAGE THERMAL DATA

Parameter		SSOP−24	Unit
$R_{\Theta JC}$	Typical	23	°C/W
$R_{\Theta JA}$	Typical	117	°C/W

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative