



AKD4497-SA

AK4497 Evaluation Board Rev.0

1. General Description

The AKD4497-SA is an evaluation board for the AK4497 (Premium 32-bit 2ch DAC) that supports Network-Audios, USB-DAC, Car-Audio Systems. It integrates differential output low pass filters, allowing quick evaluation with digital audio interface.

■ **Ordering Guide**

AKD4497-SA -- Evaluation Board for the AK4497
 (A USB I/F board for IBM-AT compatible computers and control software are included in this package.)

2. Function

- 10-pin Header for Serial Control
- Low Pass Filters (LPF) for Pre-amplifier Outputs
- Digital Audio Interface (AK4118A)

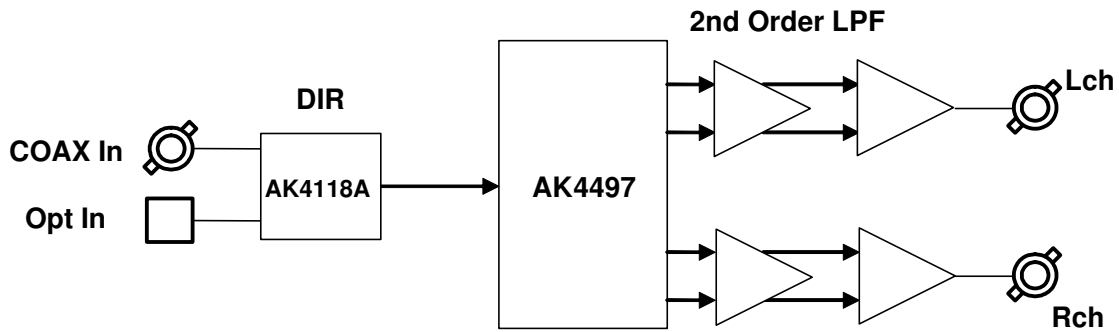


Figure 1. AKD4497-SA Block Diagram (Note 1)

Note 1. Circuit schematics are attached at the end of this document.

3. Board Appearance

■ Appearance Diagram

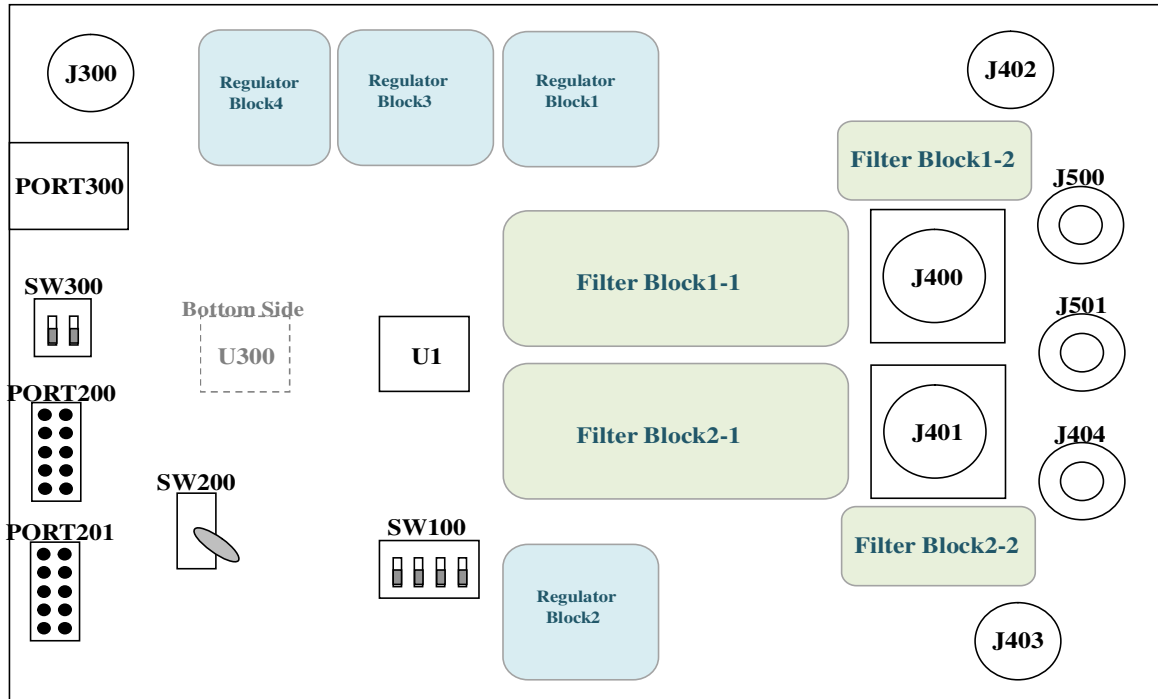


Figure 2. AKD4497-SA Outline View

■ Description

- (1) Connectors for Power Supply and GND (J500 / +15V, J404 / -15V, J501 / GND)
Connectors for power supply and the ground
Refer to the “Power Supply Connections” for details.
- (2) SPDIF Input Connectors (J300 / BNC Connector, PORT300 / Optical Connector)
Input a SPDIF signal to the AK4118A.
Set the R303 resistance to short when using the J300 (BNC Connector) jack.
Set the R302 resistance to short when using the PORT300 (Optical Connector).
- (3) Analog Differential Output Terminals (J400 / J401, XLR Connector)
Differential Analog Output Connector
- (4) Analog Output Terminals (J402 / J403, BNC Connector)
Single-ended Analog Output Connector

(5) EXT PORT (PORT200)

10-pin Header for External Interfacing

External digital audio devices are interfaced to this port.

Set the R202, R204, R206 and R208 resistances to short when using the PORT200 (EXT).

Pin	I/O	Function	pin	I/O	Function
1	I	MCLK	10	P	GND
2	I	BICK	9	P	GND
3	I	SDTO	8	P	GND
4	I	LRCK	7	P	GND
5	I	WCK	6	P	GND

Table 1. PORT200 (EXT) Pin Assignments

(6) AK4118A (U300)

The AK4118A is a digital audio transceiver.

It is used when evaluating sound quality of the AK4497 by SPDIF signals.

(7) μ P-IF PORT (PORT201)

10-pin Header for the USB I/F board

Connect the USB I/F board for IBM-AT compatible computers to this port for a connection to a USB port of a PC. Refer to the "Serial Control Mode" for details

(8) Dip Switches (SW100 / SW300)

Setting Switches for the AK4497 and the AK4118A.

Upside is "H" (ON) and Downside is "L" (OFF).

Refer to "■ Resistance and DIP Switch Settings" for details.

(9) SW200 (Toggle switch)

Toggle type-switch PDN for AK4497 and the AK4118A.

"H" : PDN = High

"L" : PDN = Low

4. Operation Sequence

■ **Operation sequence**

- 1). Power Supply Connections
- 2). Evaluation Mode
- 3). ■ Resistance and DIP Switch Settings
- 4). Power-up

■ **Power Supply Connections**

Name	Color	Voltage	Content	Note	Default Setting
J500 (REG(+15V))	Red	+10 to +15V	MVDD (AK4497), Op-Amp	This jack is always needed.	+15V
J404 (REG(-15V))	Blue	-10 to -15V	Op-Amp	This jack is always needed.	-15V
J501 (AVSS)	Black	0V	Ground	This jack is always needed.	0V

Table 2. Power Supply Connections

■ Evaluation Mode

(1) Evaluation with a DIR (COAX) < Default >

The J300 (COAX) jack is used in this mode. The DIR (AK4118A) generates MCLK, BICK, LRCK and SDATA from the input data of the J300 (COAX) connector.

Set the R303 resistance to short, and set the R201 (MCLK), R203 (BICK), R207 (LRCK) and R205 (SDTO) resistances to short.

Resistance Settings with DIR:

COAX / OPT : R303 = short (COAX)
MCLK : R201 = short (DIR)
BICK : R203 = short (DIR)
LRCK : R207 = short (DIR)
SDTO : R205 = short (DIR)

(2) Evaluation with a DIR (OPTICAL)

The PORT300 (OPTICAL) is used in this mode. The DIR (AK4118A) generates MCLK, BICK, LRCK and SDATA from the input data of the PORT300 (OPTICAL) connector.

Set the R302 resistance to short, and set the R201 (MCLK), R203 (BICK), R207 (LRCK) and R205 (SDTO) jumper pins to "DIR".

Resistance Settings with DIR:

COAX / OPT : R302 = short (OPT)
MCLK : R201 = short (DIR)
BICK : R203 = short (DIR)
LRCK : R207 = short (DIR)
SDTO : R205 = short (DIR)

(3) In the case that all interface clocks including the master clock are input externally. (PORT200)

Input all interface clocks including the master clock to the PORT200 (DSP).

Set R202 (MCLK), R204 (BICK), R208 (LRCK) and R206 (SDTO) resistances to short.

Resistance Settings with External Clocks:

COAX / OPT : R303 = short (COAX) <default>
MCLK : R202 = short (EXT)
BICK : R204 = short (EXT)
LRCK : R208 = short (EXT)
SDTO : R206 = short (EXT)

■ Resistance and DIP Switch Settings

(1) Resistance Settings

[R201 / R202 (MCLK)]: MCLK pin input select

R201 short: MCLK signal is supplied from the DIR (AK4118A). < Default >

R202 short: MCLK signal is supplied from the PORT200.

[R203 / R204 (BICK)]: BICK pin input select

R203 short: BICK signal is supplied from the DIR (AK4118A). < Default >

R204 short: BICK signal is supplied from the PORT200.

[R205 / R206 (SDTO)]: SDATA pin input select

R205 short: SDATA signal is supplied from the DIR (AK4118A). < Default >

R206 short: SDATA signal is supplied from the PORT200.

[R207 / R208 (LRCK)]: LRCK pin input select

R207 short: LRCK signal is supplied from the DIR (AK4118A). < Default >

R208 short: LRCK signal is supplied from the PORT200.

[R303 / R302 (COAX / OPT)]: SPDIF signal for AK4118A

R303 short: SPDIF signal is supplied from the J300 (COAX) connector. < Default >

R302 short: SPDIF signal is supplied from the PORT300.

(2) DIP Switch Setting

Upside is ON (“H”), and Downside is OFF (“L”).

[SW300]: Setting of the AK4118A

No.	Name	ON (“H”)	OFF (“L”)	Default
1	OCKS1	Master Clock setting for AK4118A Refer to Table 5.		L
2	OCKS0			L

Table 3. SW300 Setting

[SW100]: Setting of the AK4497

No.	Name	ON (“H”)	OFF (“L”)	Default
1	SSLOW	Digital Filter Setting Refer to Table 6. (In Pararell Control Mode)		L
2	SD			H
3	SLOW			L
4	HLOAD /I2C	Heavy Load Mode	Normal Mode	L
		(In Pararell Control Mode)		
5	PSN	I2C-Bus Control Mode	3-wire Serial Control Mode	L
		PSN pin= “H” (Pararell Control Mode)	PSN pin= “L” Serial Control Mode)	
6	ACKS /CAD1	Auto Setting Mode	Manual Setting Mode	L
		(In Pararell Control Mode)		
		CAD1 pin= “H”	CAD1 pin= “L”	

Table 4. SW100 Setting

Mode	OCKS1	OCKS0	MCKO1	fs (max)
0	L	L	256fs	96 kHz
1	L	H	256fs	96 kHz
2	H	L	512fs	48 kHz
3	H	H	128fs	192 kHz

< Default >

Table 5. Master Clock Setting

SSLOW	SD	SLOW	Mode
L	L	L	Sharp roll-off filter
L	L	H	Slow roll-off filter
L	H	L	Short delay sharp roll-off filter
L	H	H	Short delay slow roll-off filter
H	L	L	Super Slow roll-off filter
H	L	H	Super Slow roll-off filter
H	H	L	Low dispersion Shot Delay filter
H	H	H	Reserved

< Default >

Table 6. Digital Filter Setting

■ Power-up

Upside is ON (“H”), and Downside is OFF (“L”).

[SW200] (PDN): DAC / DIR Reset control. It must be set to “H” during operation.

After power-up, the AKD4497-SA must be reset once.

To reset the AKD4497-SA, set the SW200 toggle switch to “L” and power down the AK4497 and the AK4118A. Then, release the power-down by setting back the SW200 to “H”.

■ Serial Control Mode (PSN pin = “L”)

When using this evaluation board in serial control mode, settings of the CAD1 pin and the CAD2 pin on the board must match the Chip Address settings of the control software.

- (1) 3-wire Serial Control Mode: (I2C pin= “L”)
- (2) I²C Bus Control Mode: (I2C pin= “H”)

The AKD4497-SA should be connected to a PC (IBM-AT compatible) via a USB control box (AKDUSBIF-B) included in this package. The USB control box is connected to a PC with a USB cable and the AKD4497-SA with a 10-pin flat cable. (Note 2, Note 3)

- Note 2. The AKD4497-SA accepts only one AKDUSBIF-B at one time. It does not operate if two or more AKDUSBIF-Bs are connected.
- Note 3. Connect the 10pin Flat Cable as the red line of the cable is connected to the 1 pin of the 10pin Header of the board.

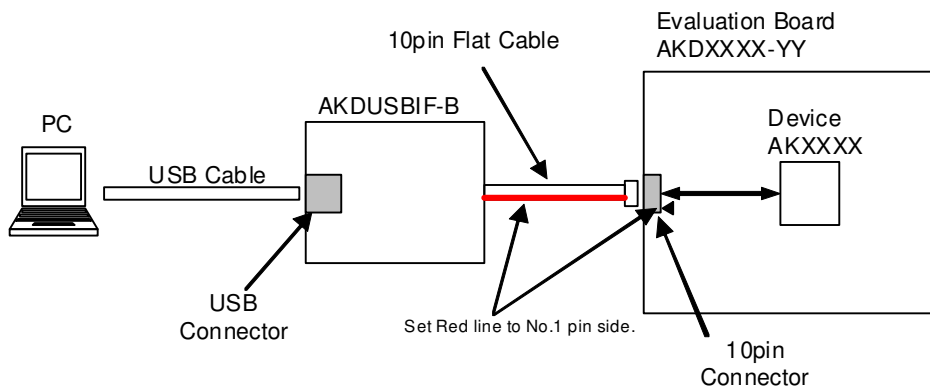


Figure 3. AKDUSBIF-B Connection

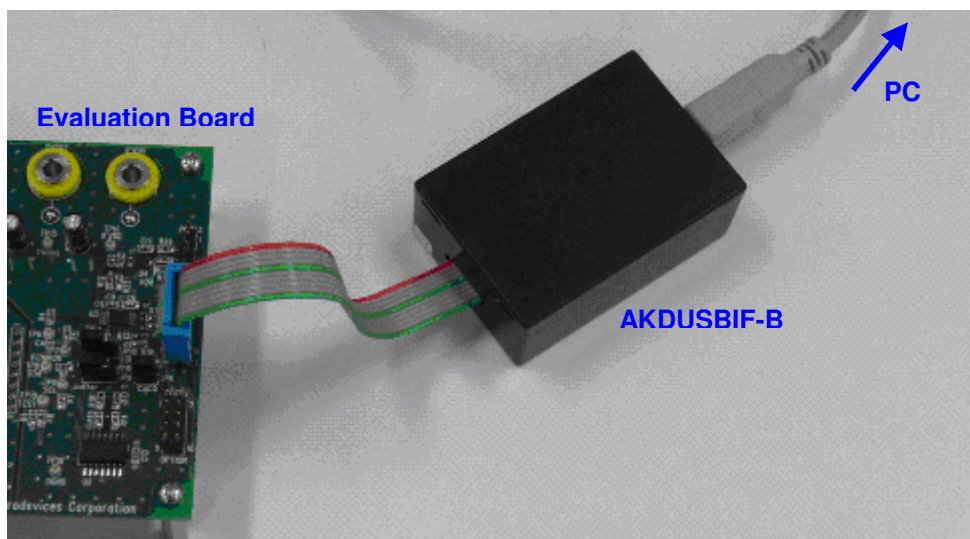


Figure 4. AKDUSBIF-B

5. Control Software Manual

■ Evaluation Board and Control Software Manual

1. Set up the evaluation board as needed, according to the previous terms.
2. Connect the evaluation board to a PC with USB cable.
3. USB control is recognized as HID (Human Interface Device) on PC. When it is not recognized properly, please reconnect the evaluation board to PC.
4. Insert the CD-ROM labeled “AKD4497-SA Evaluation Kit” into the CD-ROM drive.
5. Access the CD-ROM drive and double-click the icon “AKD4497-SA.exe” to open the control program.
6. Begin evaluation by following the procedure below.

[Supported OS]

Windows XP / Vista / 7 (32bit) (XP compatible mode is recommended for Vista / 7)
 64bit OS is not supported.

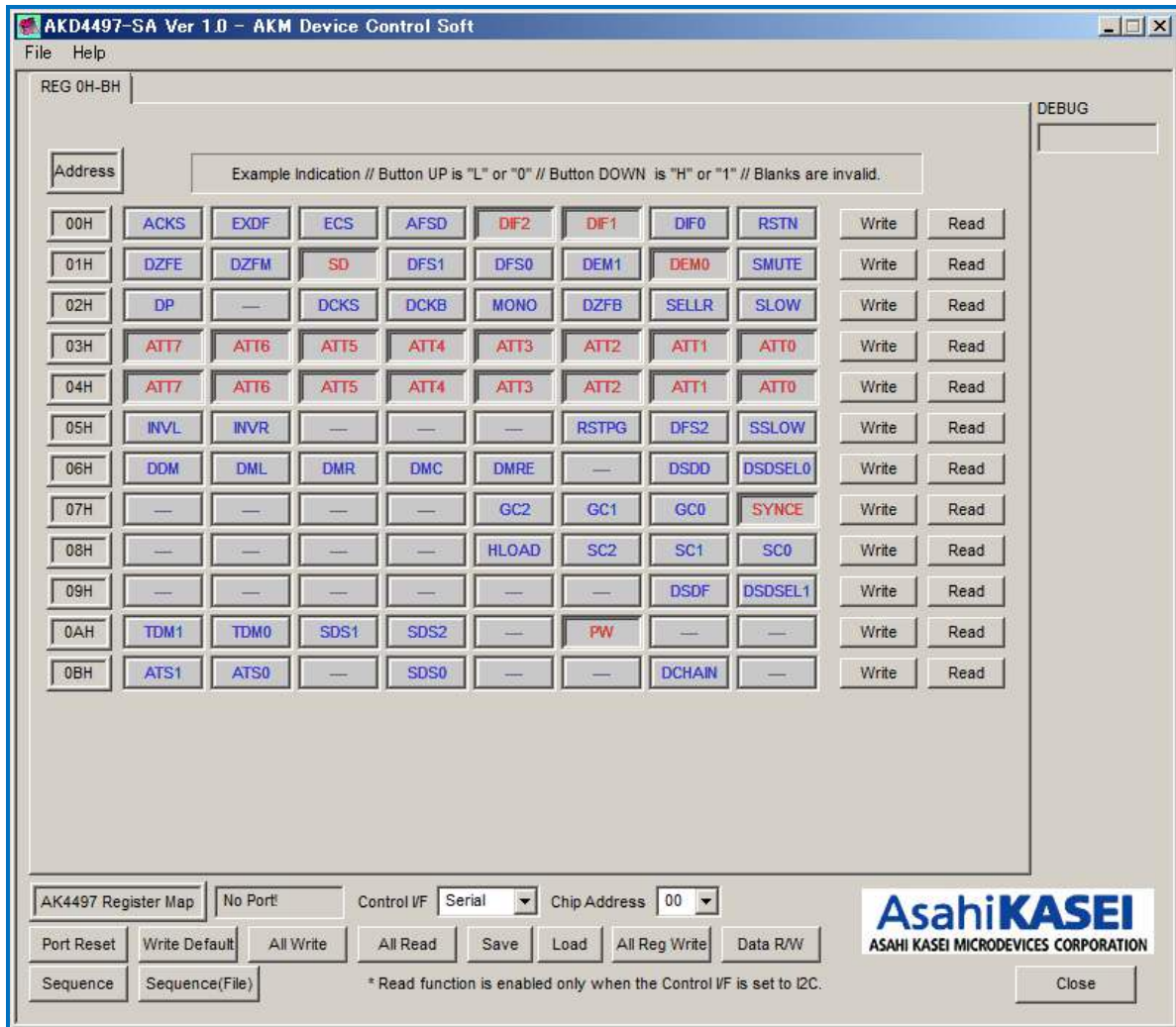


Figure 5. Control Program Window

■ Operation Overview

Register map is controlled by this control software.

Frequently used buttons, such as the register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Box” section for details of each dialog box setting.

- 1.[Port Reset]: Reset connection to PC
Click this button after the control software starts up and the evaluation board is connected to the PC via USB cable.
- 2.[Write Default]: Register Initialization
Use this button to initialize the registers when the device is reset by a hardware reset.
- 3.[All Write]: Execute write command for all registers displayed.
- 4.[All Read]: Execute read command for all registers displayed. (Note 2)
- 5.[Save]: Save current register settings to a file.
- 6.[Load]: Execute data write from a saved file.
- 7.[All Reg Write]: [All Reg Write] dialog box pops up.
- 8.[Data R/W]: [Data R/W] dialog box pops up.
- 9.[Sequence]: [Sequence] dialog box pops up.
- 10.[Sequence(File)]: [Sequence(File)] dialog box pops up.

Note 2. The [All Read] button is only valid when the interface mode for register control is in I²C bus control mode.

■ Tab Functions

1. [REG] Tab: Register Map

This tab is for register read and write.

Each bit on the register map is a push-button switch.

Button Down indicates “1” and the bit name is shown in red (when read-only the name is shown in dark red).

Button Up indicates “0” and the bit name is shown in blue (when read-only the name is shown in gray)

Grayed out registers are Read-Only registers. They cannot be controlled.

The registers which are not defined on the datasheet are indicated as “---”.

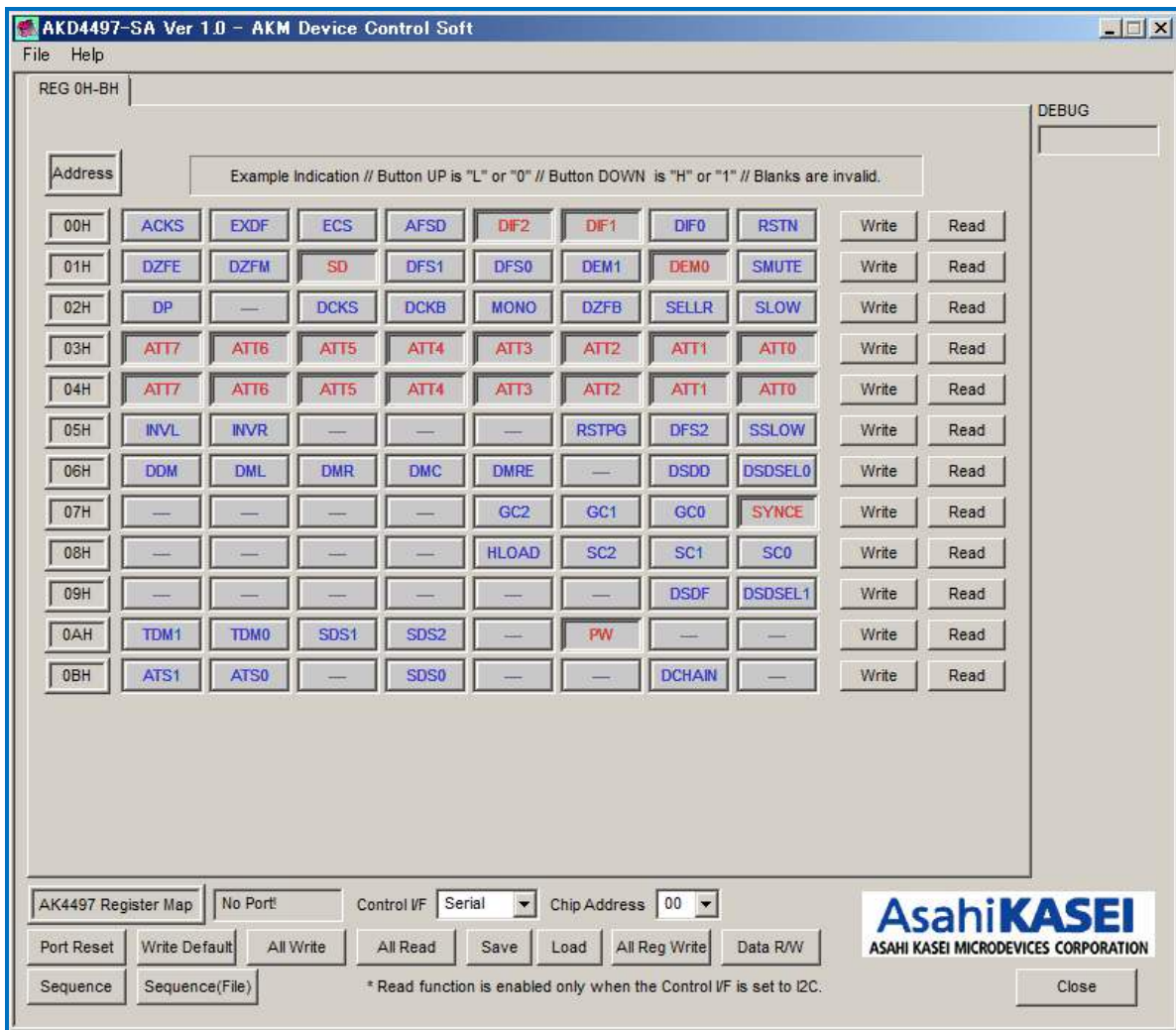


Figure 6. REG Window

[Write] button: Data Write Dialog

Select the [Write] button located on the right of the each corresponding address when changing two or more bits on the same address simultaneously.

Click the [Write] button for the register pop-up dialog box shown below.

When the checkbox next to the register is checked, the data will become “1”. When the checkbox is not checked, the data will become “0”. Click [OK] to write the set values to the registers, or click [Cancel] to cancel this setting.

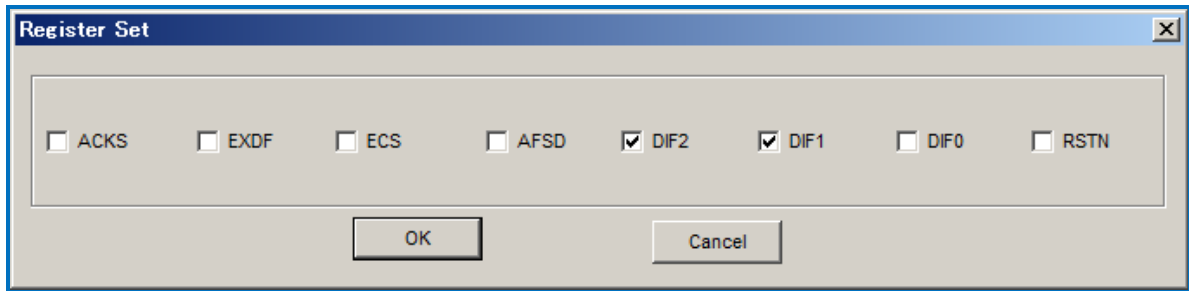


Figure 7. Register Set Window

[Read] button: Data Read (Only in I²C-bus Control Mode)

Click the [Read] button located on the right of the each corresponding address to execute a register read.

The current register value will be displayed in the register window as well as in the upper right hand DEBUG window.

Button Down indicates “1” and the bit name is shown in red (when read only the bit name is shown in dark red). Button Up indicates “0” and the bit name is shown in blue (when read only the bit name is shown in gray)

■ Dialog Box

1. [All Reg Write]: All Register Write dialog box

Click [All Reg Write] button in the main window to open register setting file window shown below.
Register setting files saved by [SAVE] button may be applied.

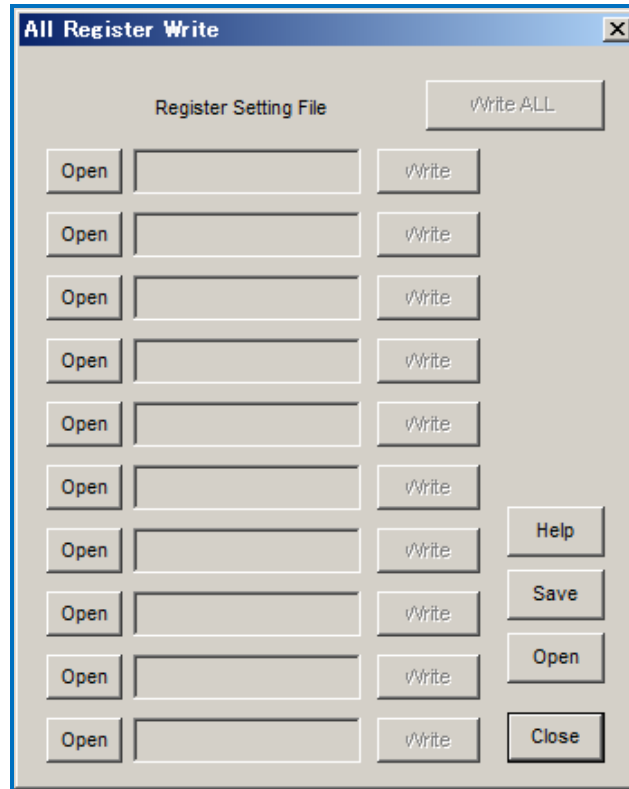


Figure 8. [All Reg Write] Window

[Open (left)]: Select a register setting file (*.akr).

[Write]: Execute register write with selected setting file.

[Write All]: Execute register write with all selected setting files.

Selected files are executed in descending order.

[Help]: Open help window.

[Save]: Save register setting file assignment. File name is “*.mar”.

[Open (right)]: Open saved register setting file assignment “*.mar”.

[Close]: Close dialog box and finish process.

~ Operating Suggestions ~

- Files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mar” should be stored in the same folder.
- When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data is written to the specified address.

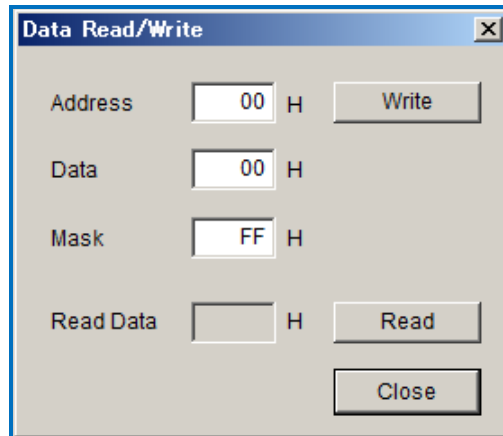


Figure 9. [Data R/W] Window

[Address] Box: Input data write address in hexadecimal numbers.

[Data] Box: Input write data in hexadecimal numbers.

[Mask] Box: Input mask data in hexadecimal numbers.

This value “ANDed” with the write data becomes the input data.

[Write]: Write data generated from Data and Mask value is written to the address specified in “Address” box.

(Note 3)

[Read]: Read data from the address specified in “Address” box. (Note 4)

[Close]: Close dialog box and finish process.

Data write will not be executed unless [Write] is clicked.

Note 3. The register map will be updated after executing the [Write] command.

Note 4. The [Read] button is only valid when the interface mode for register control is in I²C bus control mode.

3. [Sequence]: Sequence Dialog Box

Click the [Sequence] button in the main window for Sequence dialog box.
Register sequence may be set and executed.

Step	Address	Data	Mask	Interval	Select
1	00 H	00 H	FF H	0 ms	No_use
2	00	00	FF	0	No_use
3	00	00	FF	0	No_use
4	00	00	FF	0	No_use
5	00	00	FF	0	No_use
6	00	00	FF	0	No_use
7	00	00	FF	0	No_use
8	00	00	FF	0	No_use
9	00	00	FF	0	No_use
10	00	00	FF	0	No_use
11	00	00	FF	0	No_use
12	00	00	FF	0	No_use
13	00	00	FF	0	No_use
14	00	00	FF	0	No_use
15	00	00	FF	0	No_use
16	00 H	00 H	FF H	0 ms	No_use
17	00	00	FF	0	No_use
18	00	00	FF	0	No_use
19	00	00	FF	0	No_use
20	00	00	FF	0	No_use
21	00	00	FF	0	No_use
22	00	00	FF	0	No_use
23	00	00	FF	0	No_use
24	00	00	FF	0	No_use
25	00	00	FF	0	No_use

Start Step: 1

Buttons: Start, Help, Save, Open, Close

Figure 10. [Sequence] Window

~ Sequence Setting ~

Set register sequence according to the following process.

1. Select a command

Use [Select] pull-down box to choose commands.
Corresponding input boxes will be valid.

<Combo Box>

- No_use: Not using this address
- Register: Register write
- Reg(Mask): Register write (Masked)
- Interval: Take an interval
- Stop: Pause the sequence
- End: End the sequence

2. Input Sequence

[Address]: Data Address

[Data]: Write Data

[Mask]: Mask

This value “ANDed” with the write data becomes the input data.

When Mask = 0x00, current setting is hold.

When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.

When Mask = 0x0F, lower 4bit data which is set in the [Data] box is written.

Upper 4bit is hold to current setting.

[Interval]: Interval Time

Valid boxes for each process command are shown below.

- No_use : None
- Register : [Address], [Data], [Interval]
- Reg(Mask) : [Address], [Data], [Mask], [Interval]
- Interval : [Interval]
- Stop : None
- End : None

~ Control Buttons ~

Functions of Control Buttons are shown below.

[Start] button : Execute the sequence.

[Help] button : Open a help window.

[Save] button : Save sequence settings as a file. The file name is “*.aks”.

[Open] button : Open a sequence setting file “*.aks”.

[Close] button : Close the dialog box and finishes the process.

Stop Sequence

When “Stop” command is selected in the sequence, the process is paused at this step. It is resumed by clicking the [Start] button. The process starts from the step shown in [Start Step] box. This step number returns to “1” when the sequence is executed until the end. Input arbitrary step number to the [Start Step] box to start the process from the middle of sequence.

The process sequence can be restarted from the beginning by writing “1” to the [Start Step] box and click the [Start] button during the process.

4. [Sequence(File)]: Sequence(File) Dialog

Click the [Sequence(File)] button to open sequence setting file dialog box shown below.
Files saved in the “Sequence setting dialog” can be applied in this dialog.

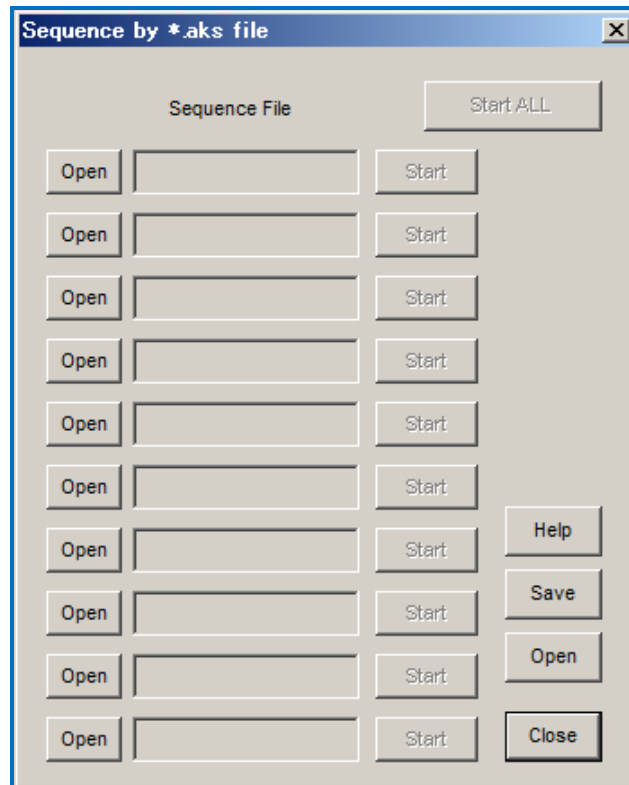


Figure 11. [Sequence (File)] Window

[Open (left)] button: Select a sequence setting file (*.aks)

[Start] button: Execute the sequence by the setting of selected file.

[Start All] button: Execute sequence with all selected setting files.

Selected files are executed in descending order.

[Help] button: Open help window.

[Save] button: Save register setting file assignment. File name is “*.mas”.

[Open (right)] button: Open saved sequence setting file assignment “*. mas”.

[Close] button: Close dialog box and finish process.

~ Operating Suggestions ~

1. Files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mas” should be stored in the same folder.
2. When “Stop” command is selected in the sequence, the process is paused at this step and a message shown below pops up. The sequence is resumed by clicking “OK” button.

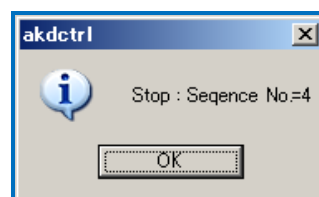


Figure 12. Sequence Pause Window

6. Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision APX 555 Audio Analyzer
- MCLK : 256fs (44.1 kHz), 256fs (96 kHz), 128fs (192 kHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V
- Pass : DIR → AK4497 → Cannon Connector
- Interface : Internal DIR (44.1 kHz, 96 kHz, 192 kHz)
- Temperature : Room Temperature
- Operational Amplifiers : OPA1611, OPA1612
- Control Soft Register : HLOAD="1", SC2="1"

fs=44.1kHz

Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
S/(N+D)	1kHz, 0dB	20kHz LPF	116.9 dB	/	116.6 dB
DR	1kHz, -60dB		124.2 dB	/	124.1 dB
		A-weighted	126.5 dB	/	126.3 dB
S/N	"0" data	20kHz LPF	124.1 dB	/	124.1 dB
		A-weighted	126.5 dB	/	126.4 dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
S/(N+D)	1kHz, 0dB	40kHz LPF	114.1 dB	/	115.1 dB
DR	1kHz, -60dB		121.5 dB	/	121.5 dB
S/N	"0" data	40kHz LPF	121.6 dB	/	121.5 dB

fs=192kHz

Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
S/(N+D)	1kHz, 0dB	40kHz LPF	115.3 dB	/	114.6 dB
DR	1kHz, -60dB		121.5 dB	/	121.3 dB
S/N	"0" data	40kHz LPF	121.5 dB	/	121.6 dB

■ Capacitance between the VREFH pin and the VREFL pin

Distortion (THD+N) can be improved by increasing the capacitance of a capacitor between the VREFH pin and the VREFL pin. Applicable capacitors are C108 and C111 in the circuit schematic.

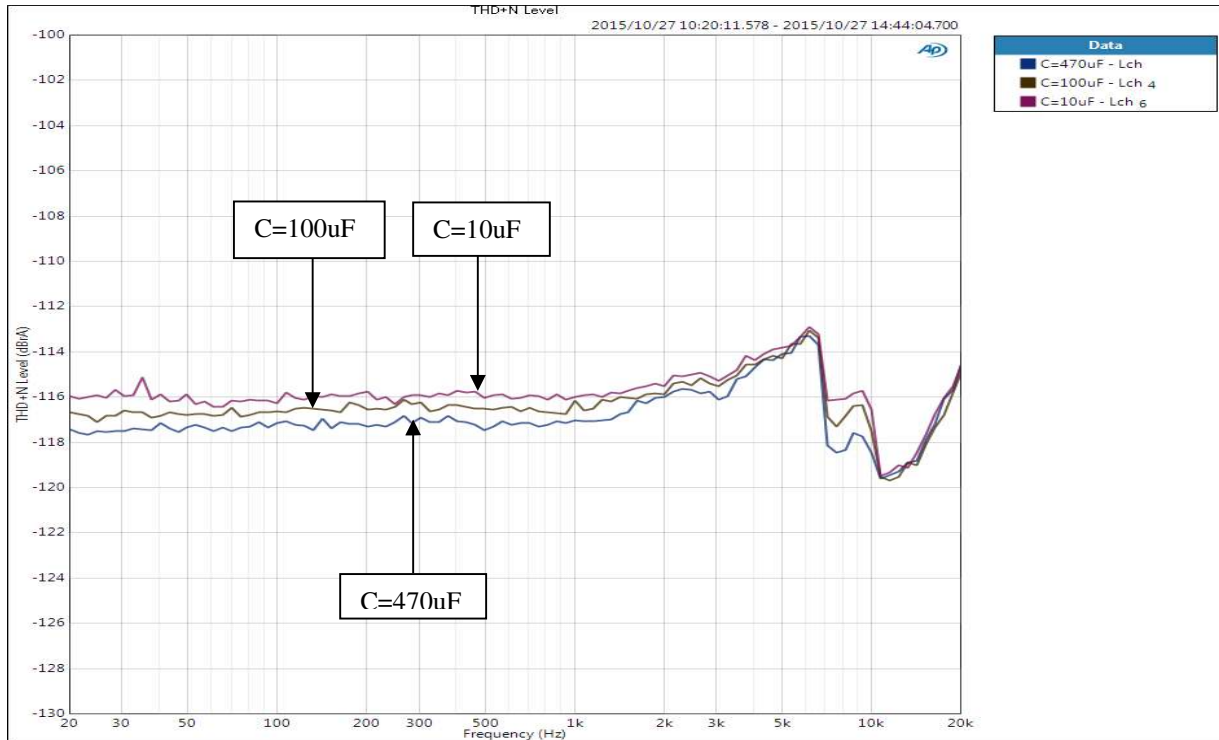


Figure 13. THD+N vs. Input Frequency Comparison by Capacitance

[Plots]

fs = 44.1 kHz

AK4497 THD+N vs. Input Level
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

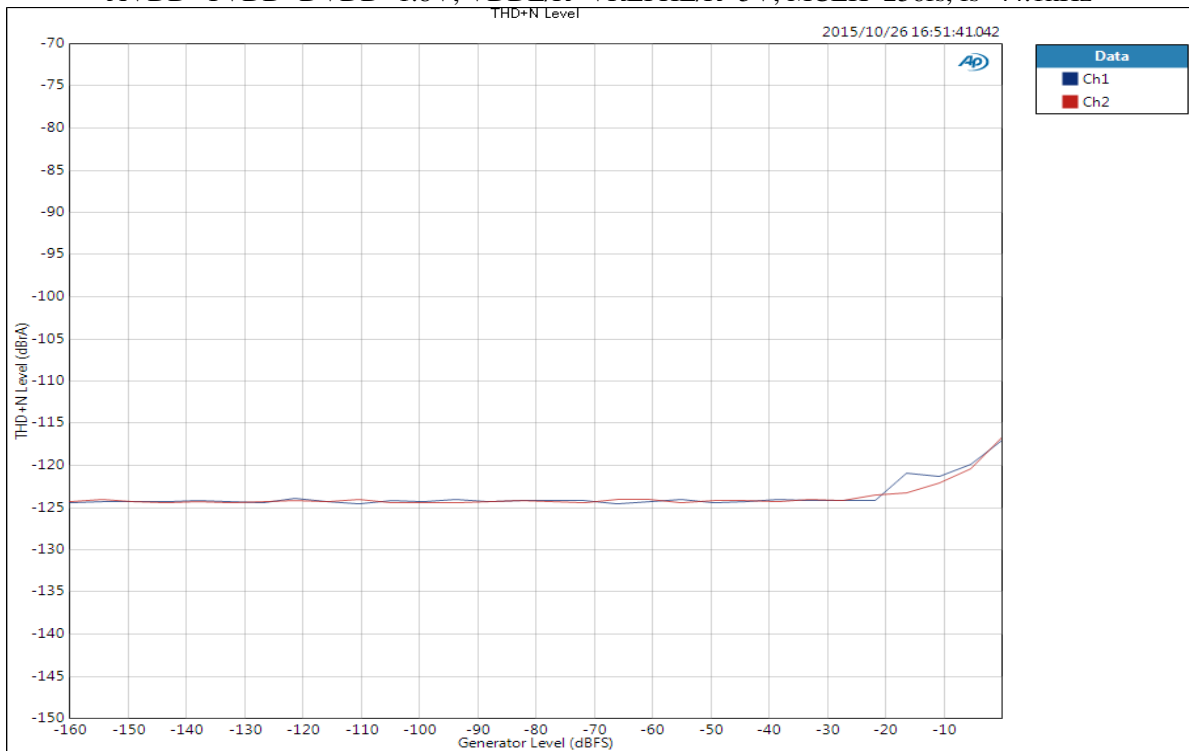


Figure 14. THD+N vs. Input Level

AK4497 THD+N vs. Input Frequency
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

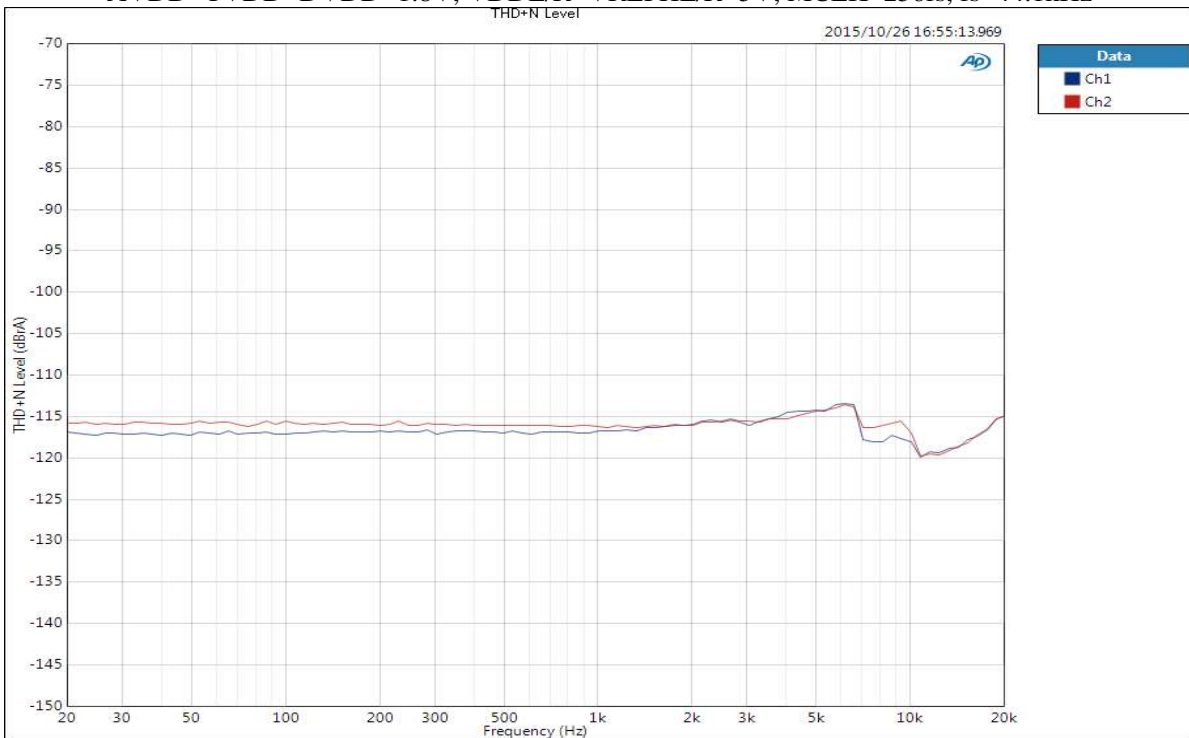


Figure 15. THD+N vs. Input Frequency

fs = 44.1 kHz

AK4497 Linearity

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

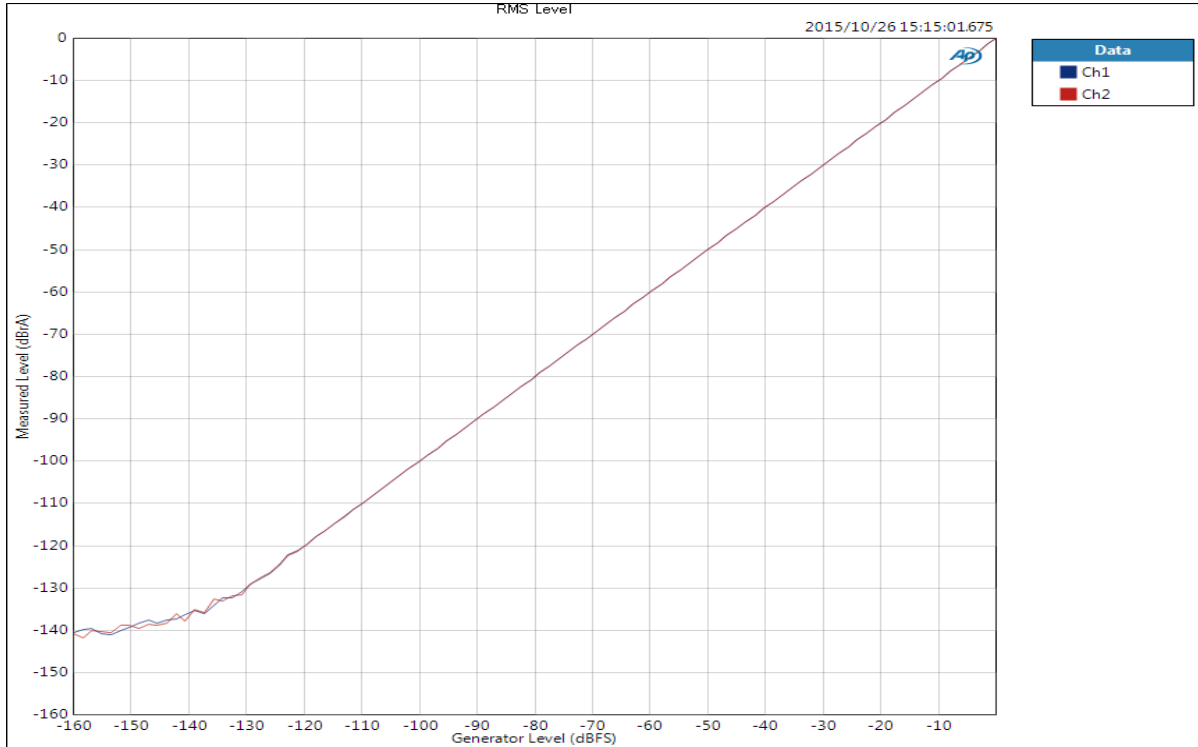


Figure 16. Linearity

AK4497 Frequency Response

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

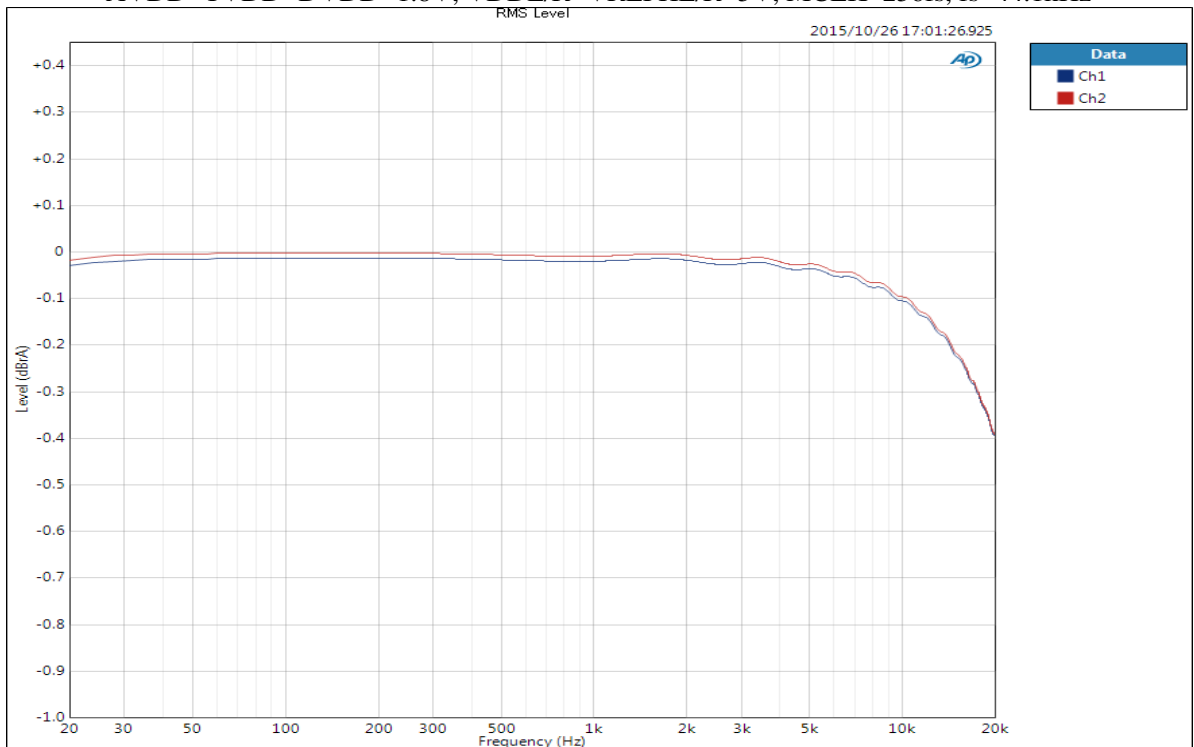


Figure 17. Frequency Response

fs = 44.1 kHz

AK4497 Crosstalk

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

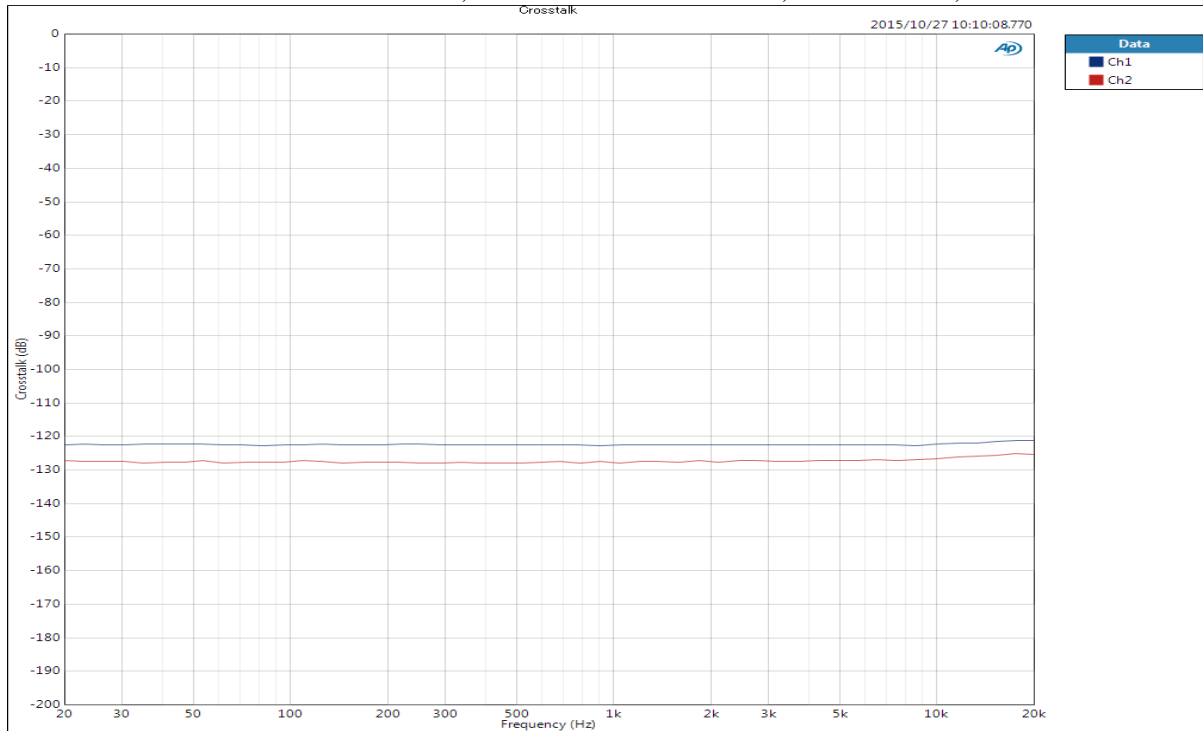


Figure 18. Crosstalk

AK4497 FFT (0dBFS Input)

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

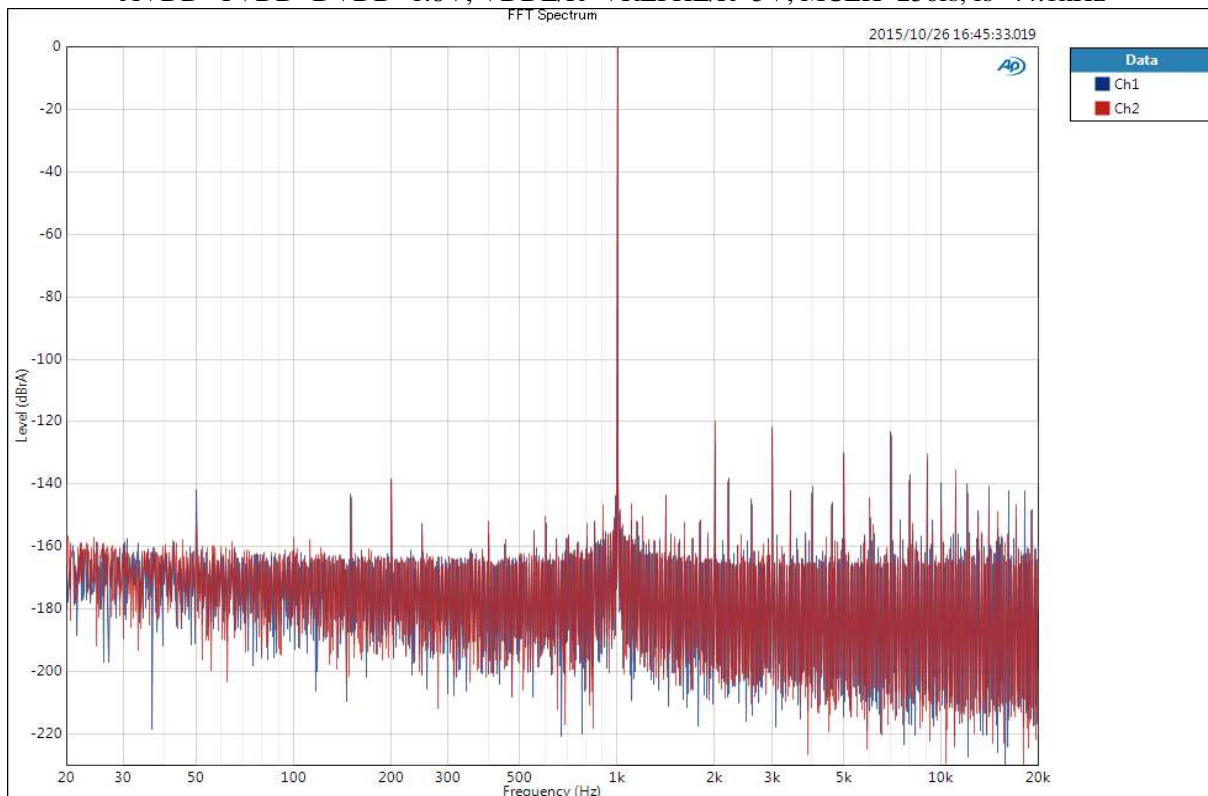


Figure 19. FFT (0dBFS Input)

fs = 44.1 kHz

AK4497 FFT (-60dBFS Input)
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

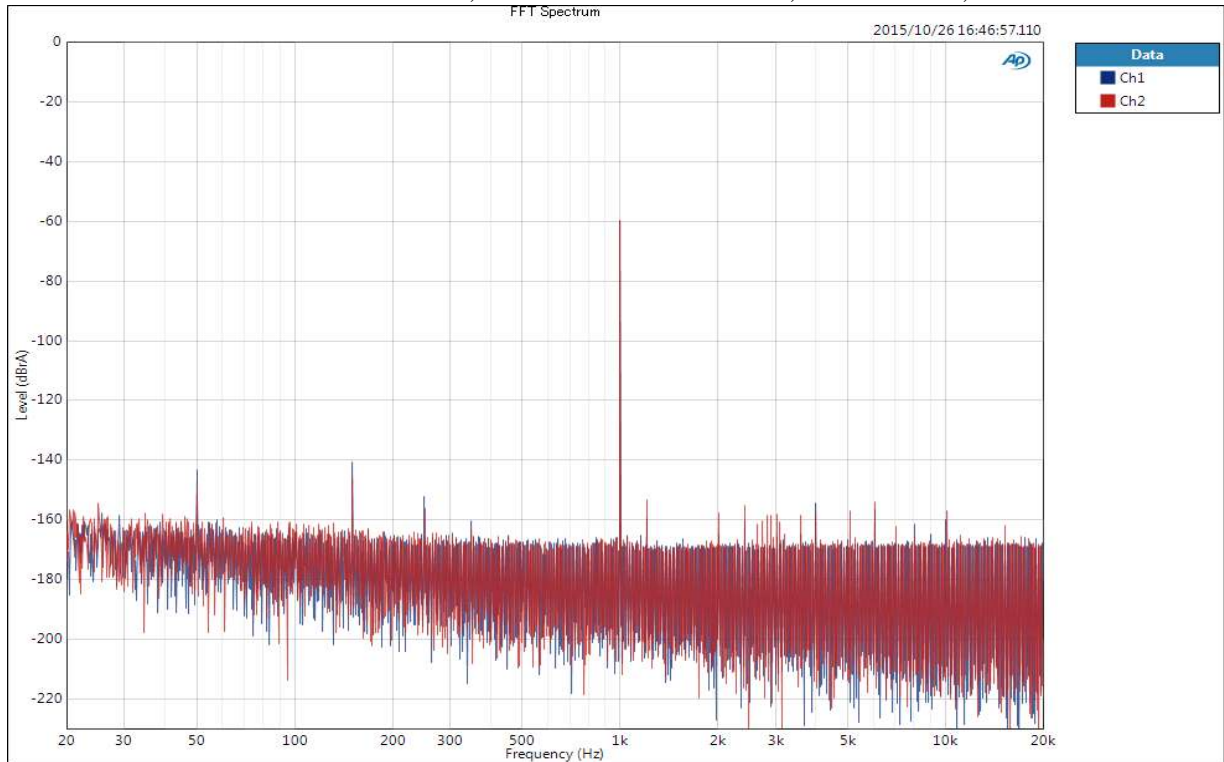


Figure 20. FFT (-60dBFS Input)

AK4497 FFT (No Signal Input)
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

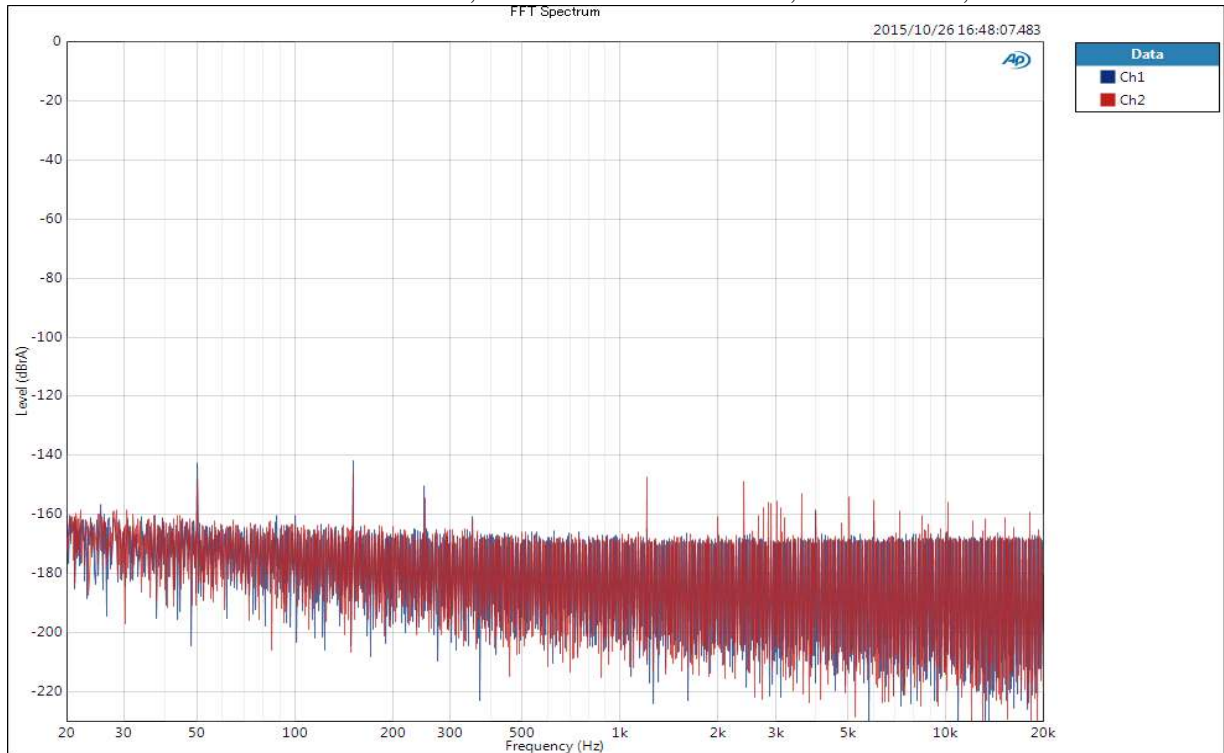


Figure 21. FFT (No Signal Input)

fs = 96 kHz

AK4497 THD+N vs. Input Level
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

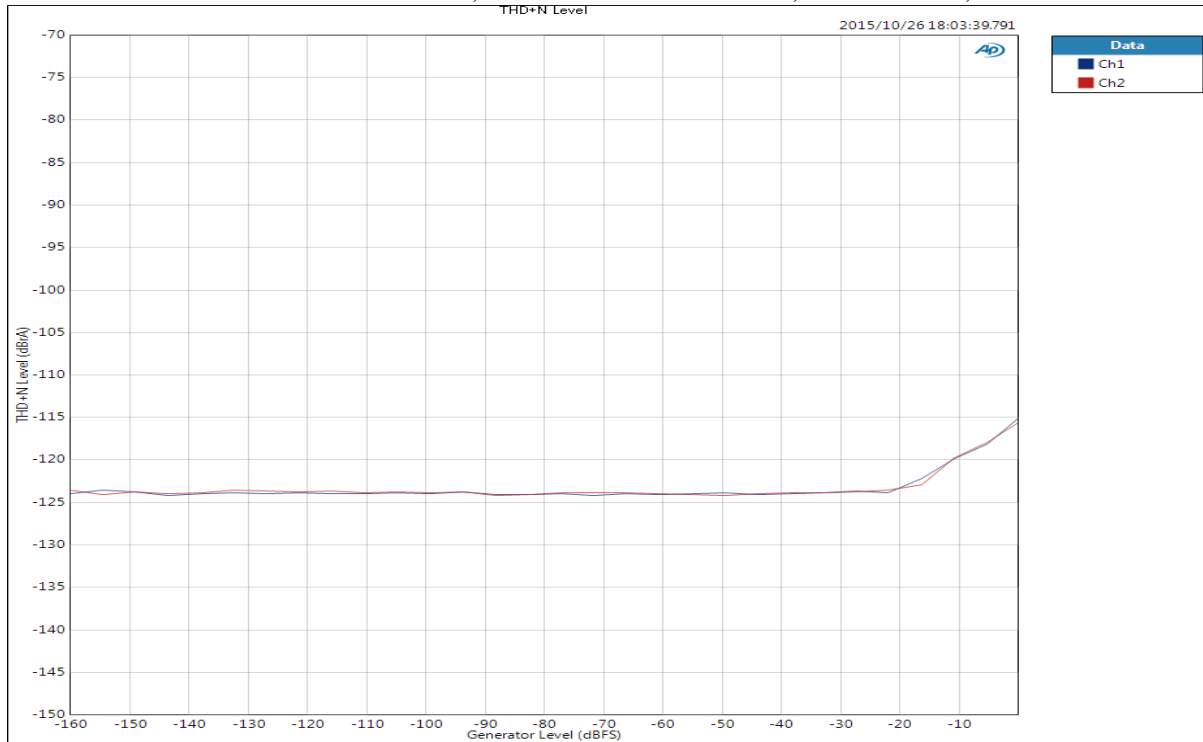


Figure 22. THD+N vs. Input Level

AK4497 THD+N vs. Input Frequency
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

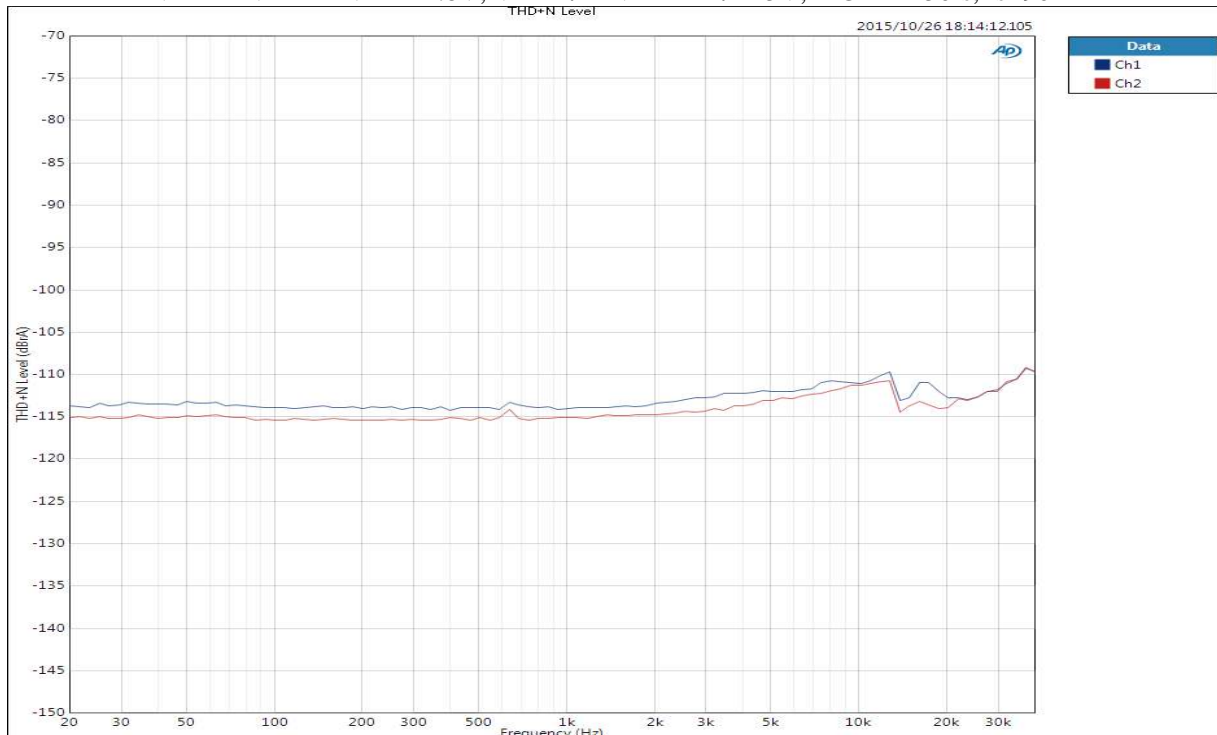


Figure 23. THD+N vs. Input Frequency

fs = 96 kHz

AK4497 Linearity

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

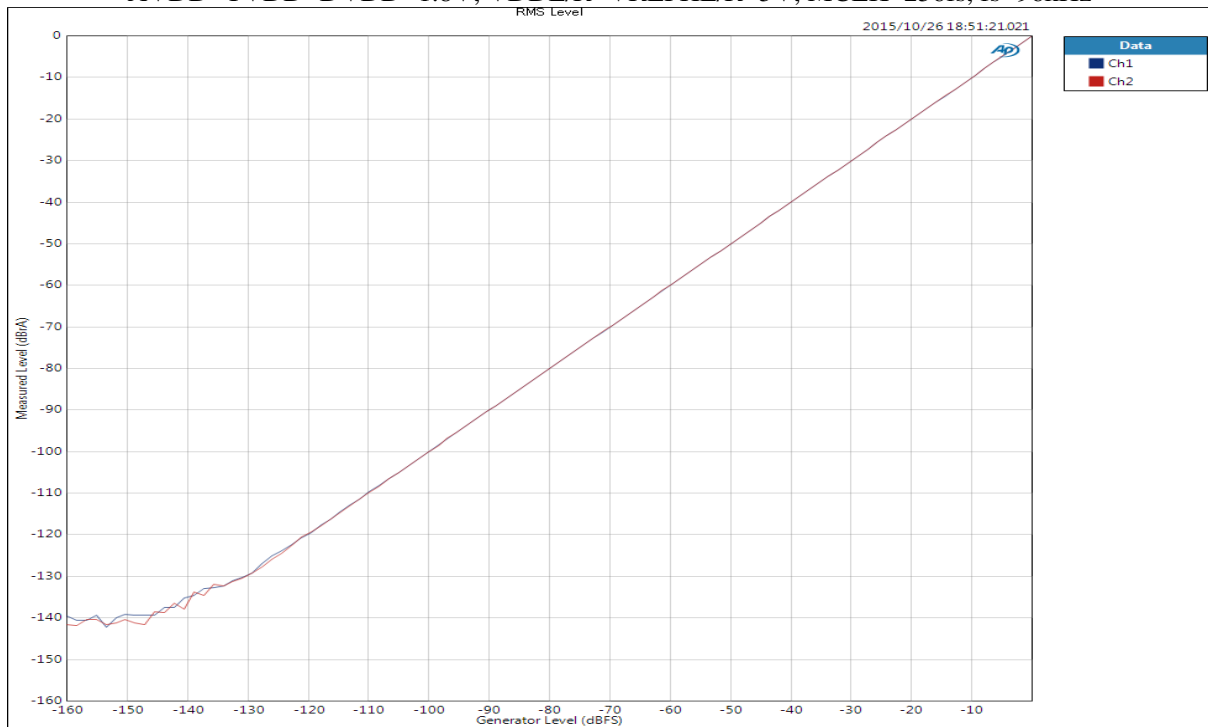


Figure 24. Linearity

AK4497 Frequency Response

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

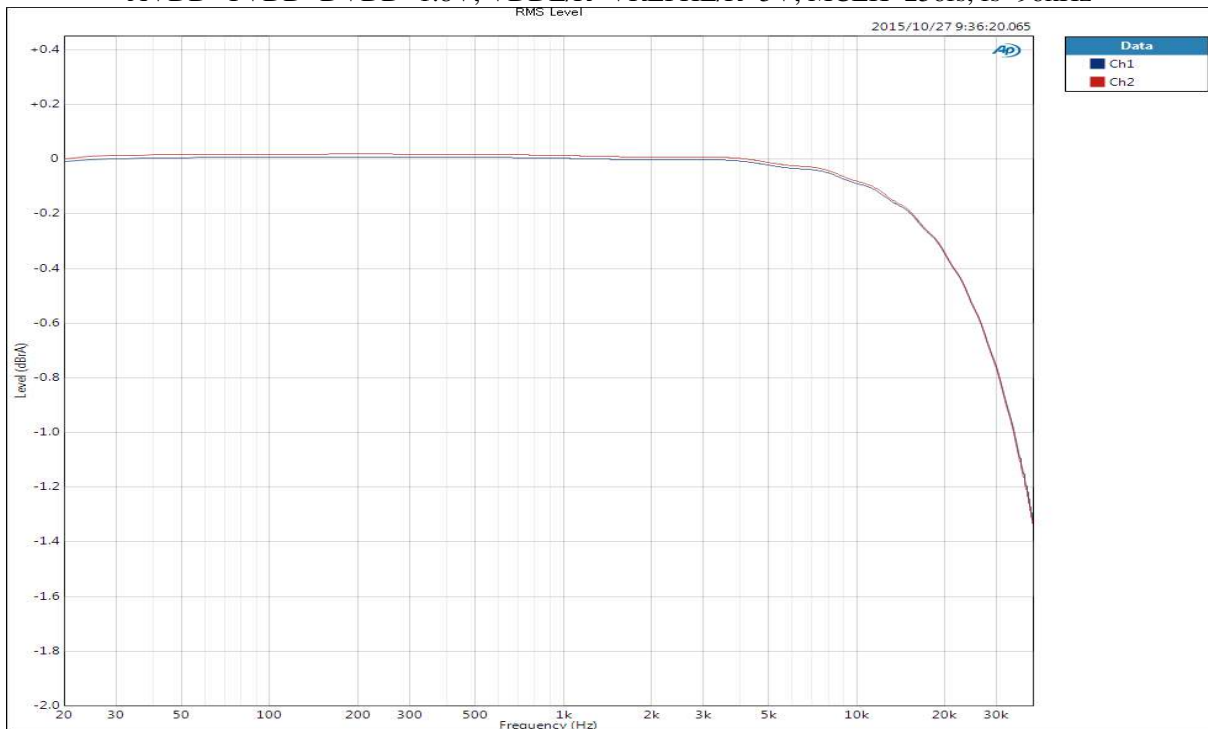


Figure 25. Frequency Response

fs = 96 kHz

AK4497 Crosstalk

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

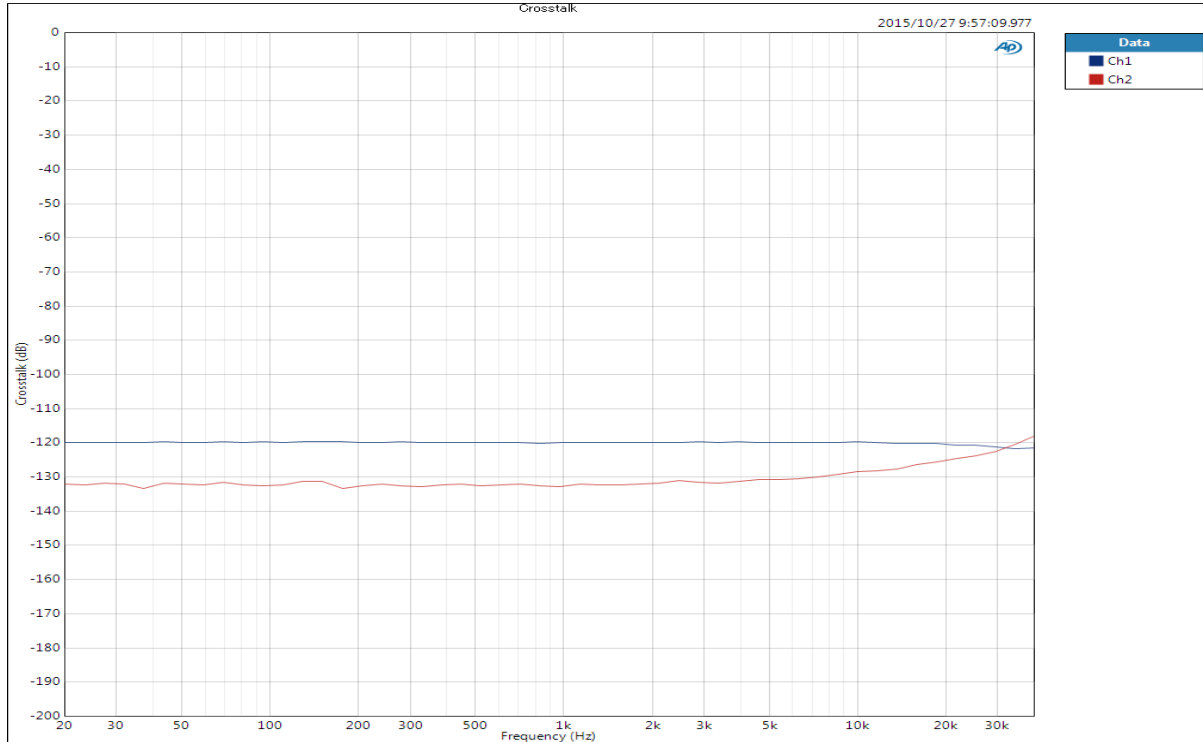


Figure 26. Crosstalk

AK4497 FFT (0dBFS Input)

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

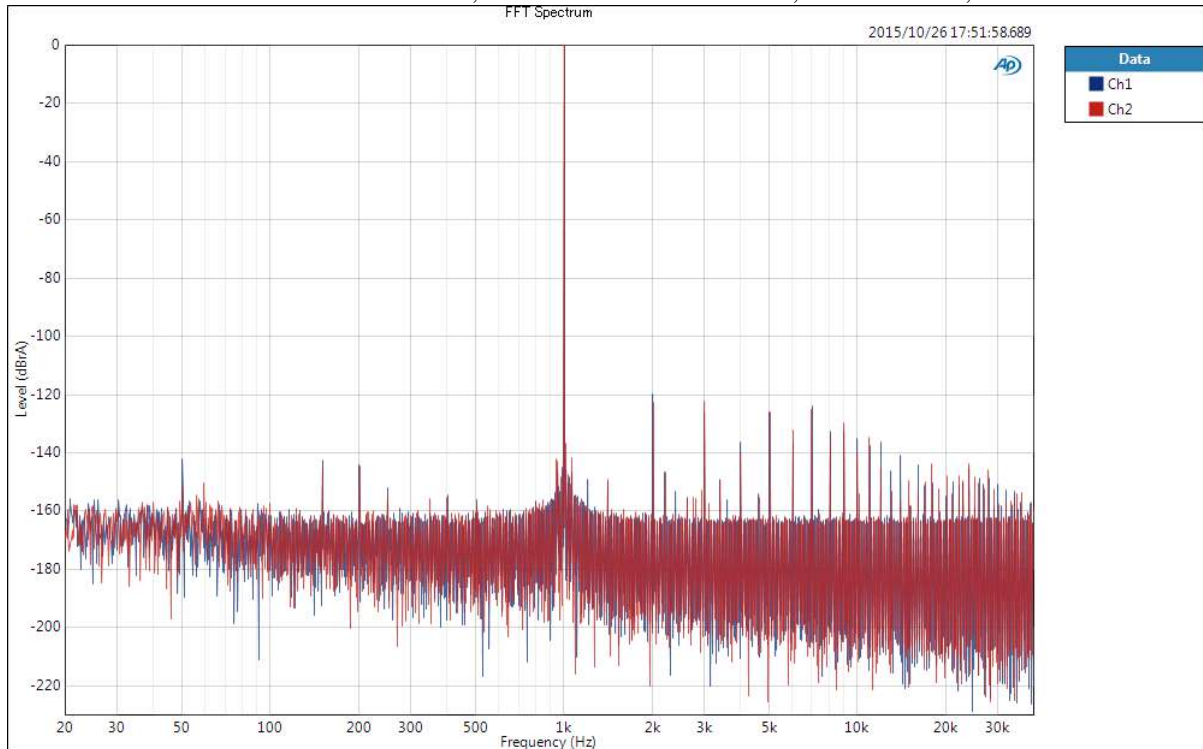


Figure 27. FFT (0dBFS Input)

fs = 96 kHz

AK4497 FFT (-60dBFS Input)
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

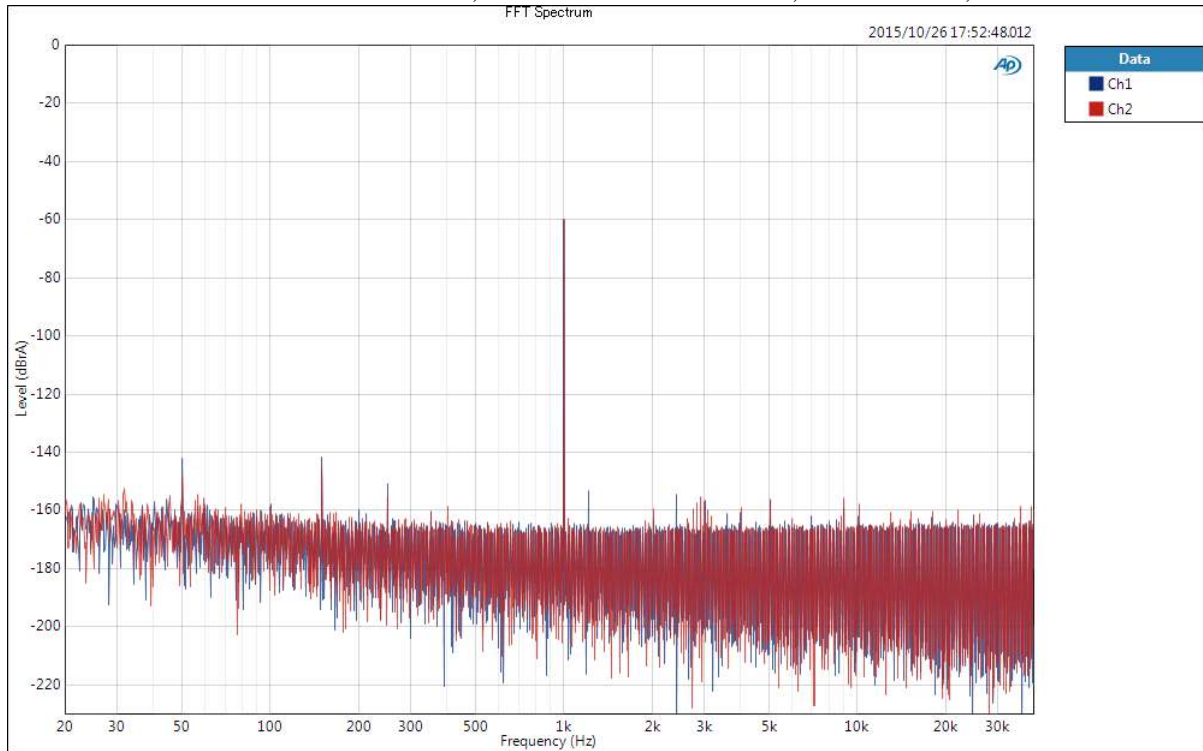


Figure 28. FFT (-60dBFS Input)

AK4497 FFT (No Signal Input)
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

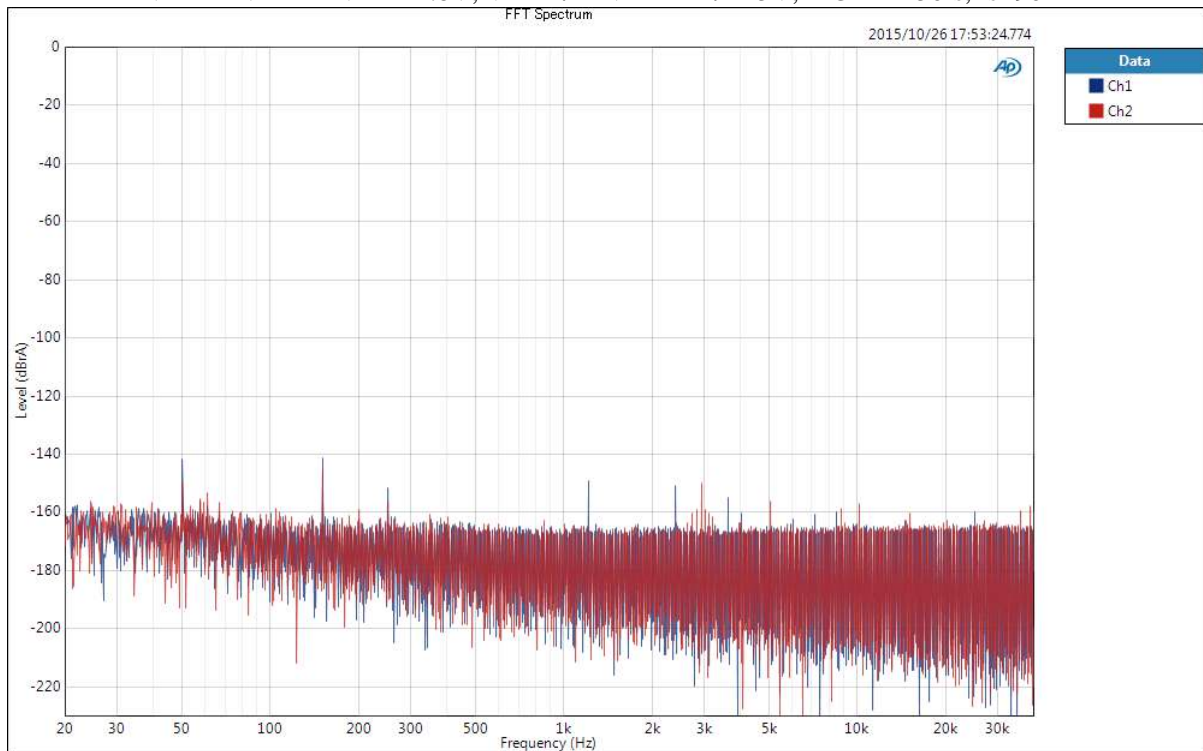


Figure 29. FFT (No Signal Input)

fs = 192 kHz

AK4497 THD+N vs. Input Level
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

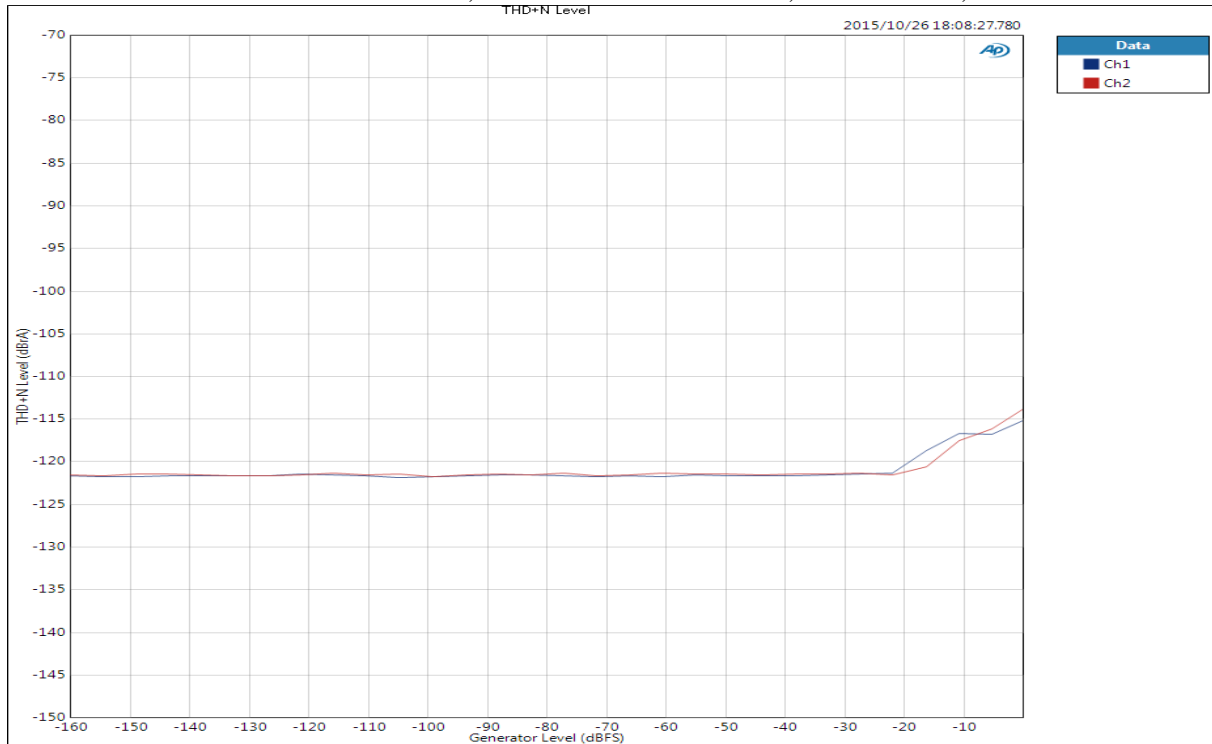


Figure 30. THD+N vs. Input Level

AK4497 THD+N vs. Input Frequency
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

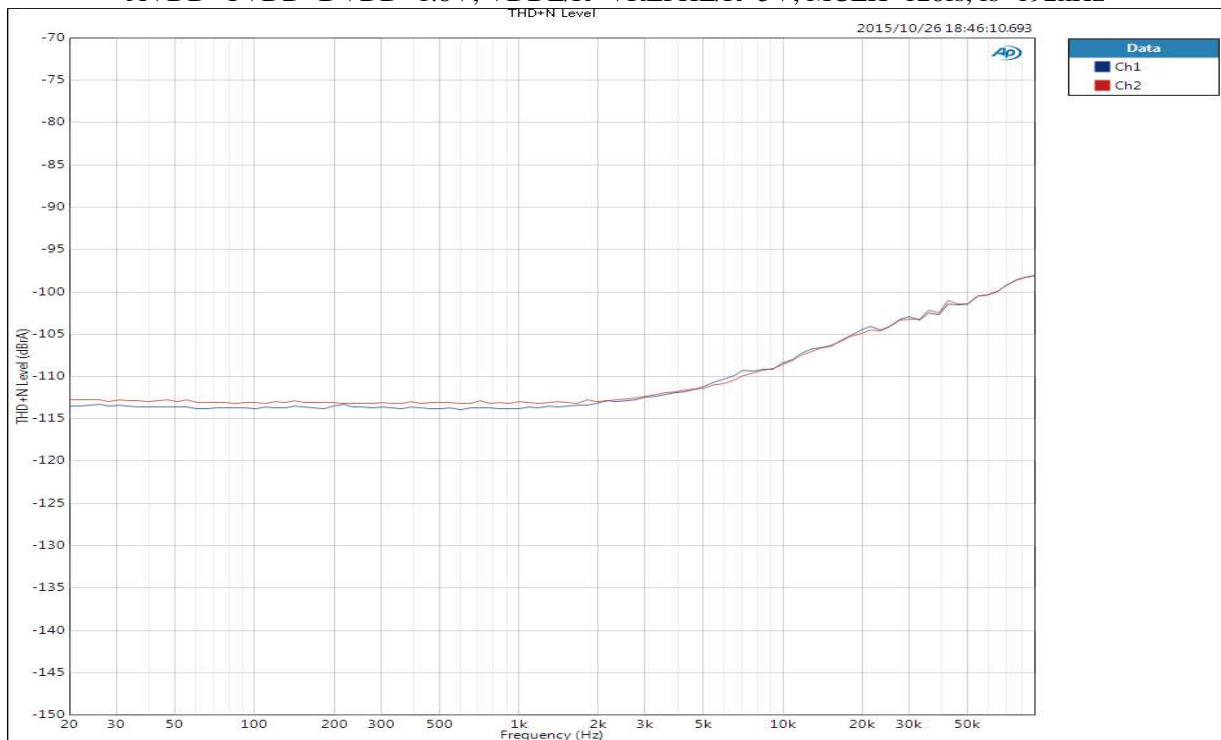
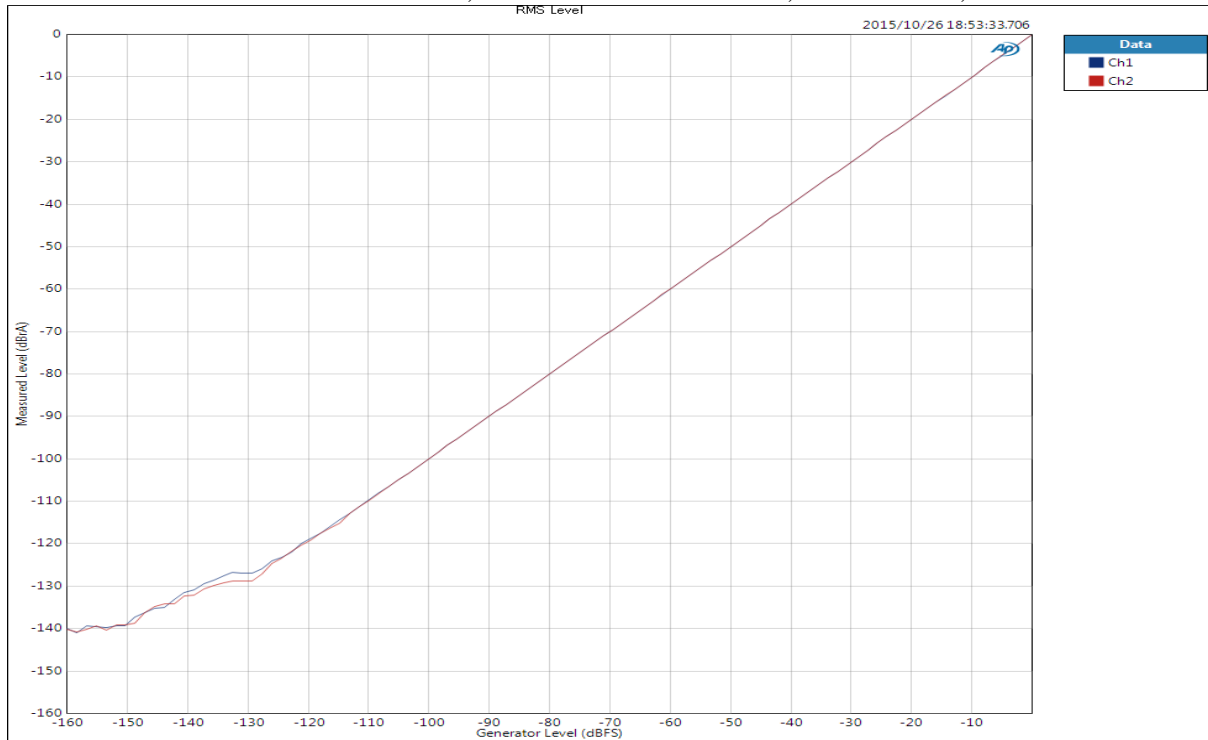


Figure 31. THD+N vs. Input Frequency

$f_s = 192 \text{ kHz}$

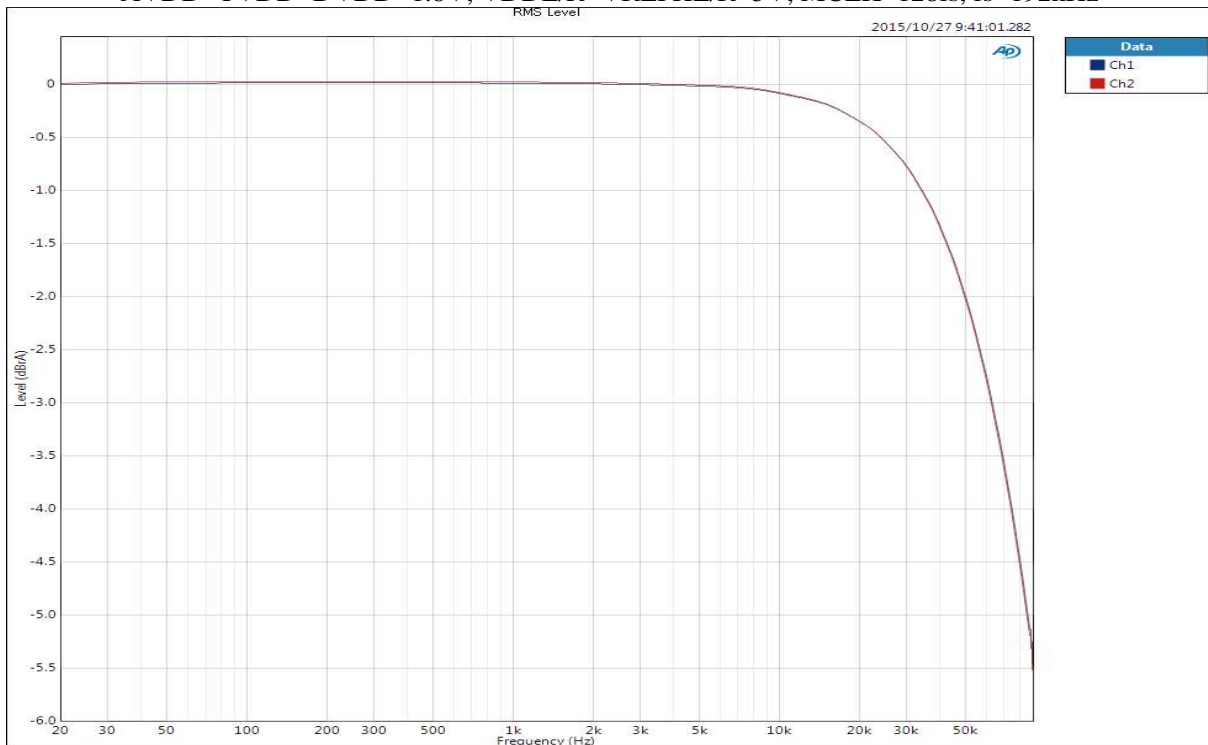
AK4497 Linearity

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, $f_s=192\text{kHz}$



AK4497 Frequency Response

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, $f_s=192\text{kHz}$



$f_s = 192 \text{ kHz}$

AK4497 Crosstalk

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, $f_s=192\text{kHz}$

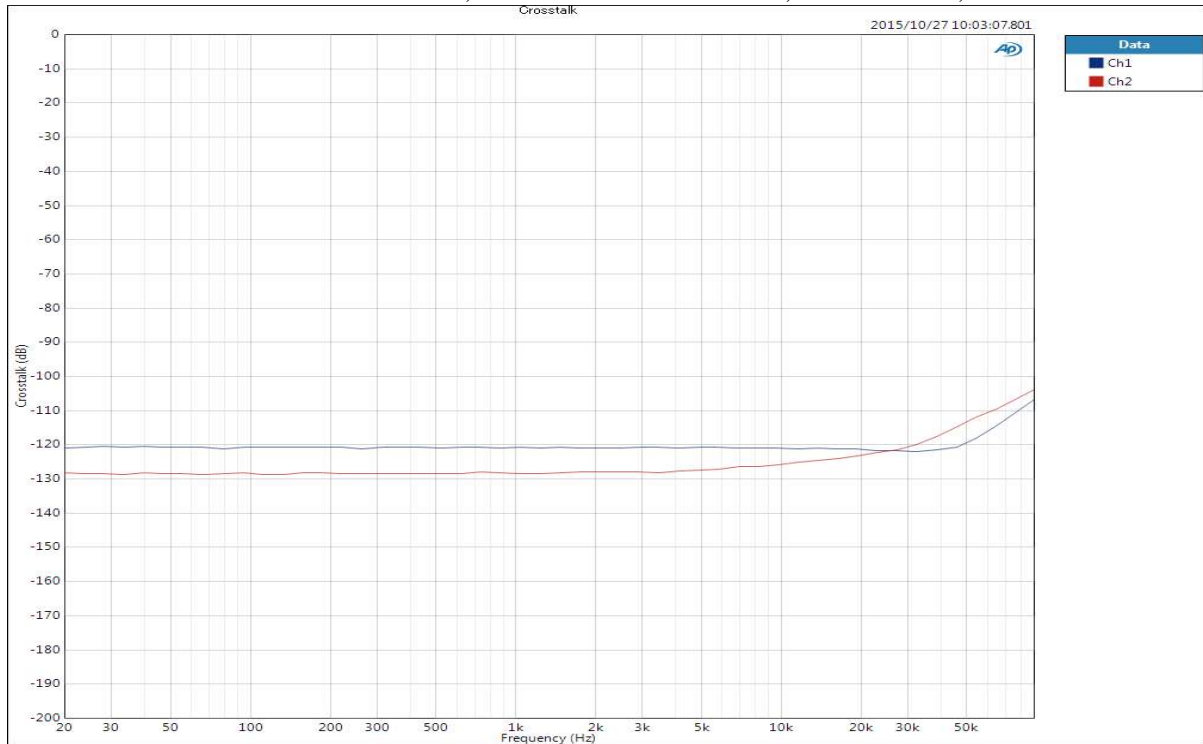


Figure 34. Crosstalk

AK4497 FFT (0dBFS Input)

AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, $f_s=192\text{kHz}$

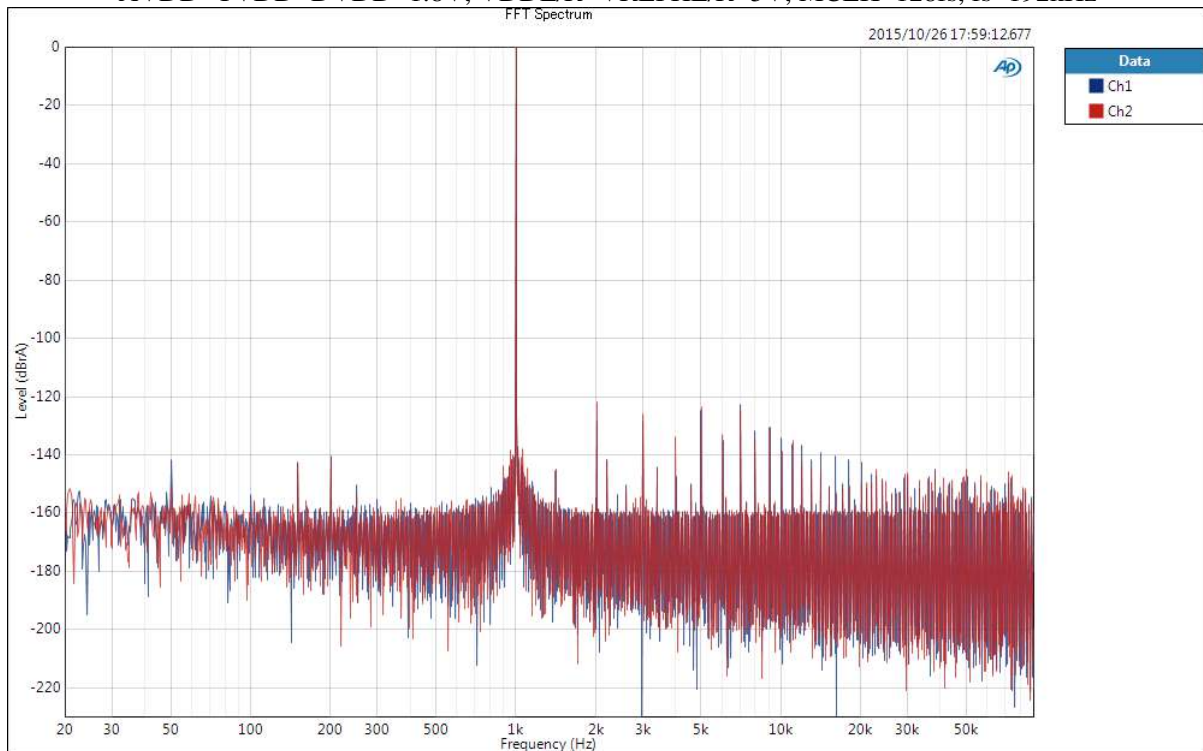


Figure 35. FFT (0dBFS Input)

fs = 192 kHz

AK4497 FFT (-60dBFS Input)
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

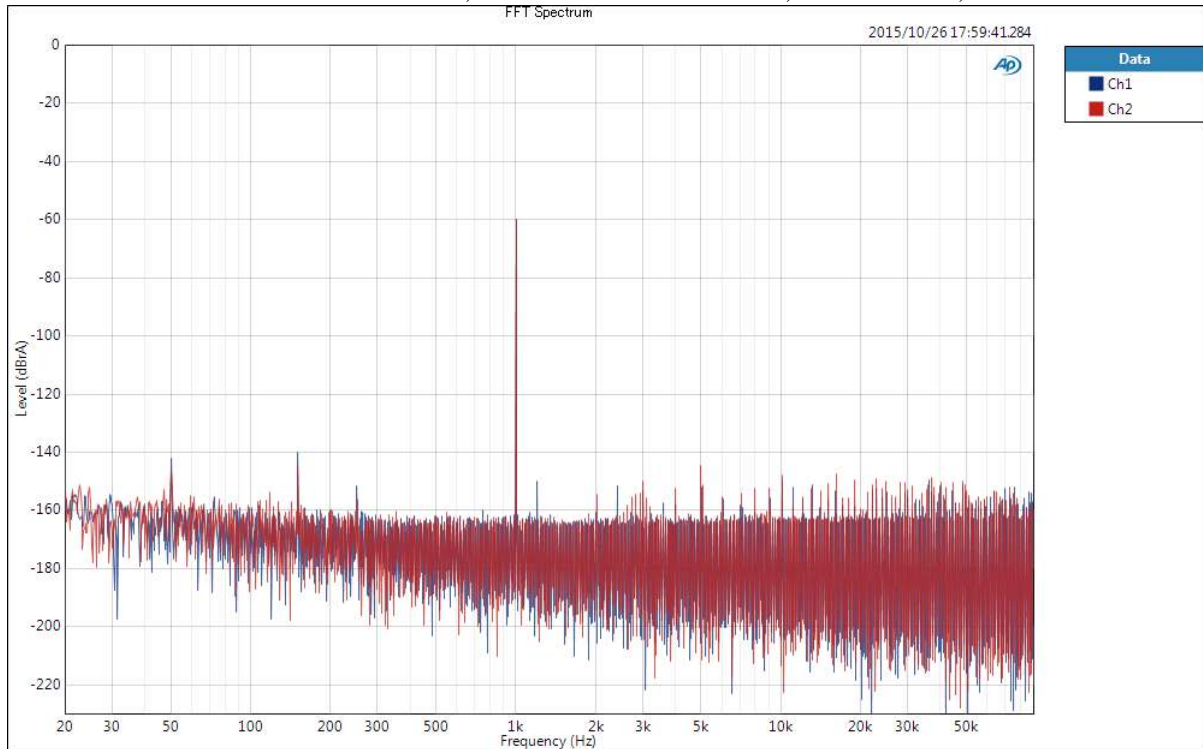


Figure 36. FFT (-60dBFS Input)

AK4497 FFT (No Signal Input)
AVDD=TVDD=DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

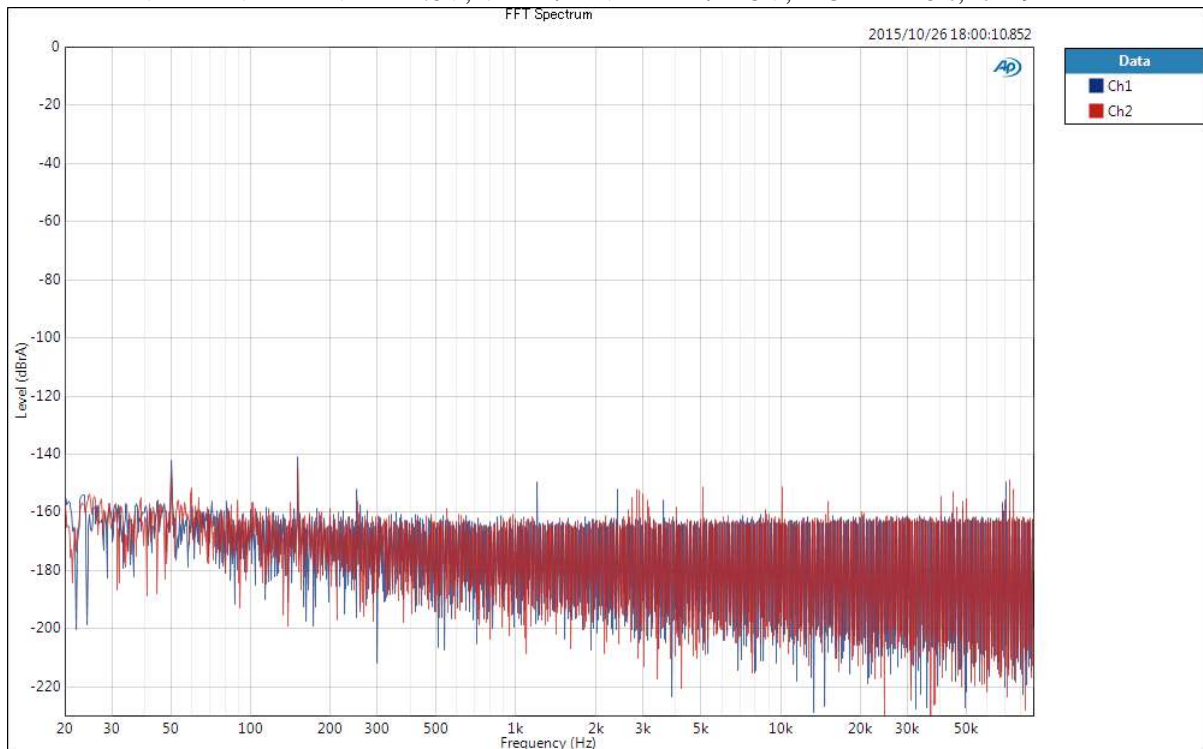


Figure 37. FFT (No Signal Input)

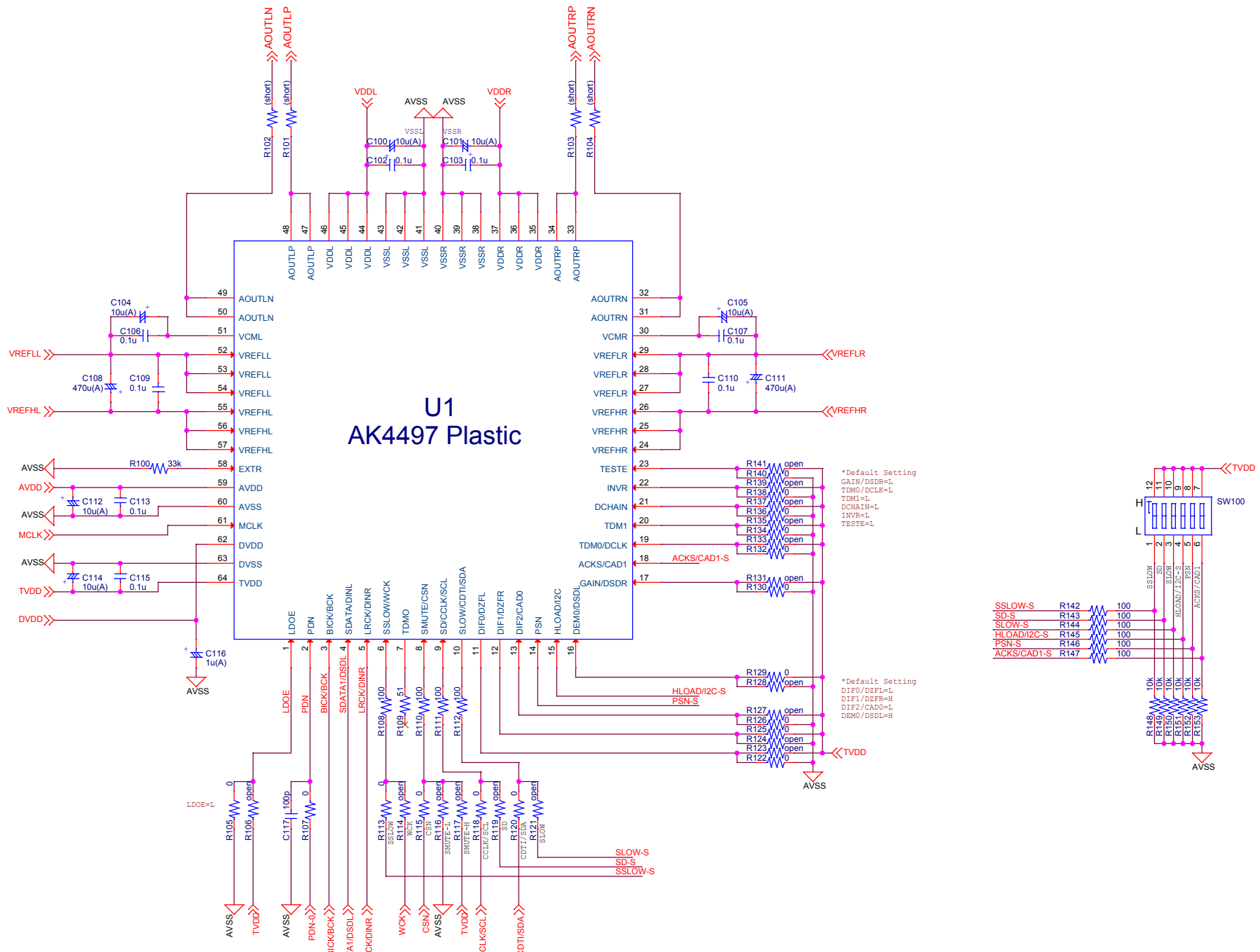
7. Revision History

Date (y/m/d)	Manual Revision	Board Revision	Reason	Page	Contents
15/10/30	KM122100	0	First Edition	-	-
20/03/09	KM122101	0	Change	7	Change setting. Table 6. Digital Filter Setting

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Rev.1



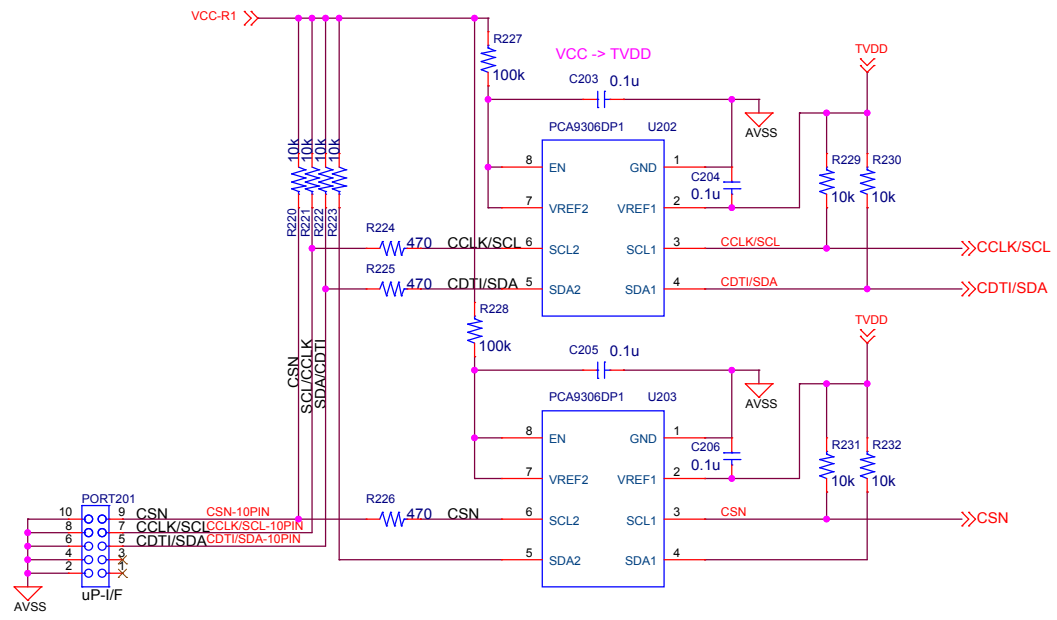
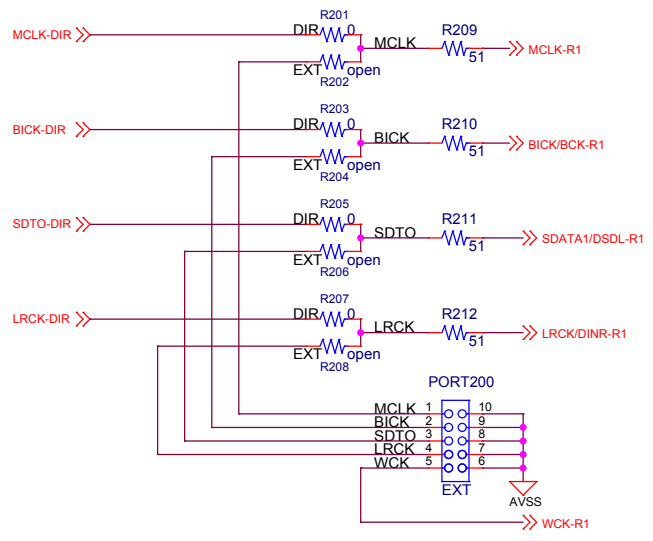
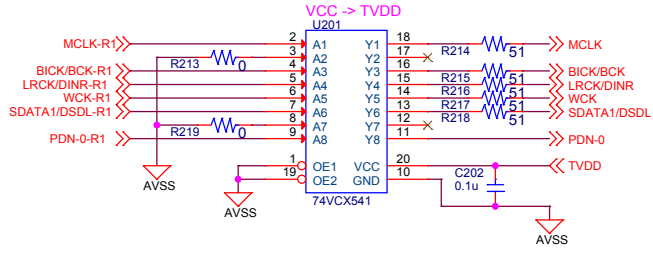
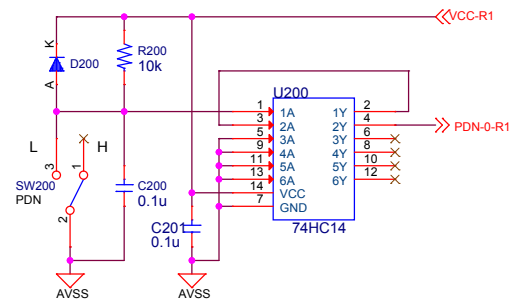
U1
AK4497 Plastic

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TDM0/DCLK=L
TDMI=L
DCHIN=L
INVR=L
TESTE=L

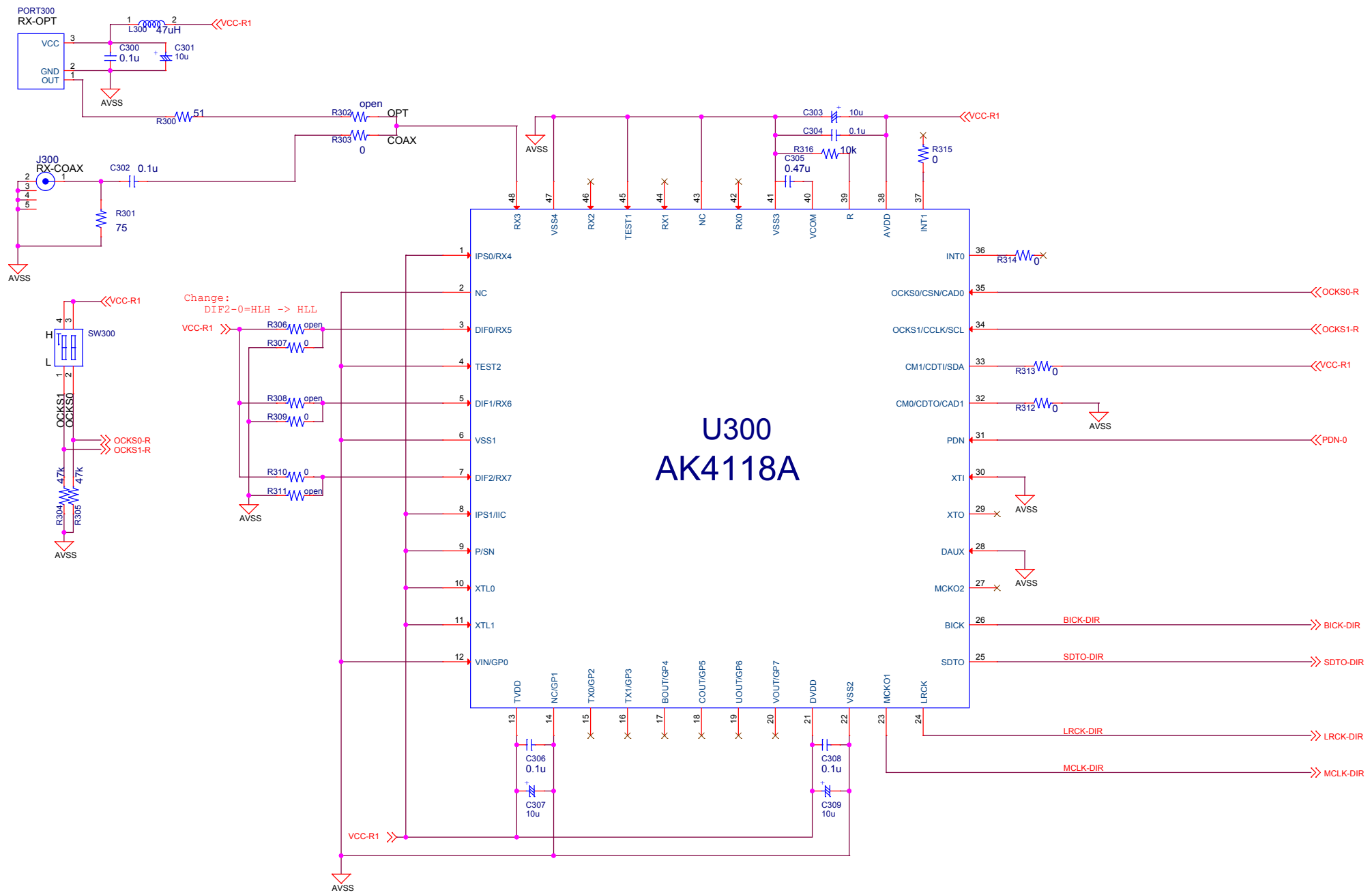
*Default Setting
DIF0/D2FL=L
DIF1/D2FR=H
DIF2/CAD0=L
DEMO/DSDI=H

- SSLOW-S R142 100
- SD-S R143 100
- SLOW-S R144 100
- HLOAD/I2C-S R145 100
- PSN-S R146 100
- ACKS/CAD1-S R147 100

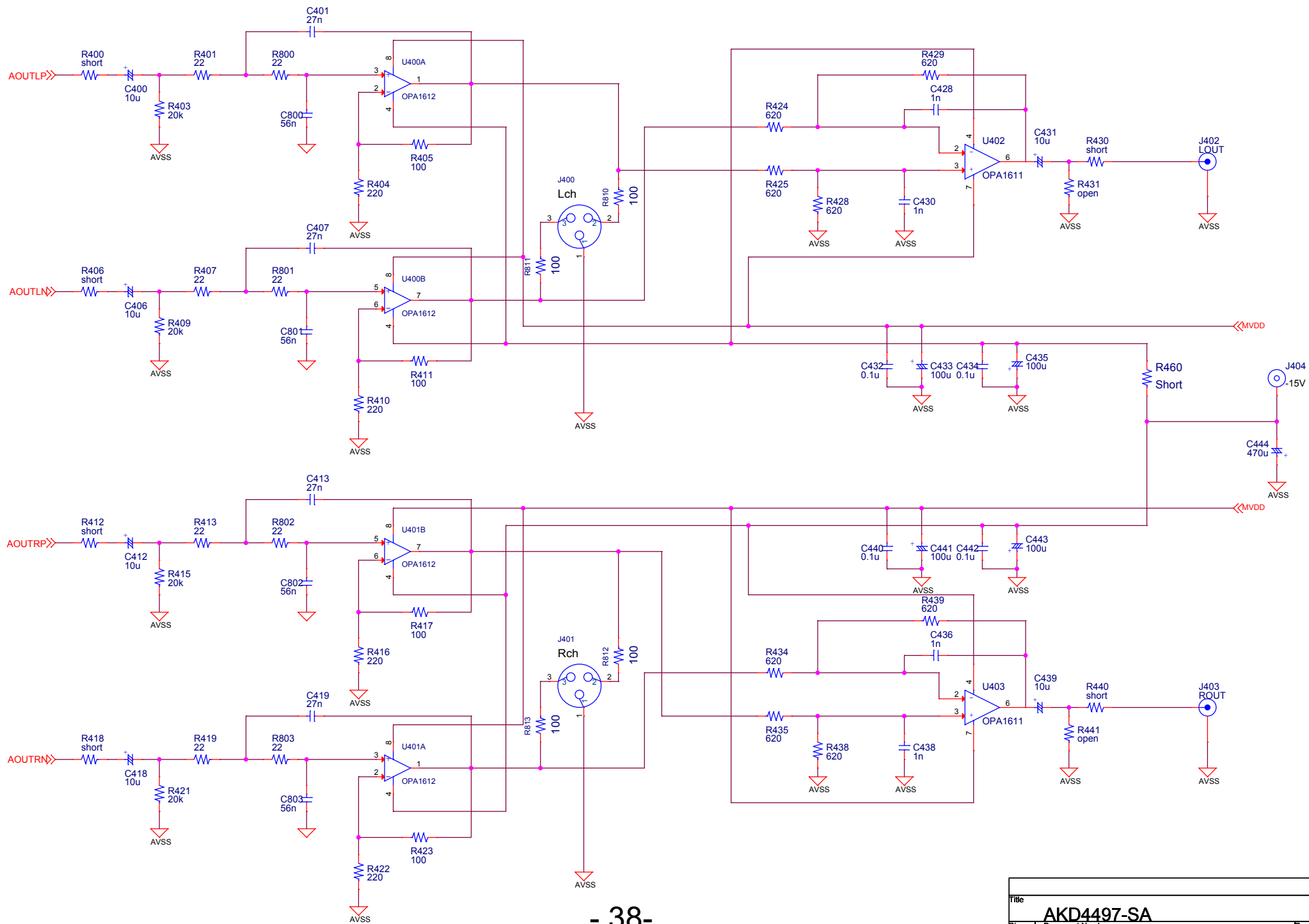
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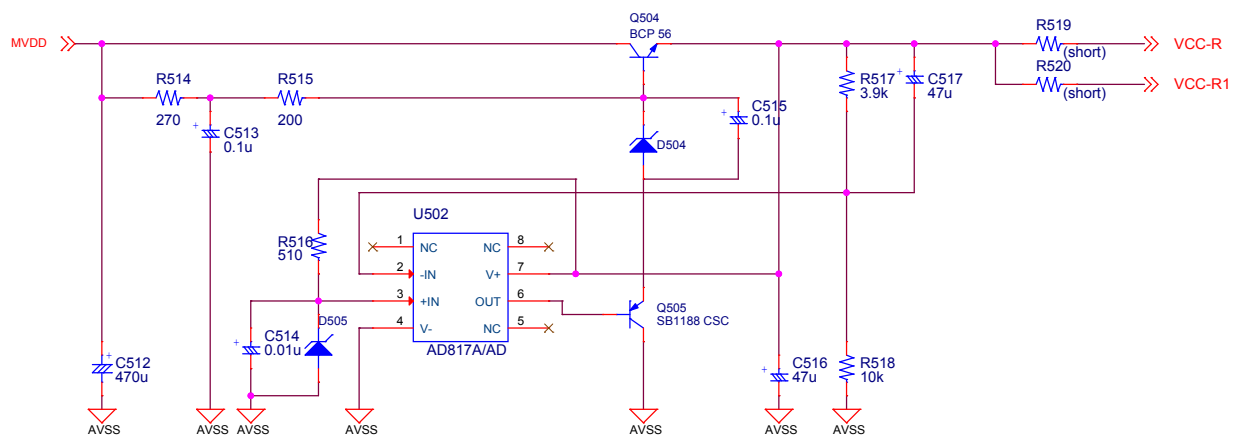
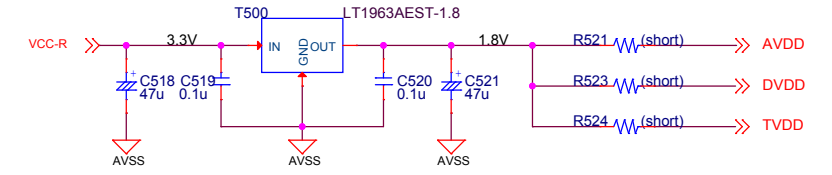
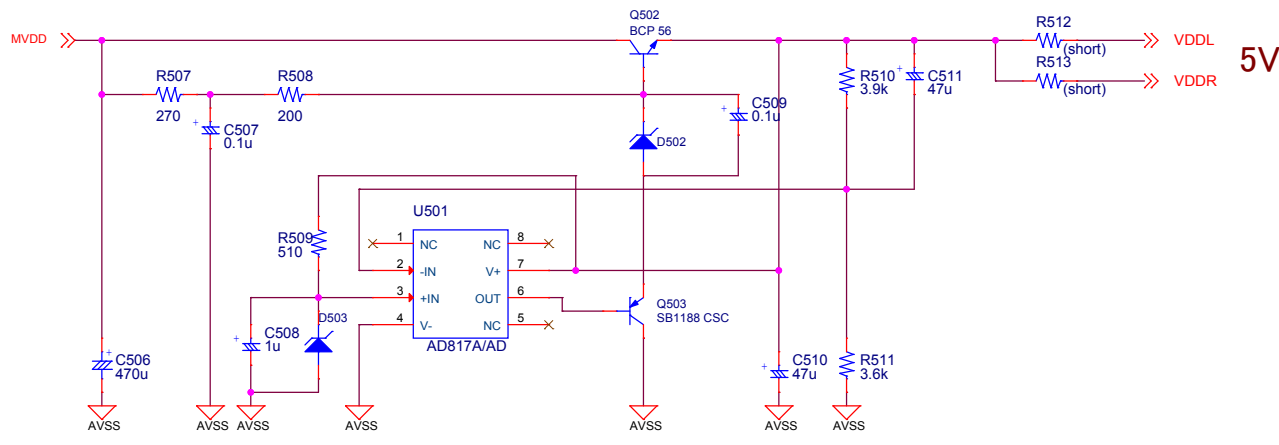
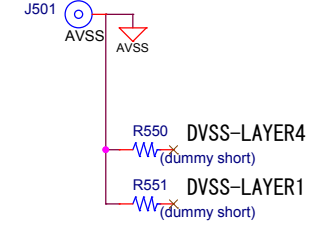
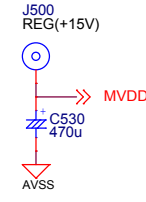
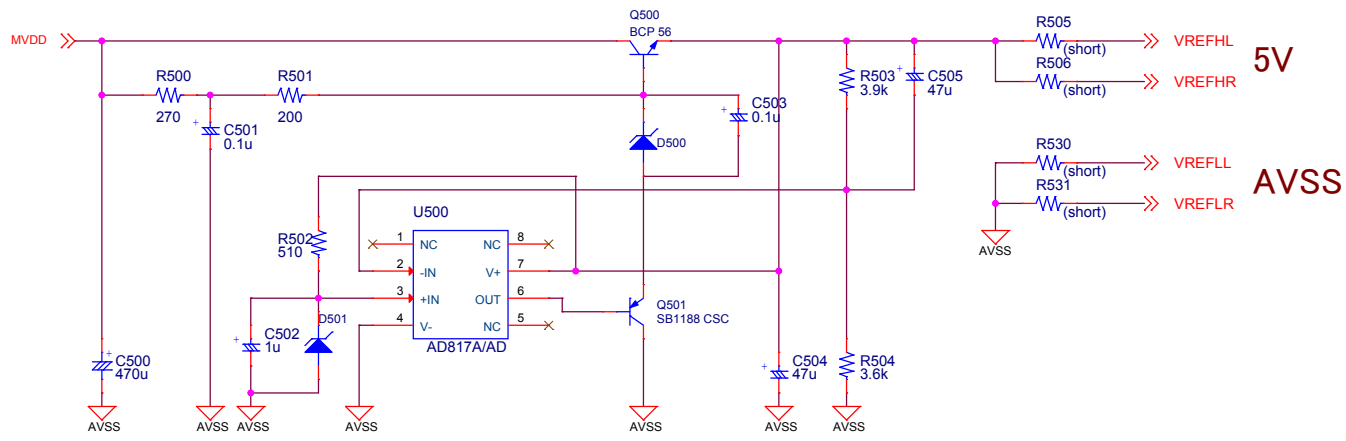
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VCC-R -> Regulator(3.3V->1.8V)
3.3V
 VCC-R1 -> AK4118A, DigitalSignal

Title		
AKD4497-SA		
Size	Document Number	Rev
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Pwuer Supply Unit		
Date:	Thursday, October 29, 2015	Sheet 5 of 5