ISOx5 Isolated 3.3-V Half- and Full-Duplex RS-485 Transceivers

1 Features

- Meets or exceeds TIA/EIA RS-485 requirements
- 1/8 unit load – Up to 256 nodes on a bus
- Signaling rates up to 1 Mbps
- Thermal shutdown protection
- Low bus capacitance – 16 pF (typical)
- 50 kV/μs typical transient immunity
- Fail-safe receiver for bus open, short, idle
- 3.3-V inputs are 5-V tolerant
- Safety and regulatory approvals
  - 4000-V_{PK} V_{IOTM}, 560-V_{PK} V_{IORM} per DIN EN IEC 60747-17 (VDE 0884-17)
  - 2500 V_{RMS} isolation rating per UL 1577
  - 2500 V_{RMS} isolation rating per CSA 62368-1.

2 Applications

- Security systems
- Chemical production
- Factory automation
- Motor and motion control
- HVAC and building automation networks
- Networked security stations

3 Description

The ISO15 is an isolated half-duplex differential line transceiver while the ISO35 is an isolated full-duplex differential line driver and receiver for TIA/EIA 485/422 applications. The ISO15M and ISO35M have extended ambient temperature ratings of –55°C to 125°C while the ISO15 and ISO35 are specified over –40°C to 85°C.

These devices are ideal for long transmission lines because the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical barrier of the device is tested to provide isolatlion of 4000 V_{PK} per VDE and 2500 V_{RMS} per UL and CSA between the bus-line transceiver and the logic-level interface.

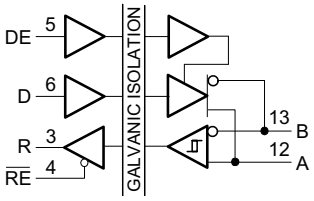
Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or nearby sensitive circuitry if they are of sufficient magnitude and duration. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO15	SOIC (16)	10.30 mm × 7.50 mm
ISO35		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ISO15x



Simplified Schematic

ISO35x

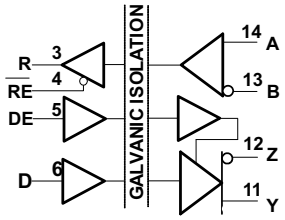


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2015) to Revision H (August 2023) **Page**

- Updated the CSA standard to CSA 62368-1, Updated VDE standard to DIN EN IEC 60747-17 (VDE 0884-17)....1
- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations....7

Changes from Revision F (January 2012) to Revision G (October 2014) **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section....1
- Changed VDE standard to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12....1

Changes from Revision E (April 2010) to Revision F (January 2012) **Page**

- Changed the FEATURES From: 4000-V_{peak} 560-V_{peak} V_{IORM} per IEC....Rev 2) To: 4000-V_{PK} V_{IOTM}, 560-$V_{PK}V_{IORM}$, IEC 60747-5-2 (VDE 0884, Rev 2)....1
- Changed Description From: The symmetrical isolation.....interface. To; The symmetrical isolation barrier of the device is tested to provide isolatlion of 4000 V_{PK} per VDE and 2500 V_{RMS} per UL and CSA between ....interface....1
- Updated electrical and switching characteristics to match device performance....9

Changes from Revision D (March 2009) to Revision E (April 2010) **Page**

- Added devices ISO15M and ISO35M to the data sheet....1
- Changed Description - From: The ISO15 and ISO35 are qualified for use from –40°C to 85°C. To: The ISO15M and ISO35M have extended ambient temperature ratings of –55°C to 125°C while the ISO15 and ISO35 are specified over –40°C to 85°C....1
- Added the Driver output pins Note for Figure 7-1 through Figure 7-4....14

- Changed the Driver output pins Note for Figure 7-5 through Figure 7-6 14

Changes from Revision B (July 2008) to Revision C (December 2008) **Page**

- Added added IEC.....Approved..... 1

Changes from Revision A (June 2008) to Revision B (July 2008) **Page**

- Changed From: 4000-Vpeak Isolation To: 4000-Vpeak Isolation, 560-Vpeak VIORM UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2)..... 1
- Changed Figure 7-13, Full-Duplex Common-Mode Transient Immunity Test Circuit.....14

5 Pin Configuration and Functions

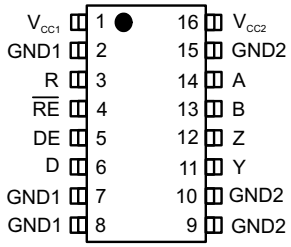


Figure 5-1. ISO35x DW Package 16-Pin SOIC Top View

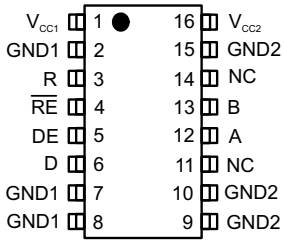


Figure 5-2. ISO15x DW Package 16-Pin SOIC Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO15x NO.	ISO35x NO.		
A	12	14	I/O	ISO15x: Noninverting bus input or output
			I	ISO35x: Noninverting bus input
B	13	13	I/O	ISO15x: Inverting bus input or output
			I	ISO35x: Inverting bus input
D	6	6	I	Driver input
DE	5	5	I	Driver logic-high enable input
GND1	2,7,8	2,7,8	—	Logic side ground; internally connected
GND2	9,10,15	9,10,15	—	Bus side ground; internally connected
NC	11,14	—	—	Not connected internally; may be left floating
R	3	3	O	Receiver output
$\overline{RE}$	4	4	I	Receiver logic-low enable
V_{CC1}	1	1	—	Logic side power supply
V_{CC2}	16	16	—	Bus side power supply
Y	—	11	O	Noninverting bus output
Z	—	12	O	Inverting bus output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC1}	Supply voltage, side 1(2)	-0.3	6	V
V_{CC2}	Supply voltage, side 2(2)	-0.3	6	V
VO	Voltage at any bus I/O terminal	-9	14	V
Vit	Voltage input, transient pulse, A, B, Y, and Z (through 100Ω, see Figure 13)	-50	50	V
V_I	Voltage input at any D, DE or RE terminal	-0.5	6	V
I_O	Receiver output current	-10	10	mA
T_J	Junction temperature		150	℃
T_{STG}	Storage temperature	-65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins and GND1	±6000	V
$V_{(ESD)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins and GND2	±16000	V
$V_{(ESD)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±4000	V
$V_{(ESD)}$	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±1000	V
$V_{(ESD)}$	Machine model ANSI/ESDS5.2-1996		±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{CC1}	Supply Voltage, Side 1	3.15	3.3	3.6	V
V_{CC2}	Supply Voltage, Side 2	3.15	3.3	3.6	V
V_{OC}	Common Mode voltage at any bus terminal: A or B	-7		12	V
V_{IH}	High-level input voltage (D, DE, $\overline{RE}$ inputs)	2		V_{CC1}	V
V_{IL}	Low-level input voltage (D, DE, $\overline{RE}$ inputs)	0		0.8	V
V_{ID}	Differential input voltage, A with respect to B	-12		12	V
R_L	Differential load resistance	54	60		Ω
I_O	Output current, Driver	-60		60	mA
$1/t_{UI}$	Signaling rate ISO15x and ISO35x			1	Mbps
T_A	Operating ambient temperature (ISO15 and ISO35)	-40	25	85	°C
	Operating ambient temperature (ISO15M and ISO35M)	-55	25	125	°C

		MIN	TYP	MAX	UNIT
T_J	Operating juntion temperature (ISO15 and ISO35)	-40		150	°C
	Operating junction temperature (ISO15M and ISO35M)	-55		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		ISO15, ISO35 DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 3.6$ V, TJ = 150°C, C_L = 15 pF, Input a 0.5 MHz 50% duty cycle square wave			220	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE DW-16	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	8	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) [2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	4000	V_{PK}
q_{pd}	Apparent charge[3]	Method b; At routine test (100% production) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤5	pC
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 x sin (2πft), f = 1 MHz	2	pF
C_I	Input capacitance to ground	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, f = 1 MHz, V_{CC} = 3.3 V	2	pF
R_{IO}	Isolation resistance[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, T_S = 150°C	$>10^9$	
	Pollution degree		2	
	Climatic Category		40/125/21	
UL 1577				

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DW-16	
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), V_{TEST} = 1.2 x V_{ISO} , t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 60950-1 and IEC 62368-1	Certified according to UL 1577 Component Recognition Program
Basic insulation, 4000 V_{PK} Maximum transient isolation voltage, 560 V_{PK} Maximum repetitive peak isolation voltage	2500 V_{RMS} Isolation rating, Reinforced insulation per CSA 60950-1 and IEC 60950-1 148V_{RMS} working voltage; Basic insulation per CSA 62368-1 and IEC 62368-1 300V_{RMS} working voltage	Single protection, 2500 V_{RMS}
Certificate number: 40047657	Master contract number: 220991	File number: E181974

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 79.6°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C.			436	mA
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics: Driver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential-output voltage magnitude	I_O = 0 mA, no load	2.5		V_{CC2}	V
		R_L = 54 Ω, See Figure 3	1.5	2		V
		R_L = 100 Ω (RS-422), See Figure 3	2	2.3		V
		V_{test} from –7 V to +12 V, See Figure 4	1.5			V
$\Delta\|V_{OD}\|$	Change in differential output voltage between two states	See Figure 3 and Figure 4	–200		200	mV
V_{OC}	Common-mode output voltage	See Figure 5	1	2.6	3	V
$\Delta V_{OC(SS)}$	change in steady-state common-mode output voltage between two states	See Figure 5	–100		100	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 5		0.5		V
I_I	Input current	D, DE, V_I at 0 V or V_{CC1}	–10		10	µA
I_{OZ}	High-impedance state output current	ISO15 See receiver input current				
		ISO35 V_Y or V_Z = 12 V			90	µA
		ISO35 V_Y or V_Z = 12 V, VCC = 0			90	µA
		ISO35 V_Y or V_Z = –7 V	-10			µA
		ISO35 V_Y or V_Z = –7 V, VCC = 0	-10			µA
I_{OS}	Short-circuit output current	V_A or V_B at –7 V	–250		250	mA
		V_A or $V_B$at 12 V	–250		250	mA
C_{OD}	Differential output capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		16		pF
CMTI	Common-mode transient immunity	V_I = VCC or 0 V, See Figure 14 and Figure 15	25	50		kV/µs

6.10 Electrical Characteristics: Receiver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA			–20	mV
$V_{IT–}$	Negative-going input threshold voltage	I_O = 8 mA	–200			mV
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			50		mV
V_O	Output Voltage	V_{ID} = 200mV, I_O = -8mA	2.4			V
		V_{ID} = –200mV, I_O = 8mA			0.4	V
I_{OZ}	Output high-impedance current on the R pin	V_I = –7 to 12 V, Other input = 0 V	–1		1	µA
I_A or I_B	Bus input current	-55°C ≤ T_A ≤ 85°C V_A or V_B = 12 V		50	100	µA
		-55°C ≤ T_A ≤ 85°C V_A or V_B = 12 V, V_{CC} = 0		50	100	µA
		85°C ≤ T_A ≤ 125°C V_A or V_B = 12 V			200	µA
		85°C ≤ T_A ≤ 125°C V_A or V_B = 12 V, VCC = 0			200	µA
		-55°C ≤ T_A ≤ 125°C V_A or V_B = –7 V	-100	-40		µA
		-55°C ≤ T_A ≤ 125°C V_A or V_B = –7 V, VCC = 0	-100	-30		µA
I_{IH}	High-level input current, RE	V_{IH} = 2 V	-10			µA

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input current, RE	V_{IL} = 0.8 V	-10			µA
R_{ID}	Differential input resistance	A, B	48			kohm
C_{ID}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5V, DE at 0 V		16		pF

6.11 Supply Current

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER ENABLED, RECEIVER DISABLED					
I_{CC1}	ISO35x and ISO15x: $\overline{RE}$ at 0 V or V_{CC}, DE at 0 V, No load (driver disabled)			8	mA
I_{CC1}	ISO35x and ISO15x: $\overline{RE}$ at 0 V or V_{CC}, DE at V_{CC}, No load (driver enabled)			8	mA
I_{CC2}	ISO35x and ISO15x: $\overline{RE}$ at 0 V or V_{CC}, DE at 0 V, No load (driver disabled)			15	mA
I_{CC2}	ISO35x and ISO15x: $\overline{RE}$ at 0 V or V_{CC}, DE at V_{CC}, No Load (driver enabled)			19	mA

6.12 Switching Characteristics: Driver

All typical specs are at V_{CC1}=3.3V, V_{CC2}= 3.3V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
500-kbps DEVICES						
t_r, t_f	Differential output rise time and fall time	ISO15M and ISO35M	120	180	350	ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 7			205	ns
t_{PLZ}	Propagation delay, low-level to high-impedance output	See Figure 8			330	ns
t_{PZL}	Propagation delay, standby-to-low-level output	See Figure 8			530	ns
t_{PHL}, t_{PLH}	Propagation delay	See Figure 6			340	ns
tsk(p)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 6		6		ns
t_r, t_f	Differential output rise time and fall time	ISO15 and ISO35	120	180	300	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output	See Figure 7			530	ns

6.13 Switching Characteristics: Receiver

All typical specs are at V_{CC1}=3.3V, V_{CC2}= 3.3V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
500-kbps DEVICES						
t_{PHL}, t_{PLH}	Propagation delay	See Figure 10			100	ns
tsk(p)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	ISO15 and ISO35			13	ns
tsk(p)	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	ISO15M and ISO35M			18	ns
t_r, t_f	Differential output rise time and fall time	ISO15 and ISO35		2	4	ns
t_r, t_f	Differential output rise time and fall time	ISO15M and ISO35M		2	6	ns
t_{PHZ}, t_{PLZ}	Propagation delay, high-impedance-to-high-level output, Propagation delay, high-impedance-to-low-level output	DE at 0 V, See Figure 11 and Figure 12		13	25	ns
t_{PZH}, t_{PZL}	Propagation delay, high-level-to-high-impedance output, Propagation delay, low-level to high-impedance output	DE at 0 V, See Figure 11 and Figure 12		13	25	ns

6.14 Insulation Characteristics Curves

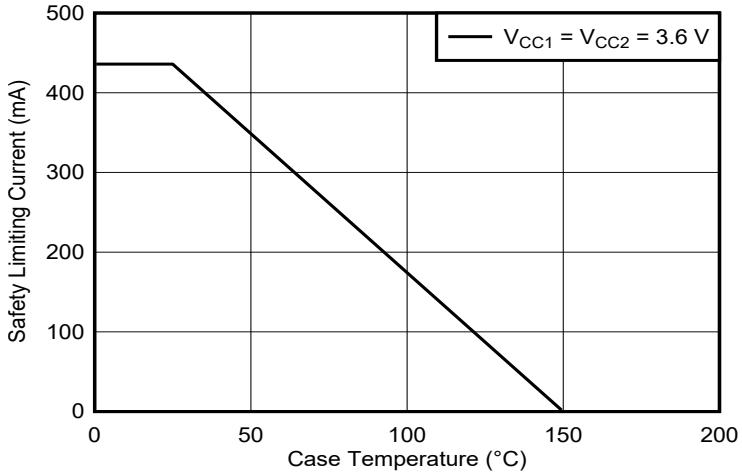


Figure 6-1. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

6.15 Typical Characteristics

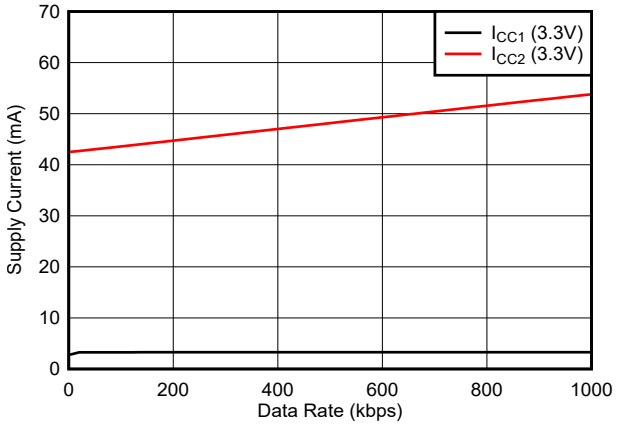


Figure 6-2. ISOx5 Supply Current vs Data Rate With Load

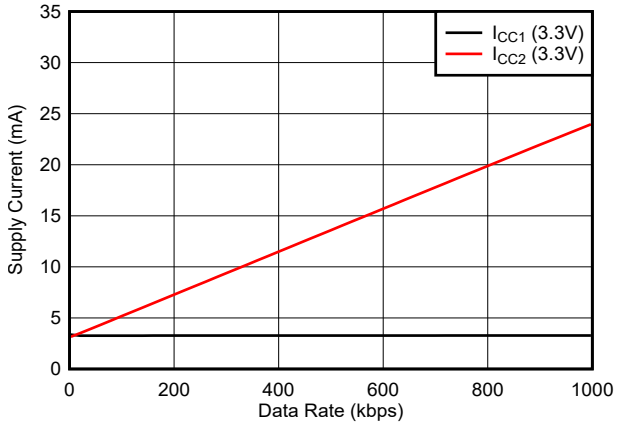


Figure 6-3. ISOx5 Supply Current vs Data Rate With No Load

7 Parameter Measurement Information

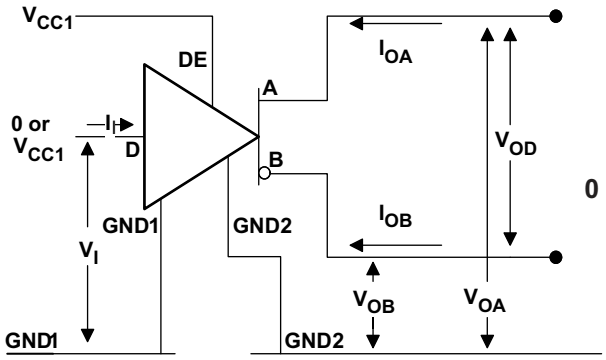


Figure 7-1. Driver V_{OD} Test and Current Definitions

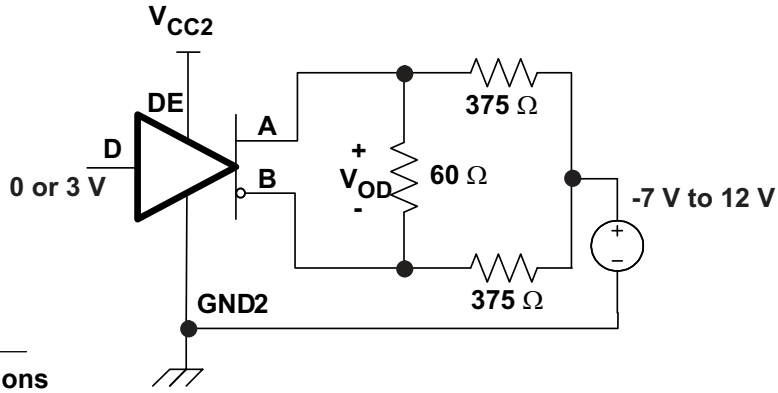


Figure 7-2. Driver V_{OD} With Common-Mode Loading Test Circuit

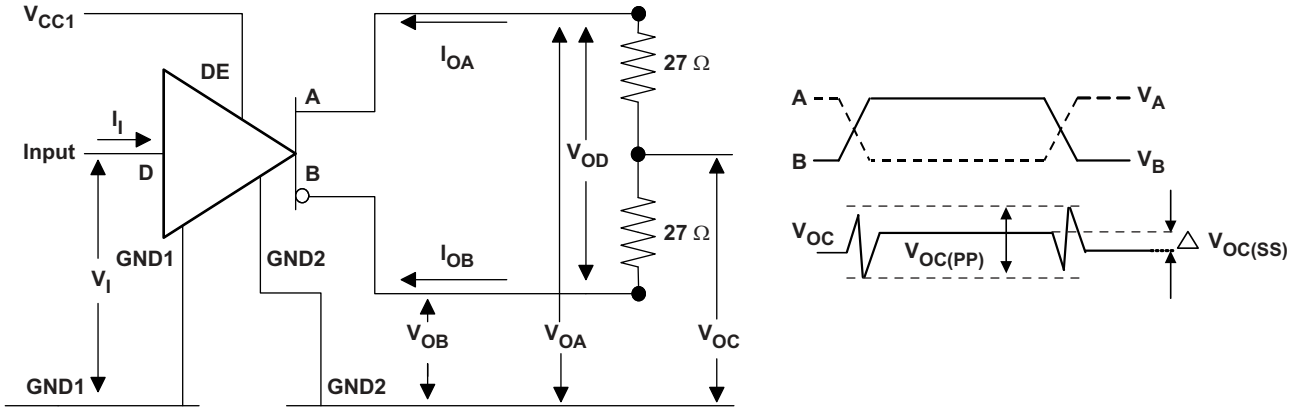
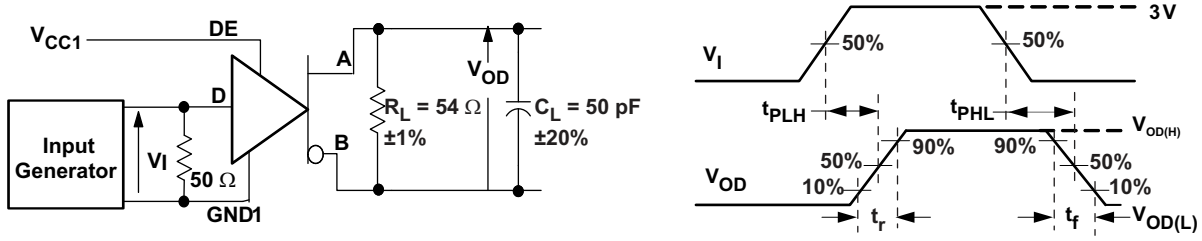


Figure 7-3. Test Circuit and Waveform Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% duty cycle, t_r <6ns, t_f <6ns, Z_O = 50 Ω

C_L includes fixture and Instrumentation Capacitance

Figure 7-4. Driver Switching Test Circuit and Voltage Waveforms

Note

Driver output pins are A and B for the ISO15 (see Figure 7-1 through Figure 7-4). These correspond to ISO35 pins Y and Z

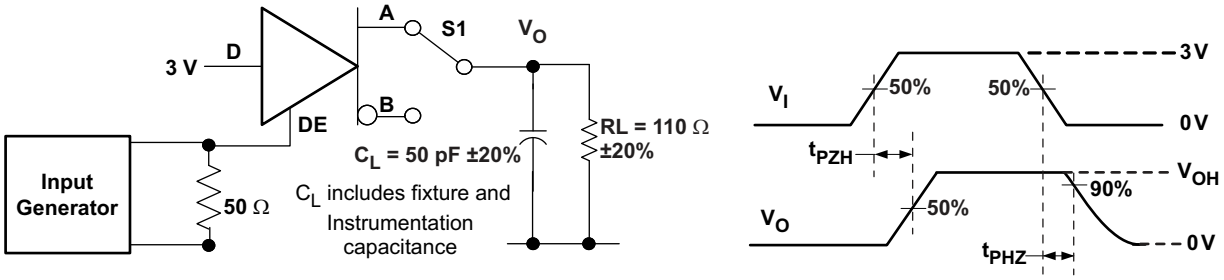
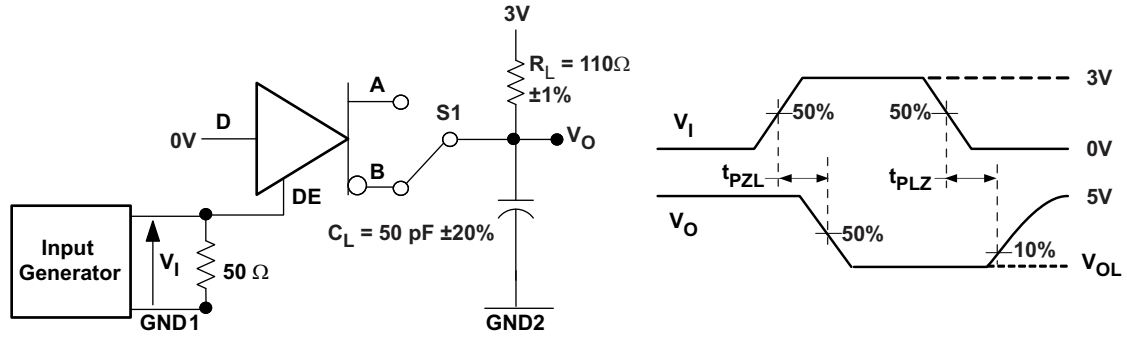


Figure 7-5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% duty cycle, t_r <6ns, t_f <6ns, Z_O = 50Ω

C_L includes fixture and Instrumentation capacitance

Figure 7-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

Note

Driver output pins are A and B for the ISO15 (see Figure 7-5 through Figure 7-6). These correspond to ISO35 pins Y and Z

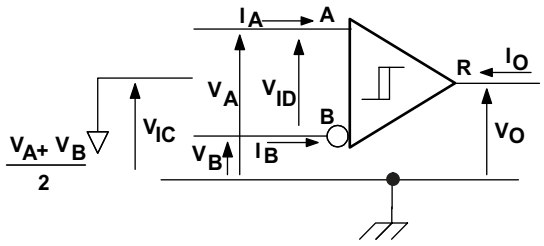
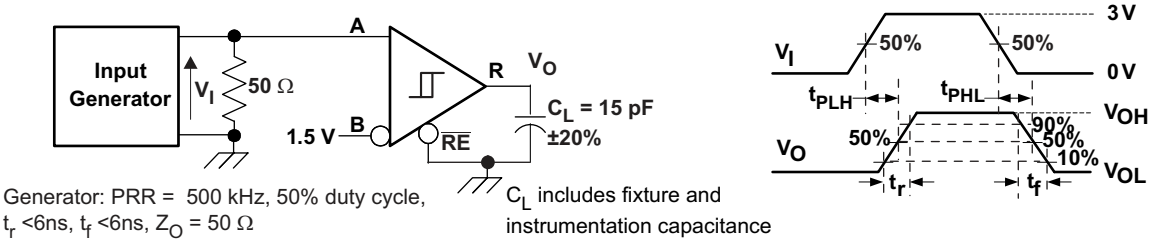


Figure 7-7. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% duty cycle, t_r <6ns, t_f <6ns, Z_O = 50 Ω

C_L includes fixture and instrumentation capacitance

Figure 7-8. Receiver Switching Test Circuit and Waveforms

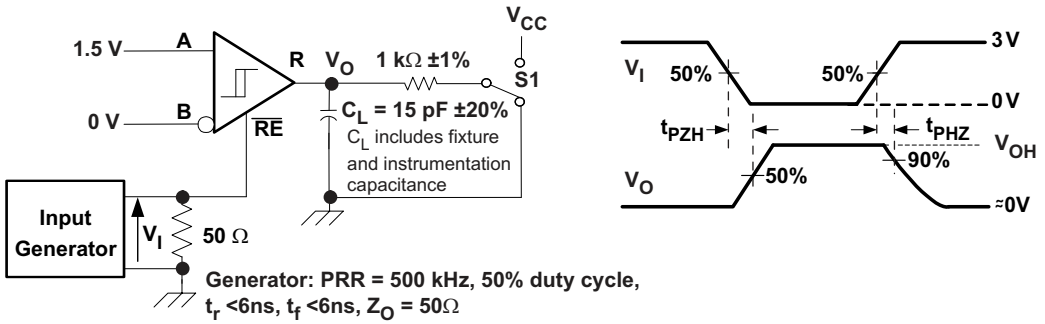


Figure 7-9. Receiver Enable Test Circuit and Waveforms, Data Output High

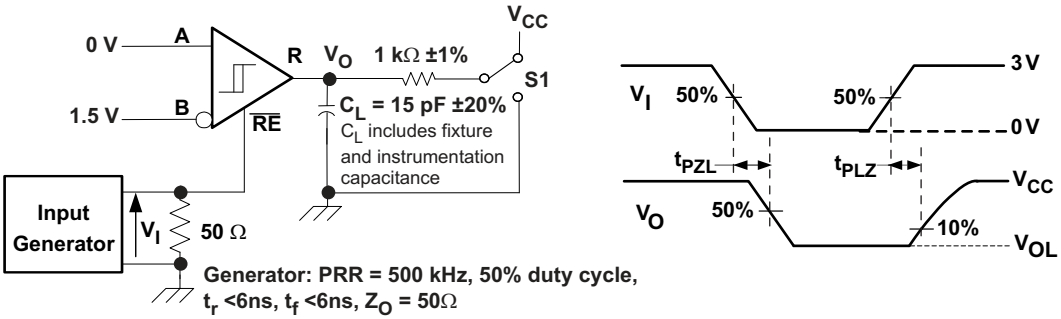
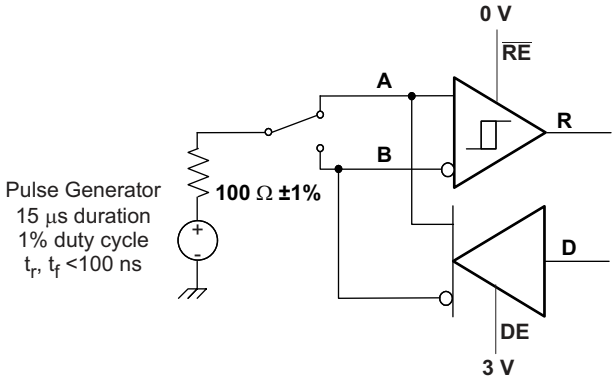


Figure 7-10. Receiver Enable Test Circuit and Waveforms, Data Output Low



Note: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 7-11. Transient Overvoltage Test Circuit

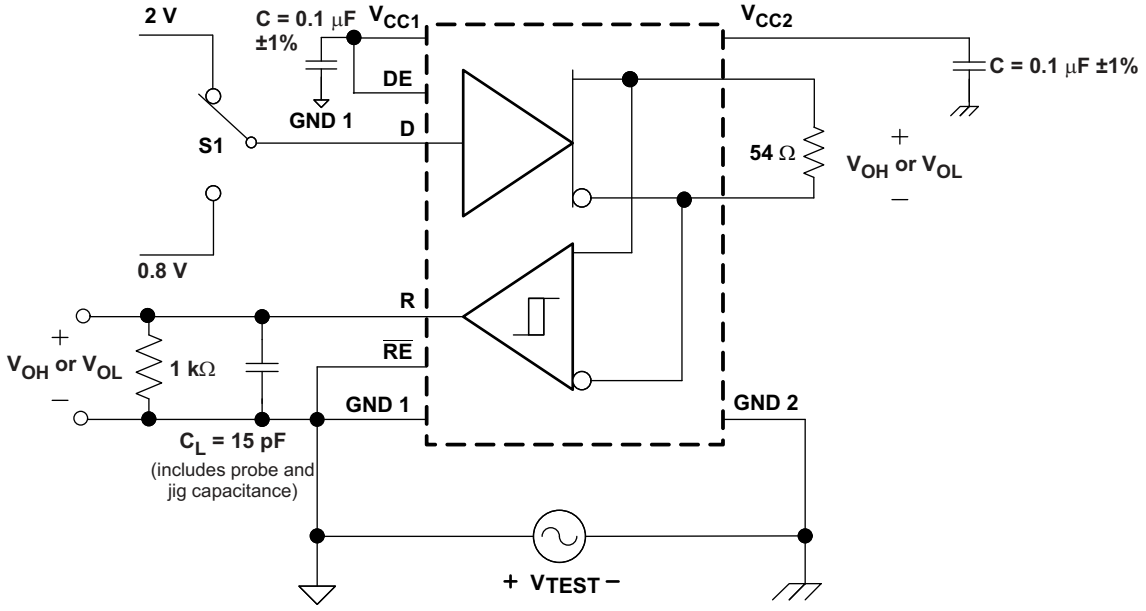


Figure 7-12. Half-Duplex Common-Mode Transient Immunity Test Circuit

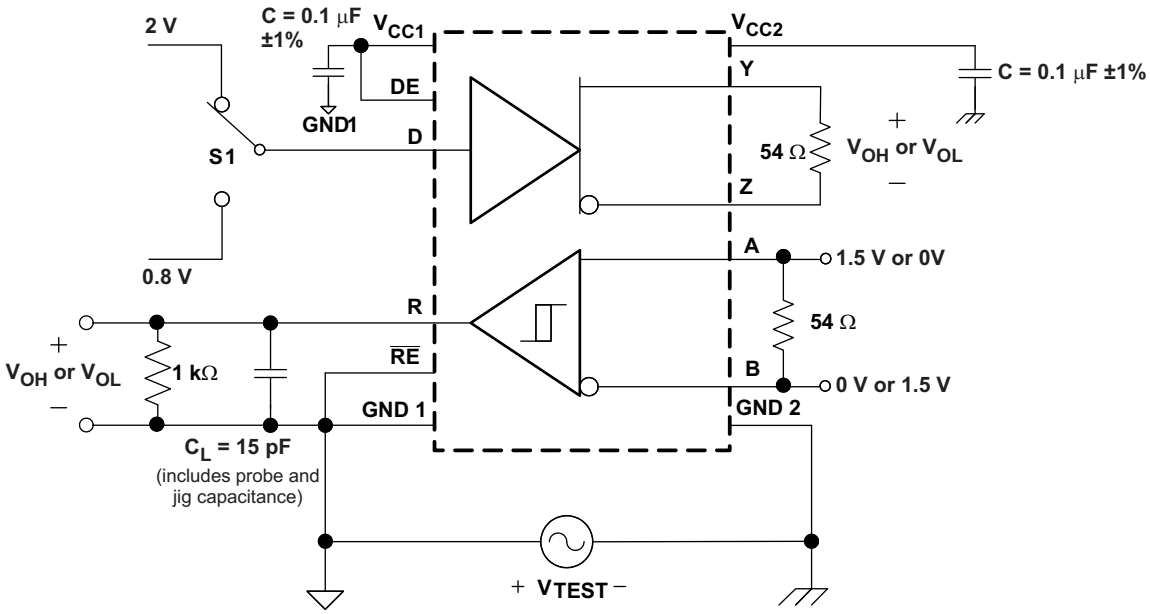


Figure 7-13. Full-Duplex Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

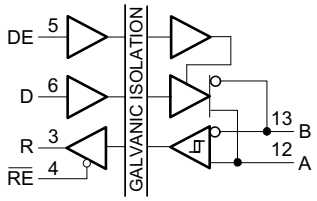
The ISO15 and ISO15M are isolated half-duplex differential line drivers and receivers while the ISO35 and ISO35M are isolated full-duplex differential line transceivers for TIA/EIA 485/422 applications. They are rated to provide galvanic isolation of up to 2500 V_{rms} for 60 sec as per the standard. They have active-high driver enables and active-low receiver enables to control the data flow.

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} – V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

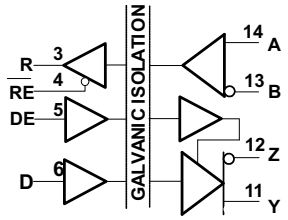
When the receiver enable pin, RE, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and less than the negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate. When RE is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

8.2 Functional Block Diagrams

ISO15x



ISO35x



8.3 Device Functional Modes

Table 8-1. Driver Function Table(2)

V_{CC1}	V_{CC2}	INPUT (D)	ENABLE INPUT (DE)	OUTPUTS(1)	
				Y / A	Z / B
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Hi-Z	Hi-Z
PU	PU	X	OPEN	Hi-Z	Hi-Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Hi-Z	Hi-Z
PU	PD	X	X	Hi-Z	Hi-Z

Table 8-1. Driver Function Table(2) (continued)

V_{CC1}	V_{CC2}	INPUT (D)	ENABLE INPUT (DE)	OUTPUTS(1)	
				Y / A	Z / B
PD	PD	X	X	Hi-Z	Hi-Z

(1) Driver output pins are Y and Z for full-duplex devices and A & B for half-duplex devices.
(2) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (off)

Table 8-2. Receiver Function Table(1)

V_{CC1}	V_{CC2}	DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
PU	PU	$-0.01\ V \le V_{ID}$	L	H
PU	PU	$-0.2\ V < V_{ID} < -0.01\ V$	L	?
PU	PU	$V_{ID} \le -0.2\ V$	L	L
PU	PU	X	H	Hi-Z
PU	PU	X	OPEN	Hi-Z
PU	PU	Open circuit	L	H
PU	PU	Short Circuit	L	H
PU	PU	Idle (terminated) bus	L	H
PD	PU	X	X	Hi-Z
PU	PD	X	L	H

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (off), ? = Indeterminate

8.3.1 Device I/O Schematics

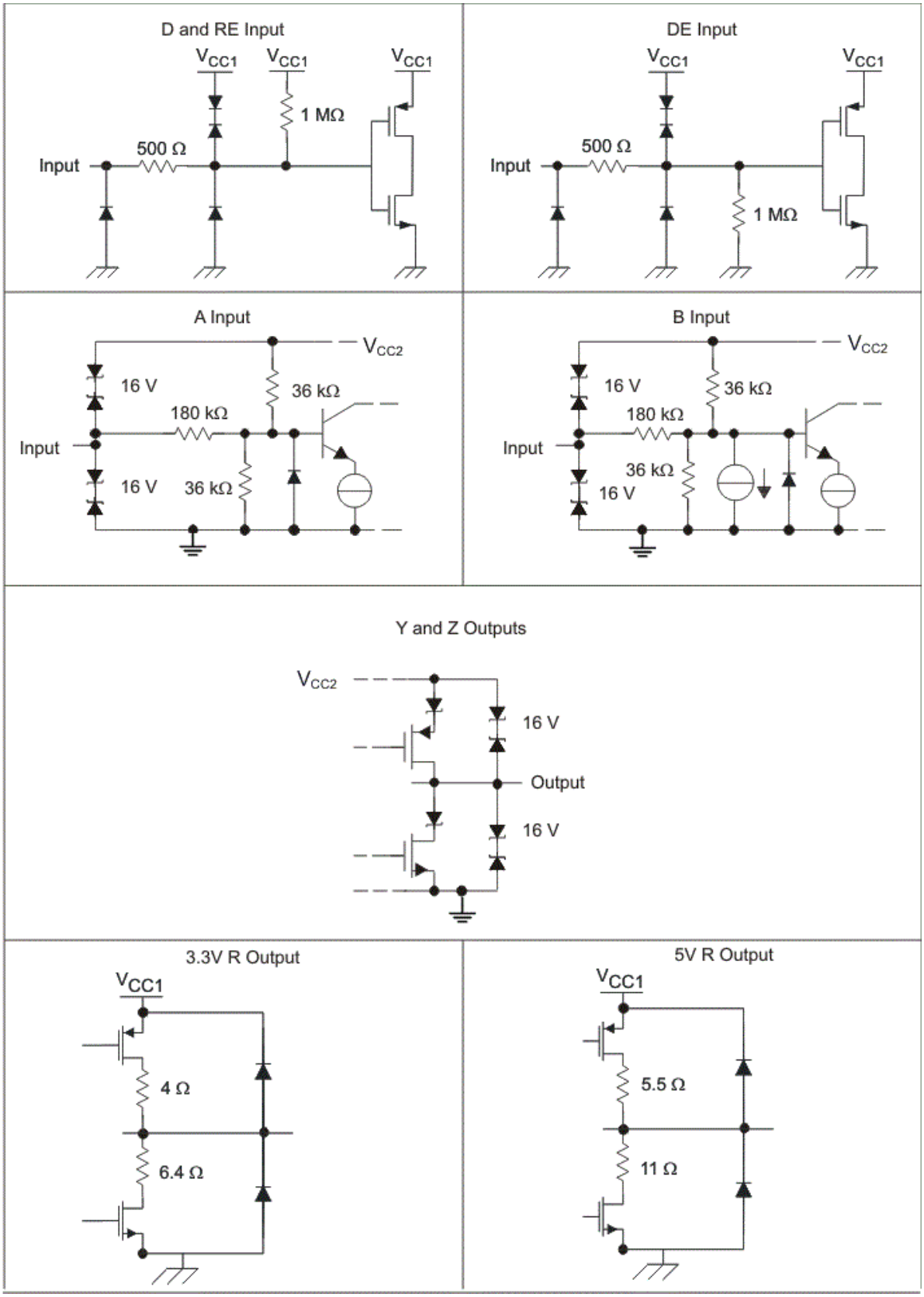


Figure 8-1. Device I/O Schematics

9 Application and Implementation

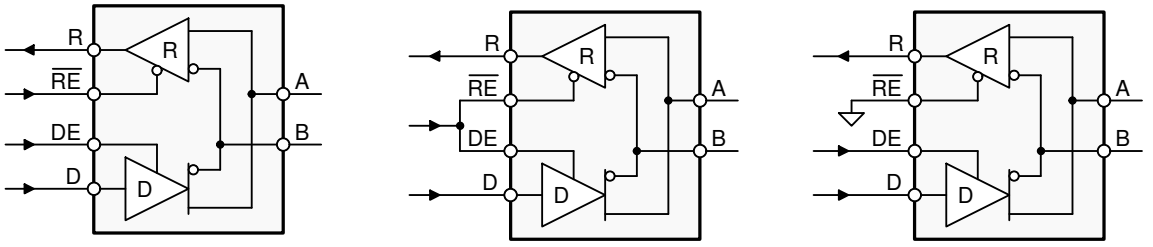
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The ISO15x and ISO35x family consists of RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. For half-duplex transmission there is only one pair which shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor, R(T), whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

9.2 Typical Application



a) Independent driver and receiver enable signals

b) Combined enable signals for use as directional control pin

c) Receiver always on

Figure 9-1. Half-Duplex Transceiver Configurations

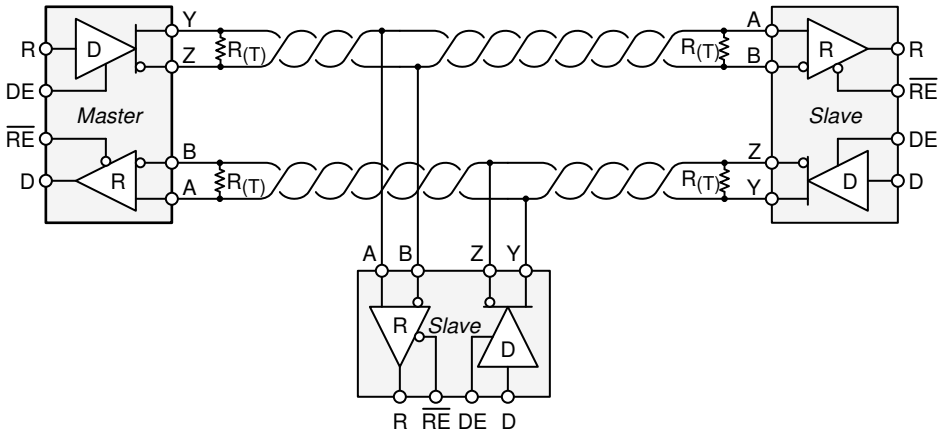


Figure 9-2. Typical RS-485 Network With Full-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

Table 9-1. Design Parameters

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

9.2.2 Detailed Design Procedure

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver. The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because these devices consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

9.2.3 Application Curve

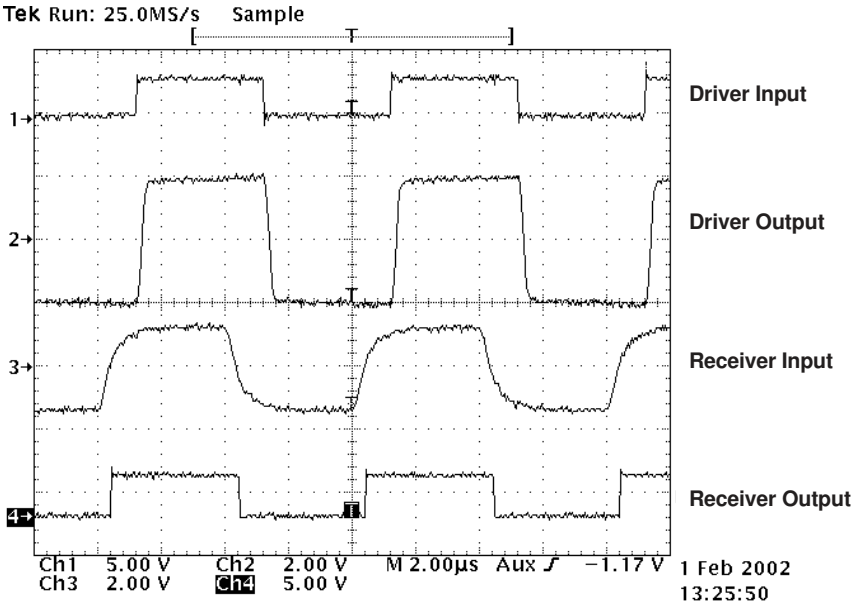


Figure 9-3. Typical Input and Output Waveforms

Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 . For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

10 Layout

10.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, highfrequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 10-1).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating the board.
- Use VCC and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC-pins of transceiver, UART, controller ICs on the board (see Figure 10-1).
- Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via-inductance (see Figure 10-1).
- Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in theses lines during transient events (see Figure 10-1).
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up (see Figure 10-1).
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Note

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

10.2 Layout Example

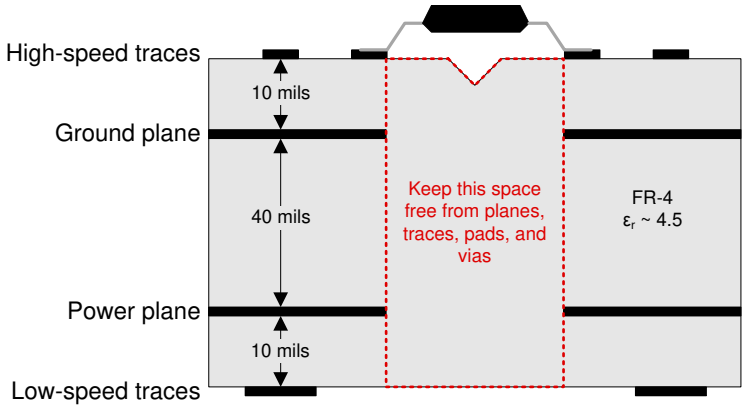


Figure 10-1. Recommended Layer Stack

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide* data sheet
- Texas Instruments, *Transformer Driver for Isolated Power Supplies* application report
- Texas Instruments, *Isolation Gloassary* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO15DW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15	
ISO15DWG4	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15	
ISO15DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15	Samples
ISO15MDW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO15M	
ISO15MDWR	LIFEBUY	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO15M	
ISO35DW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35	
ISO35DWG4	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35	
ISO35DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35	Samples
ISO35MDW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO35M	
ISO35MDWR	LIFEBUY	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO35M	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

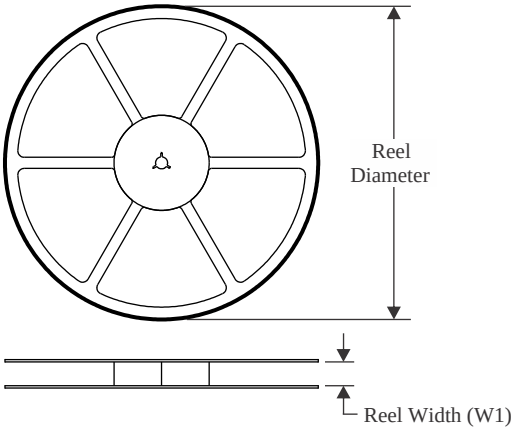
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

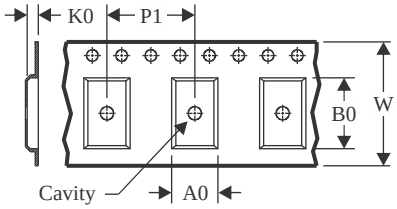
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

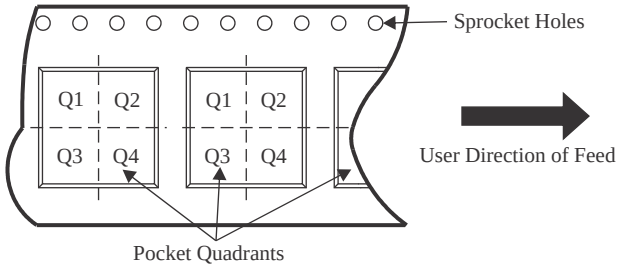


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

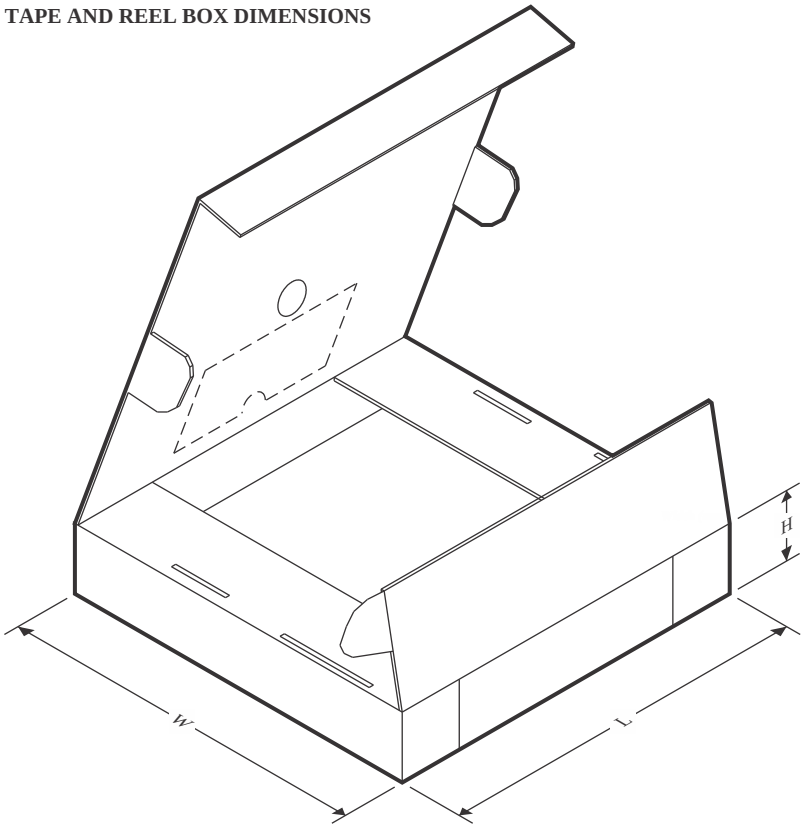
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO15DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO15MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO35DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO35MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

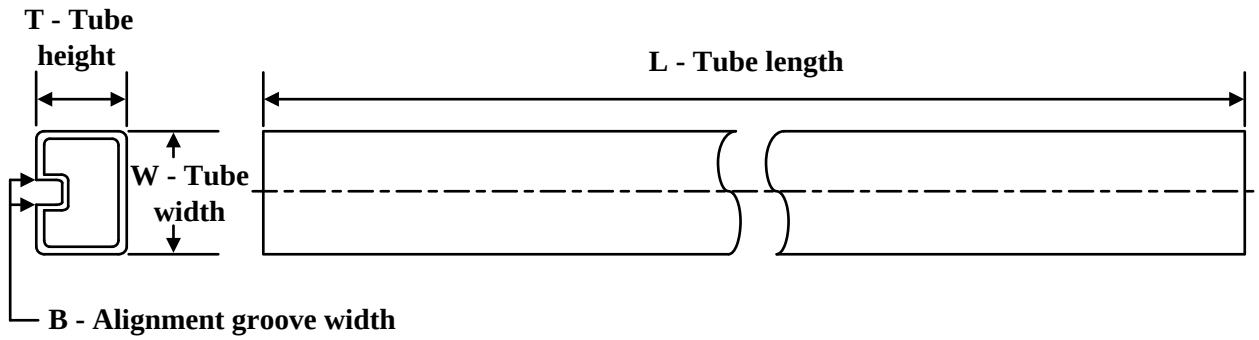
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO15DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO15MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO35DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO35MDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO15DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO15DWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO15MDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO35DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO35DWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO35MDW	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

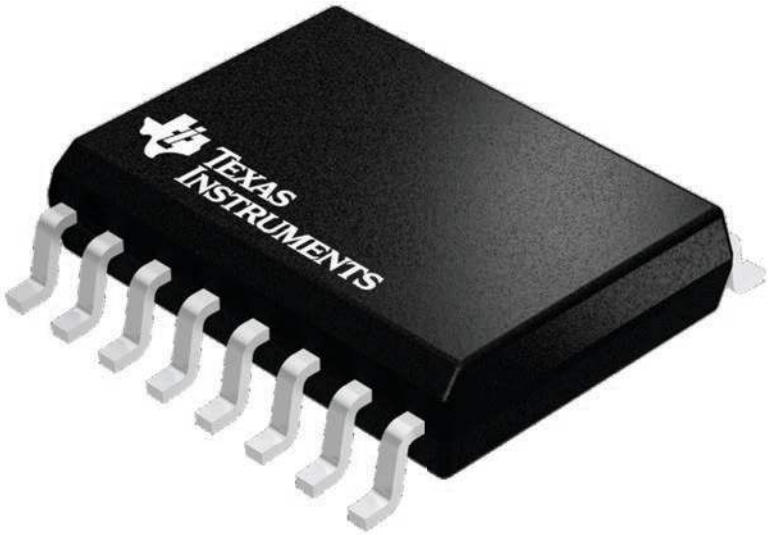
DW 16

SOIC - 2.65 mm max height

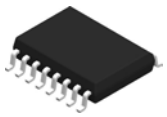
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

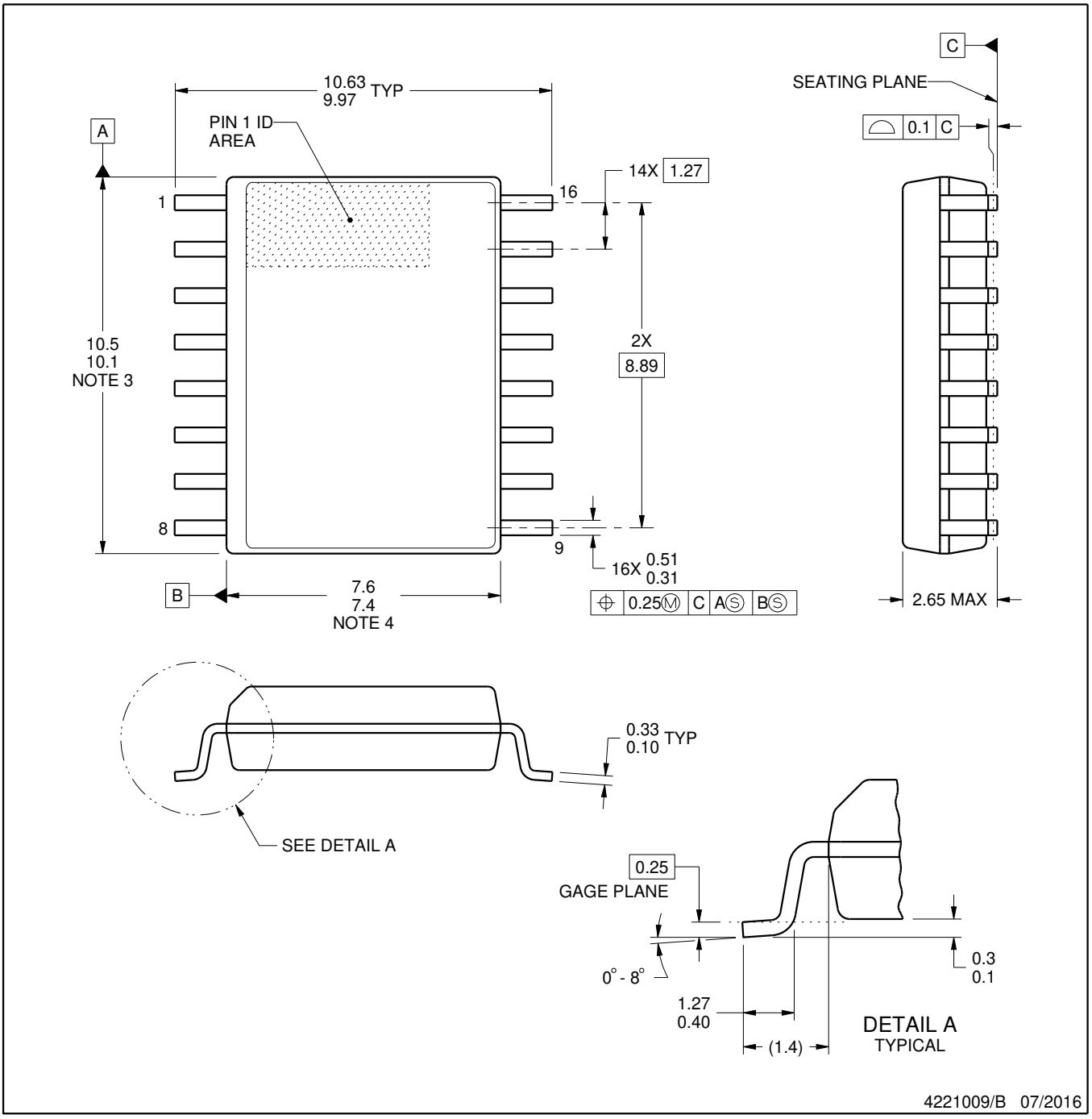


PACKAGE OUTLINE

DW0016B

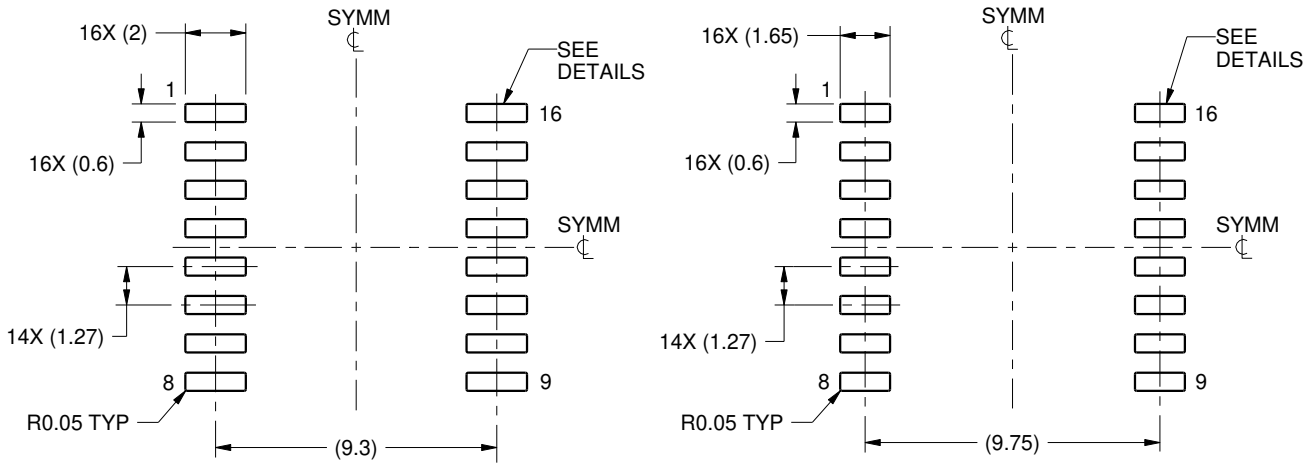
SOIC - 2.65 mm max height

SOIC

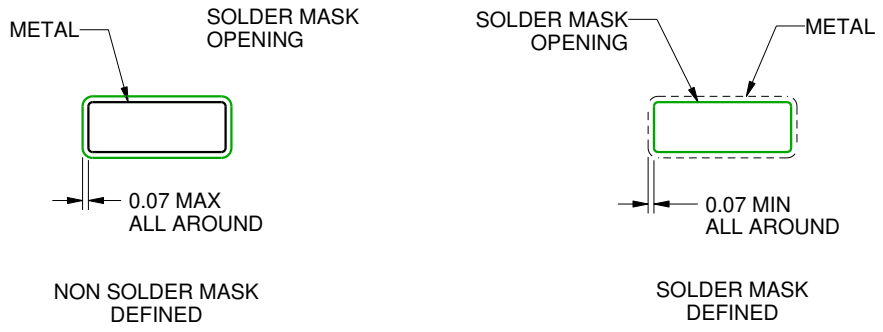


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

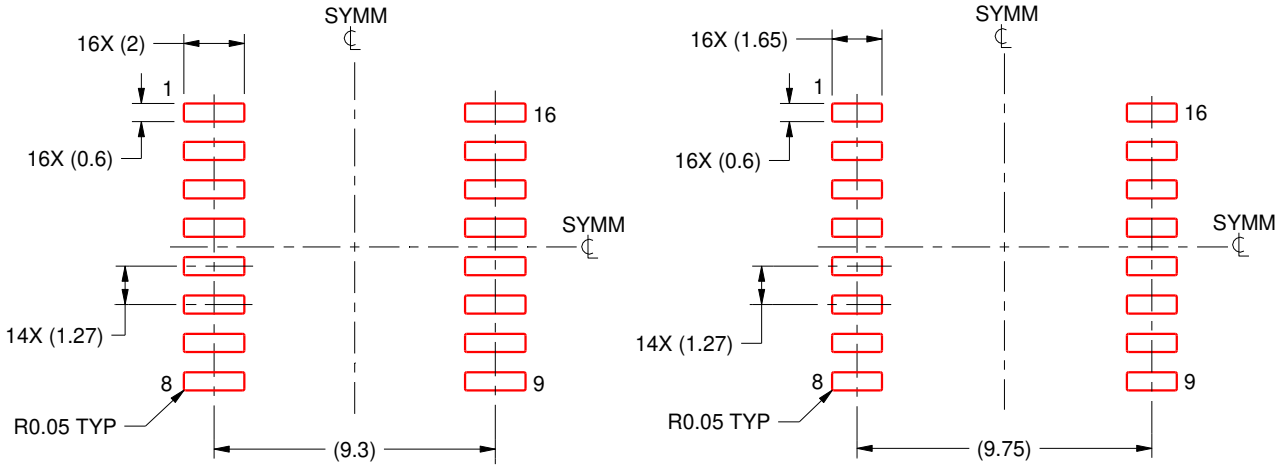
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265