Title	***Reference Design Report for 4.5 W Power Factor Corrected LED Driver (Non-Isolated Buck Boost) Using LinkSwitch^{TM}-PL LNK458KG***
Specification	85 VAC – 135 VAC Input; 35 V, 130 mA Output
Application	LED Driver for E17 Lamp Replacement
Author	Applications Engineering Department
Document Number	RDR-271
Date	June 8, 2011
Revision	1.0

Summary and Features

- Single-stage power factor corrected and accurate constant current (CC) output
- Low cost, low component count and small PCB footprint solution
- Highly energy efficient, >85 % at 115 VAC input
- Superior performance and end user experience
- Fast start-up time (<300 ms) – no perceptible delay
- Integrated protection and reliability features
  - Single shot no-load protection / output short-circuit protected with auto-recovery
  - Auto-recovering thermal shutdown with large hysteresis protects both components and PCB
  - No damage during brown-out conditions
- PF >0.95 at 115 VAC
- Meets EN55015 conducted EMI
- %A THD <15% at 115 VAC
- Meets IEC ring wave, differential line surge and EN55015 conducted EMI
- No potting required up to 90 ºC internal ambient

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Table of Contents

Important Note:
Although this board is designed to satisfy safety requirements for non-isolated LED driver, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a non-isolated LED driver (power supply) utilizing a LNK458KG from the LinkSwitch-PL family of devices.

The RD-271 provides a single constant current output of 130 mA over an LED string voltage of 35 V.

The board was optimized to operate over the low AC input voltage range (85 VAC to 135 VAC, 47 Hz to 63 Hz). LinkSwitch-PL based designs provide a high power factor (>0.9) meeting current international requirements.

The form factor of the board was chosen to meet the requirements for standard pear shaped (E17) LED replacement lamps. The output is non-isolated and requires the mechanical design of the enclosure to isolate the output of the supply and the LED load from the user.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

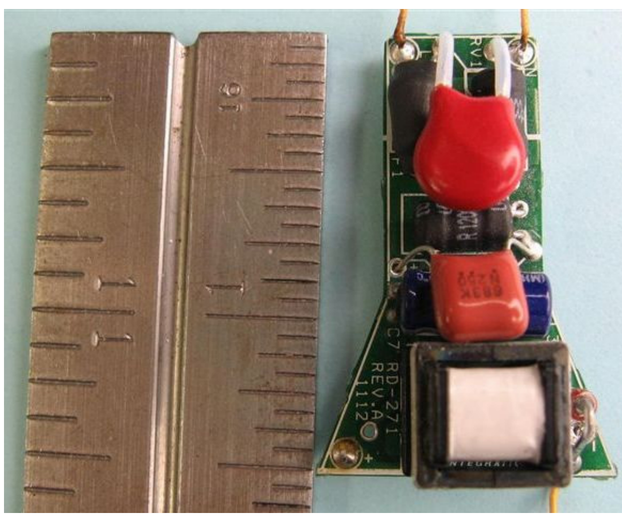

Figure 1 – Size of Populated Circuit Board Photograph.

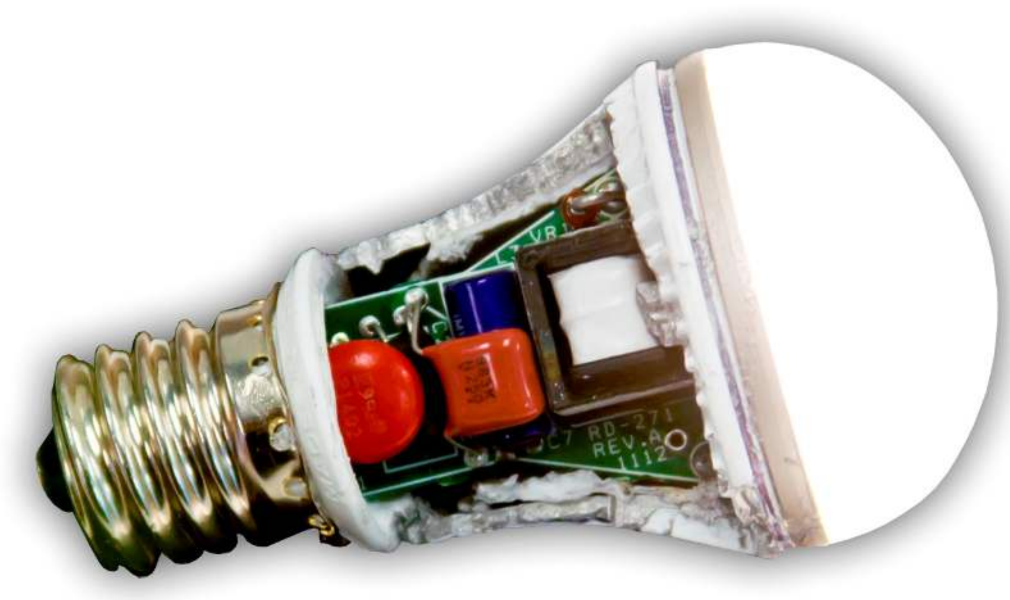

Figure 2 – Populated Circuit Board Retrofitted Inside A17 Bulb.

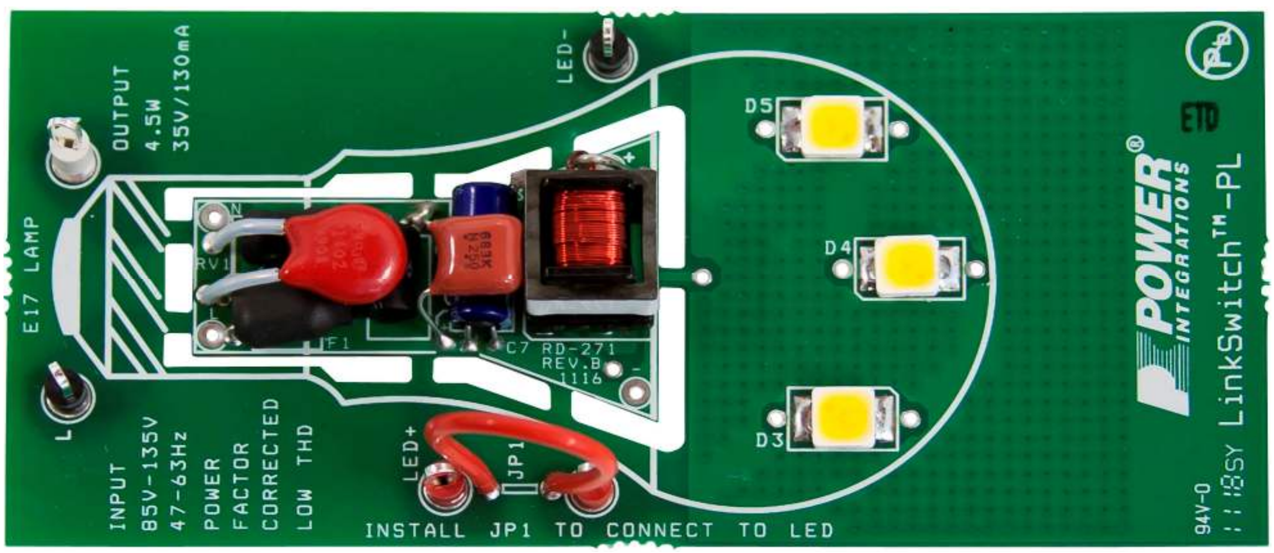

Figure 3 – Reference Design Test Board with LED Load for Ease of Testing, Top.

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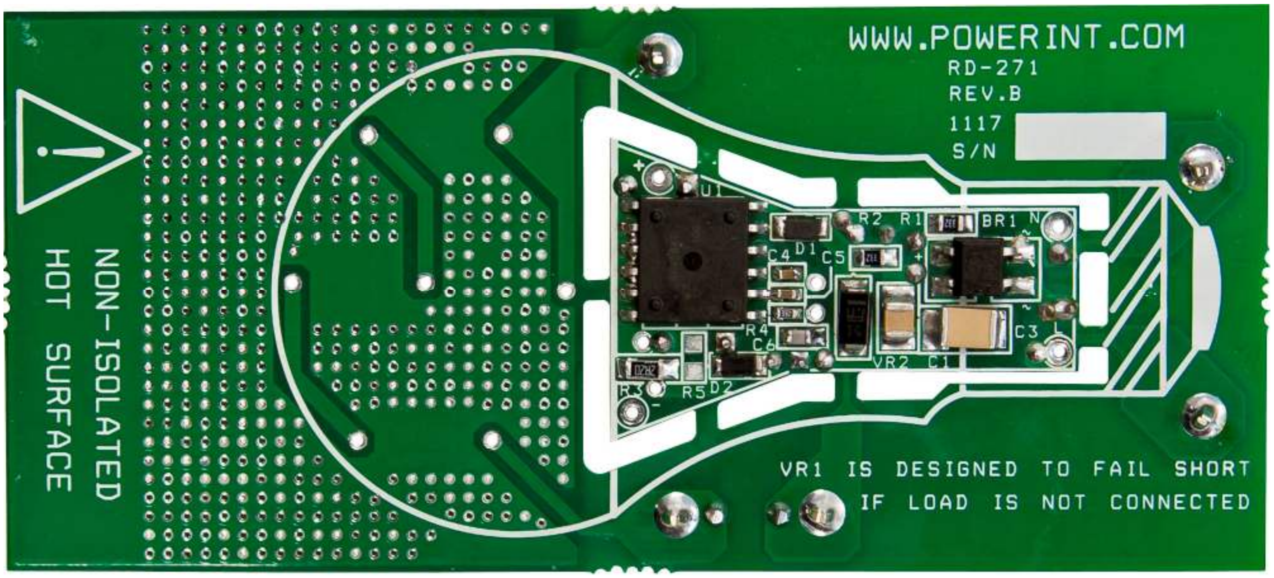

Figure 4 – Reference Design Test Board with LED Load for Ease of Testing, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		135	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
Power Factor >		0.9				At any line input voltage
%ATHD <				15		
Output						
Output Voltage	V_{OUT}		35		V	
Output Current	I_{OUT}	120	130	140	A	
Total Output Power						
Continuous Output Power	P_{OUT}		4.5		W	
Efficiency						
Nominal	η		85		%	Measured at P_{OUT} 25^{o}C at 115 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55015				
Line Surge (OPTION 1: VR2 not populated) Differential Mode (L1-L2)		0.5	>0.7		kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω
Line Surge (OPTION 2: VR2 populated-TVS) Differential Mode (L1-L2)		1	>1.5		kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Above 1.7 kV, F1 opens
Ring Wave (100 kHz) Differential Mode (L1-L2)		2.5	>3		kV	2 Ω short circuit Series Impedance
Internal Ambient Temperature	T_{AMB}	-40		90	^{o}C	Board level, free convection, sea level

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3 Schematic

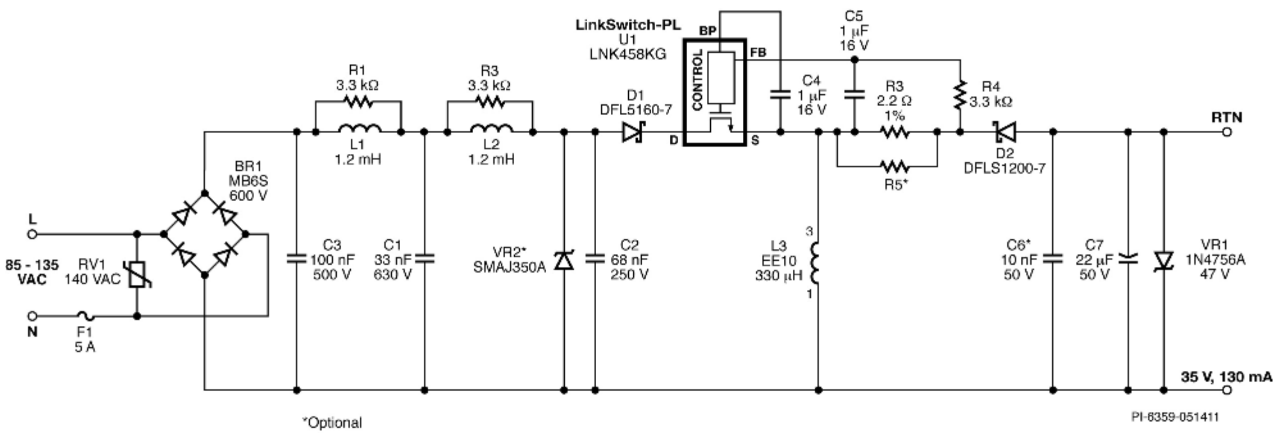

Figure 5 – Schematic. Remove VR2 for Differential Line Surge Requirement of 500 V Only.

4 Circuit Description

The LinkSwitch-PL (U1) is a highly integrated primary side controller intended for use in LED driver applications. The LinkSwitch-PL provides high power factor in a single-stage conversion topology while regulating the output current in a wide range of input (85 VAC - 135 VAC) and output voltage variations typical in LED driver application environment. All of the control circuitry responsible for these functions plus a high-voltage power MOSFET is incorporated into the device.

4.1 Input EMI Filtering

Fuse F1 provides protection against component failure. A fast 5 A rating (this being relatively high) was needed to prevent false opening during line surges. The maximum input voltage is clamped by RV1 and by VR2 (TVS) during differential line surges. Zener diode VR2 can be removed for a differential line surge requirement of ≤500 V.

The AC input is full wave rectified by BR1 (vs. half wave) to achieve good power factor and THD.

Capacitor C1, C2, C3 and differential choke L1 and L2 perform EMI filtering while the limited total capacitance maintains high power factor. This input 2-π filter network plus the frequency jittering feature of LinkSwitch-PL allows compliance to Class B emission limits. Resistor R1 and R2 were used to damp the resonance of the EMI filter, preventing peaks in the EMI spectrum.

- Inductor L1 and L2 are positioned after the bridge to avoid an imbalance in the EMI scan between line and neutral. This gives also leeway to use small high-voltage ceramic capacitors in the input filter.
- Capacitor C2 is a film capacitor to achieve more than 10 dBμV design margin. It may be replaced by X7R high-voltage ceramic capacitor if EMI design margin requirement is relaxed (<4 dBμV margin)

4.2 Buck Boost using LinkSwitch-PL

The buck boost power train is composed of U1 (power switch + control), D2 (free-wheeling diode), C6 and C7 (output capacitor), and L3 (inductor). Diode D1 was used to prevent negative voltage appearing across the drain-source of U1 especially near the zero-crossing of the input voltage. The bypass capacitor C4 provides the internal supply for the device when the power MOSFET is on.

- Diode D1 and D2 are low drop diodes (Schottky) to maximize efficiency.
- Inductor L3 winding construction and wire gauge are optimized to minimize inter-winding capacitance and reduces AC losses.

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4.3 Output Feedback

The output current feedback is sensed on the voltage drop across R3 and then filtered by a low pass filter, R4 and C5, to keep the LinkSwitch-PL operating point such that the average FEEDBACK (FB) pin voltage is 290 mV steady-state.

- Resistor R5 is provisioned in parallel with R3 to allow centering of the output current.

4.4 Disconnected Load Protection

The system is protected by VR1 if the load is not connected in order to avoid catastrophic failure of C7 (output capacitor). Zener diode VR1 will short the output it the load is not connected; this protection is not auto-recovering. Replace VR1 if this occurs in order to reuse the LED driver. Note that at the system level the LED load is always connected. If the system will be potted or enclosed tightly, VR1 might not be required.

Replace VR1 with an SCR clamp circuit it auto-recovery is required.

4.5 Reference Design Kit

The reference design is mounted with LED load as a complete kit. The load is for illustration and can be operated at 25 ºC ambient maximum only. A loop wire can be used for monitoring the output current via current probe or clamp.

The board can be dismantled to fit to common E17 lamps and for higher operating temperature test condition.

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5 PCB Layout

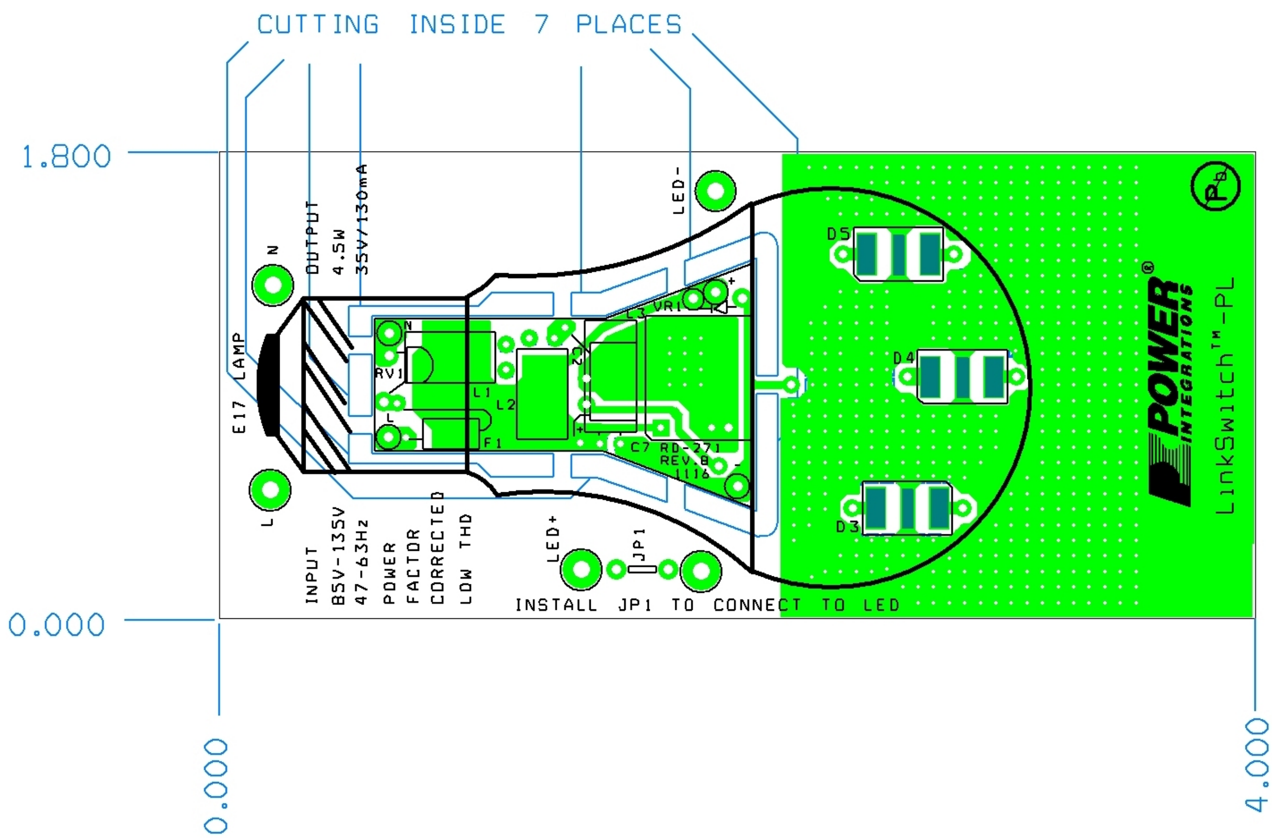

Figure 6 – Top Printed Circuit Layout.

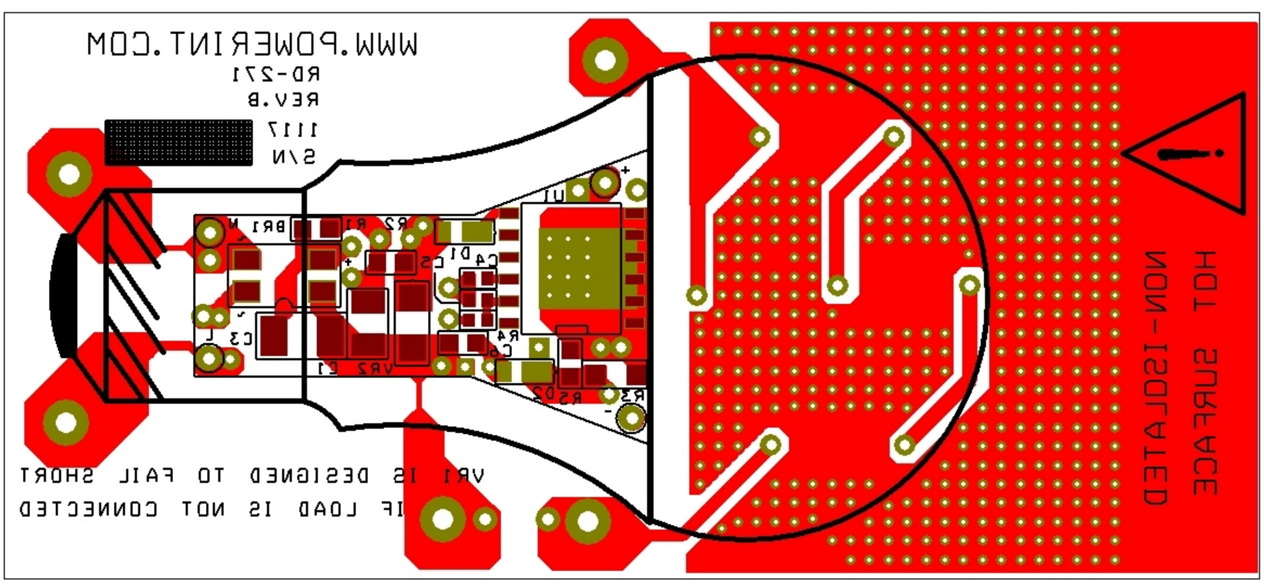

Figure 7 – Bottom Printed Circuit Layout.

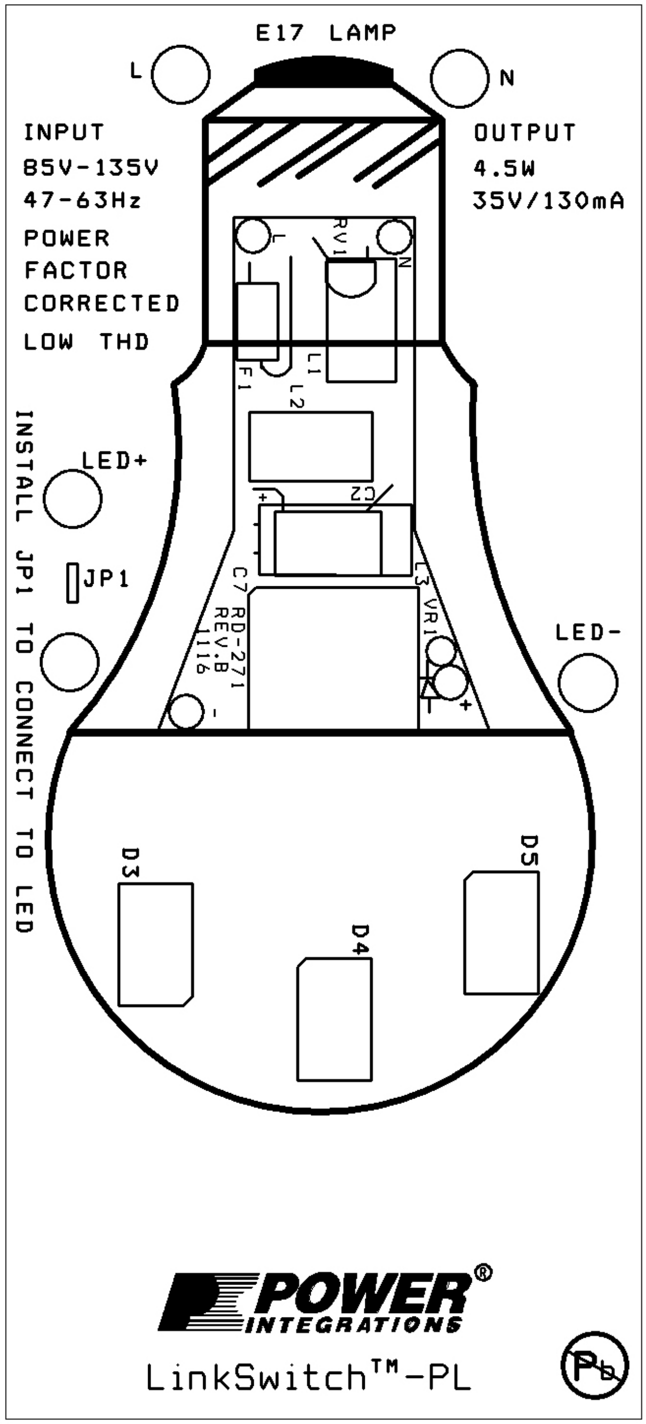

Figure 8 – Top Printed Circuit Layout of the Kit.

Note: Operate LED loads at 25ºC ambient only. Remove LED driver from the kit to test at higher ambient temperature. Make sure LED is connected before power-up to avoid fusing the non-resettable OVP protection (replace VR1 to reset the driver).

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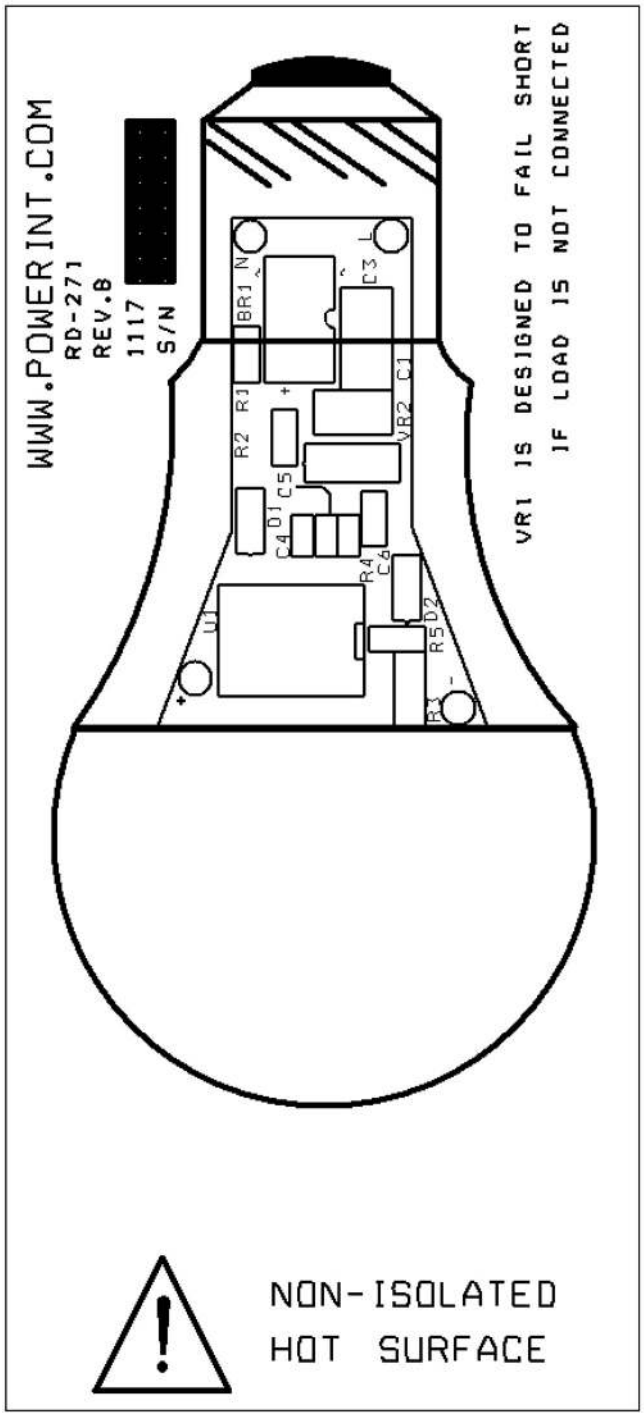

Figure 9 – Bottom Printed Circuit Layout of the Kit.

Note: Operate LED loads at 25ºC ambient only. Remove LED driver from the kit to test at higher ambient temperature. Make sure LED is connected before power-up to avoid fusing the non-resettable OVP protection (replace VR1 to reset the driver).

6 Bill of Materials

The table below is divided into two sections namely: reference design BOM and additional parts for load.

6.1 Lamp Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial
2	1	C1	33 nF, 630 V, Ceramic, X7R, 1210	GRM32DR72J333KW01L	Murata
3	1	C2	68 nF, 250 V, Polyester Film	ECQ-E2683KB	Panasonic
4	1	C3	100 nF, 500 V, Ceramic, X7R, 1812	VJ1812Y104KXEAT	Vishay
5	2	C4 C5	1 μF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
6	1	C7	22 μF, 50 V, Electrolytic, Low ESR, 900 mΩ, (5 x 11.5)	ELXZ500ELL220MEB5D	Nippon Chemi-Con
7	1	D1	60 V, 1 A, Diode Schottky, PWRDI 123	DFLS160-7	Diodes, Inc
8	1	D2	200 V, 1 A, Diode Schottky 1 A 200 V PWRDI 123	DFLS1200-7	Diodes, Inc
9	1	F1	5 A, 250V, Fast, Microfuse, Axial	0263005.MXL	Littelfuse
10	2	L1 L2	1200 μH, 0.018 A	RL-5480-1-1200	Renco
11	1	L3	330 μH EE10 inductor	RLPI-1002 SNX-R1577	Renco Santronics
12	2	R1 R2	3.3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ332V	Panasonic
13	1	R3	2.2 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2204V	Panasonic
14	1	R4	3.3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ332V	Panasonic
15	1	RV1	140 V, 12 J, 7 mm, RADIAL	V140LA2P	Littlefuse
16	1	U1	LinkSwitch-PL, eSOP-12P	LNK458KG	Power Integrations
17	1	VR1	47 V, 5%, 1 W, DO-41	1N4756A-T	Diodes Inc
18	1	VR2	350 V, 400 W, 5%, DO214AC (SMA)	SMAJ350A	LittelFuse

6.2 LED Load Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	2	+LED LED+	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
2	3	D3 D4 D5	LED, SMD, 87.4 lm, Cree, Warm-White	MX3SWT-A1-0000-000AE7	Cree
3	1	JP1	Wire Jumper, Insulated, 24 AWG, 2.2 in	C2003A-12-02	Gen Cable
4	2	LINE	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
5	1	NEUT	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
6	1 ml	Glue	Hot Melt Adhesive V0 5/8”X2)	3748 Vo-TC	3M

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7 Inductor Specification

7.1 *Electrical Diagram*

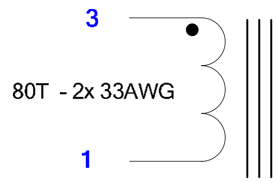

Figure 10 – Inductor Electrical Diagram.

7.2 *Electrical Specifications*

Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	330 µH ±10%

7.3 *Materials*

Item	Description
[1]	Core: EE10/PC40
[2]	Bobbin: EE10, Horizontal, 8 pins, (4/4), Taiwan Shulin Enterprise Co., Ltd. or Kunshan Fengshunhe Electronics Co., Ltd Equivalent
[3]	Magnet Wire: 2 X #33 AWG
[4]	Loctite Super Glue Control Gel

7.4 Inductor Build Diagram

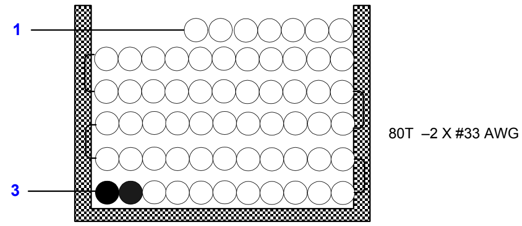

Figure 11 – Inductor Build Diagram.

7.5 Inductor Construction

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left side (see illustration). Winding direction as shown is counter-clockwise.
WD1	Start at pin 3. Wind 80 turns of item [3]. Continue winding up to 5 ½ layers and terminate it at pin 1.
Finish	Grind the core to get 330 µH, ±10%. Apply tape to secure both cores. Cut pins 2, 4, 5, 6, 7 and 8. Apply adhesive item [4] to core and bobbin to prevent core from any movement (see illustration).

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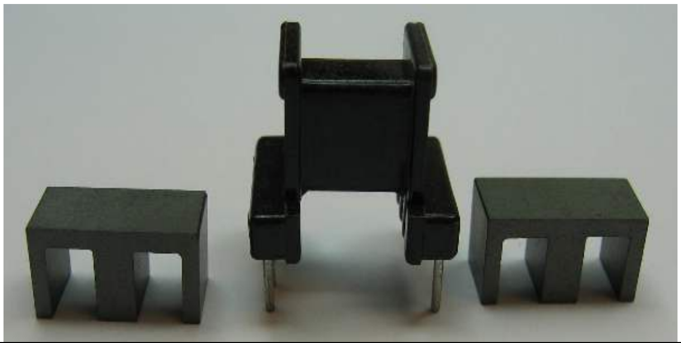
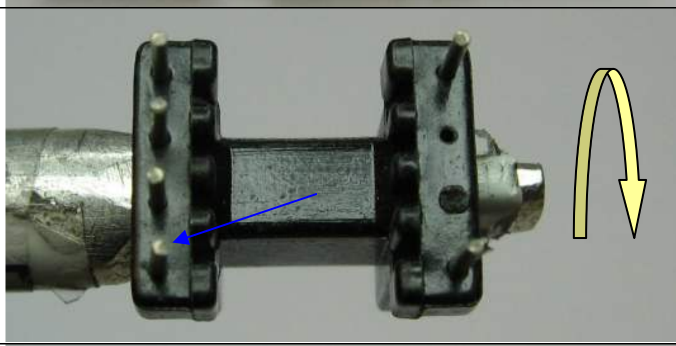
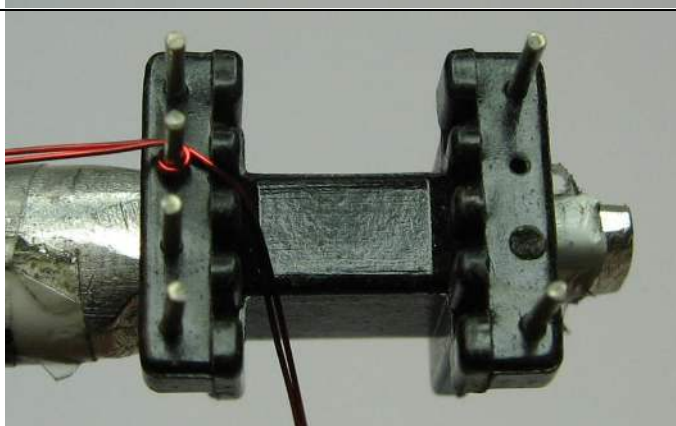
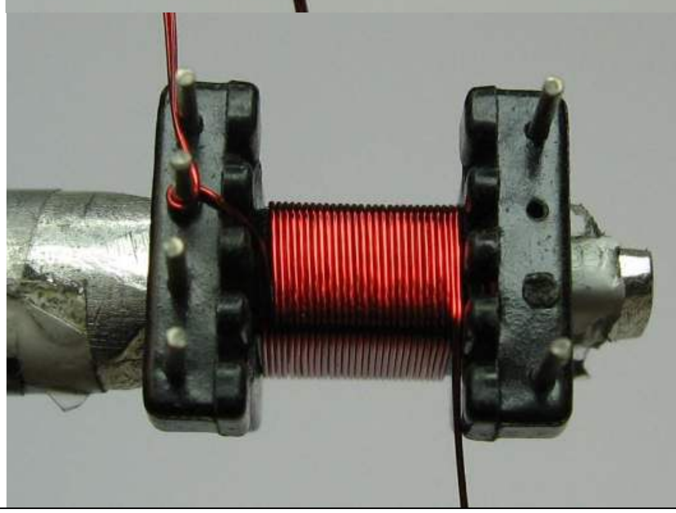
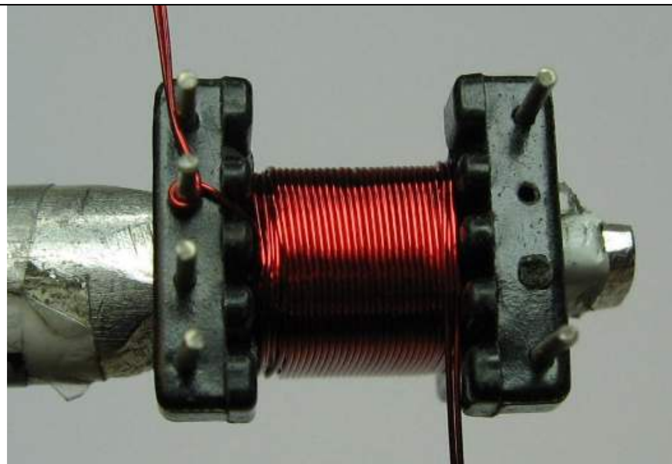
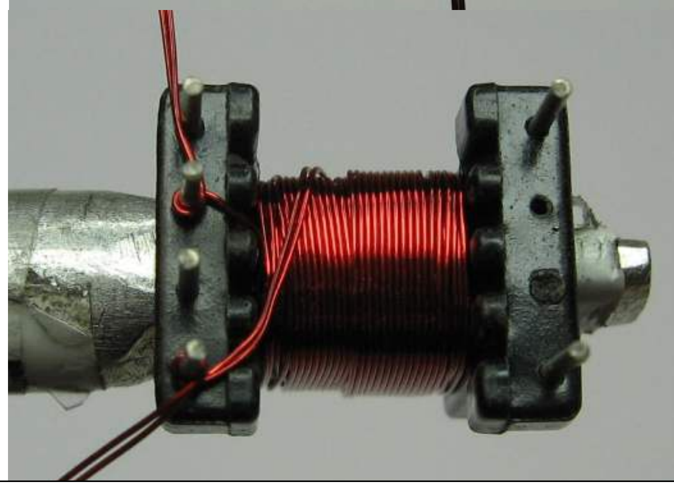
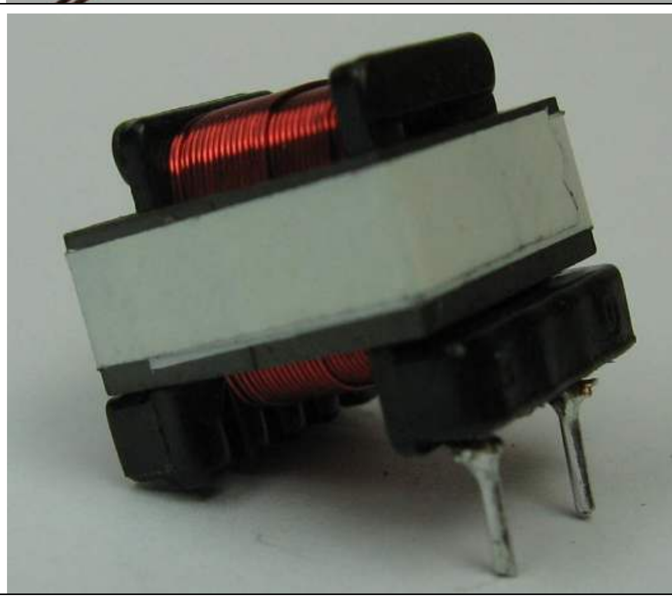
8 Inductor Illustration

Bobbin Preparation		
General Note		For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left side (see illustration). Winding direction as shown is counter-clockwise.
WD1	 	Start at pin 3. Wind 80 turns of item [3]. Continue winding up to 5 ½ layers and terminate it at pin 1.

	 	
Finish		Grind the core to get 330 μH, ±10%. Apply tape to secure both cores. Cut pins 2, 4, 5, 6, 7 and 8. Apply adhesive item [4] to core and bobbin to prevent core from any movement (see illustration).

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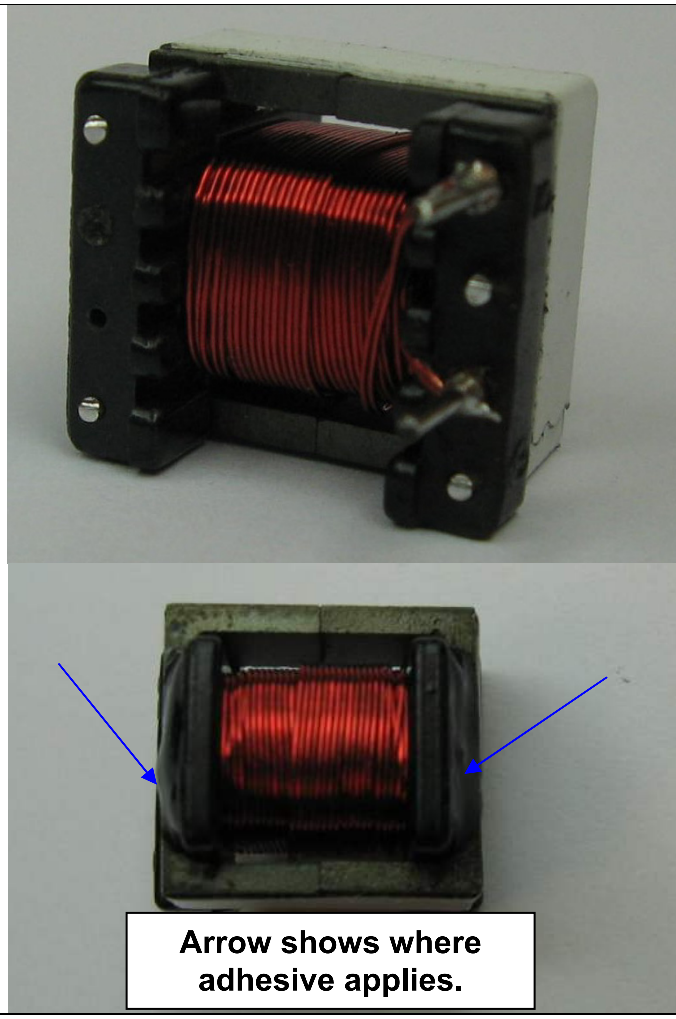

Figure 12 – Inductor Assembly.

9 Inductor Design Spreadsheet

Power Supply		INFO	OUTPUT	UNIT	LinkSwitch-PL Buck-boost Inductor Design Spreadsheet
VACMIN	85		85	V	Minimum AC input voltage
VACNOM	115		115	V	Nominal AC input voltage
VACMAX	132		132	V	Maximum AC input voltage
FL	60		60	Hz	Minimum line frequency
VO_MIN	30.00		30.0	V	Minimum output voltage tolerance
VO_NOM	35.00		35.00	V	Nominal Output Voltage
VO_MAX	38.00		38.00	V	Maximum output voltage tolerance
IO	0.130		0.130	A	Average output current specification
n	0.85		0.850	%/100	Total power supply efficiency
Z			0.5		Loss allocation factor
Enclosure	Open Frame		Open Frame		Enclosure selections determines thermal conditions and maximum power
PO			4.55	W	Total output power
VD	0.40		0.4	V	Output diode forward voltage drop
LinkSwitch-PL DESIGN VARIABLES					
Device	LNK458		LNK458		Chosen LinkSwitch-PL Device
TON			1.67	us	Expected on-time of MOSFET at low line and PO
FSW			88.9	kHz	Expected switching frequency at low line and PO
Duty Cycle			14.8	%	Expected operating duty cycle at low line and PO
VDRAIN			245	V	Estimated worst case drain voltage at VACMAX and VO_MAX
IRMS			0.129	A	Nominal RMS current through the switch
IPK			0.938	A	Worst Case Peak current
ILIM_MIN			1.012	A	Minimum device current limit
KDP	1.25		1.25		Ratio between off-time of switch and reset time of core at VACNOM
Device	LNK458		LNK458		Chosen LinkSwitch-PL Device
LinkSwitch-PL EXTERNAL COMPONENT CALCULATIONS					
RSENSE			2.231	Ohms	Output current sense resistor
Standard RSENSE			2.21	Ohms	Closest 1% value for RSENSE
PSENSE			37.7	mW	Power dissipated by RSENSE
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE10		EE10		Core Type
Core Part Number			Custom		Core Part Number (if Available)
Bobbin Part Number			Custom		Bobbin Part Number (if available)
AE	12.10		12.10	mm^2	Core Effective Cross Sectional Area
LE	26.10		26.10	mm	Core Effective Path Length
AL	850		850	nH/T^2	Ungapped Core Effective Inductance
BW	6.00		6	mm	Bobbin Physical Winding Width
L	5		5		Number of winding layers
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			330.7	uH	Primary Inductance
LP Tolerance	5.00		5	%	Tolerance of Primary Inductance
N	80		80	Turns	Number of Turns

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ALG			52	nH/T^2	Gapped Core Effective Inductance
BM		*Info*	3205	Gauss	Reduce BM < 3000 G. Decrease BP (increase NP) or increase core size.
BAC			1603	Gauss	Worst case AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
BP		*Warning*	4620	Gauss	!!! Reduce peak flux density (BP < 3600 G) by increasing NP, selecting a bigger core or decreasing KDP; See note below
LG			0.294	mm	Gap Length (Lg > 0.1 mm)
BWE			30	mm	Effective Bobbin Width
L_IRMS			0.333	A	RMS Curren through the inductor
OD			0.38	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.32	mm	Bare conductor diameter
AWG			29	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			128	Cmils	Bare conductor effective area in circular mils
CMA			384	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Current Density (J)			5.19	A/mm^2	Inductor Winding Current density (3.8 < J < 9.75 A/mm^2)
Output Parameters					
IO			0.130	A	Expected Output Current
PIVS			42.2	V	Peak Inverse Voltage at VO_MAX on output diode

Note: Peak flux density is limited by slowly increasing the duty cycle of LinkSwitch-PL family during start-up.

10 Performance Data

All measurements performed at 25 ºC room temperature, 60 Hz input frequency otherwise specified.

10.1 Active Mode Efficiency

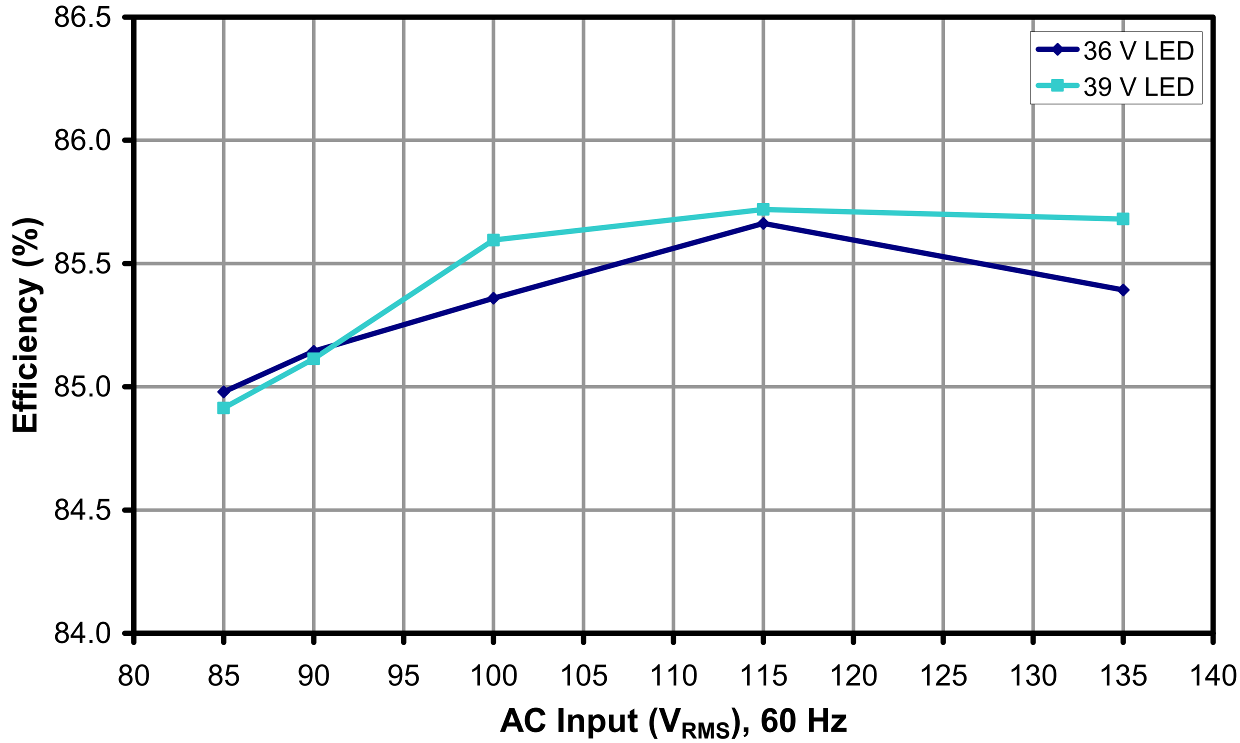

Figure 13 – Efficiency with Respect to AC Input Voltage.

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10.2 Line Regulation

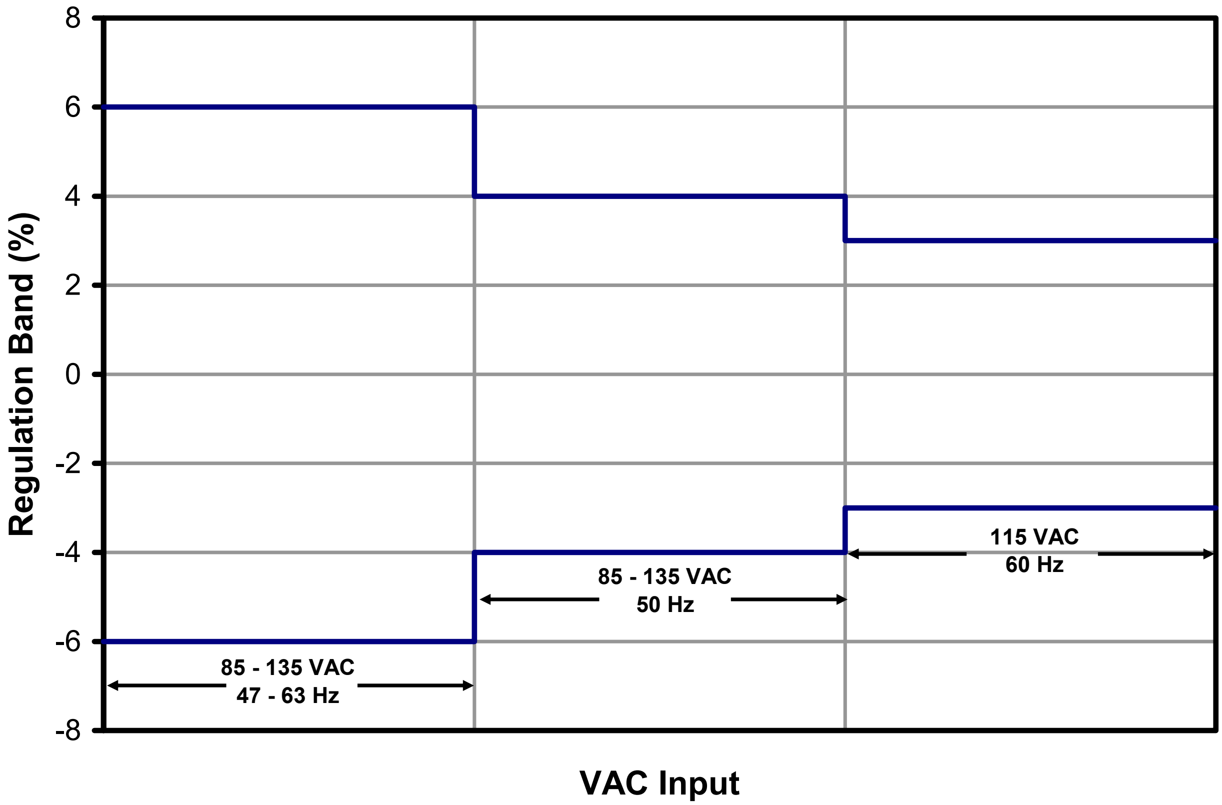

Figure 14 – Line Regulation, Room Temperature.

10.3 Power Factor

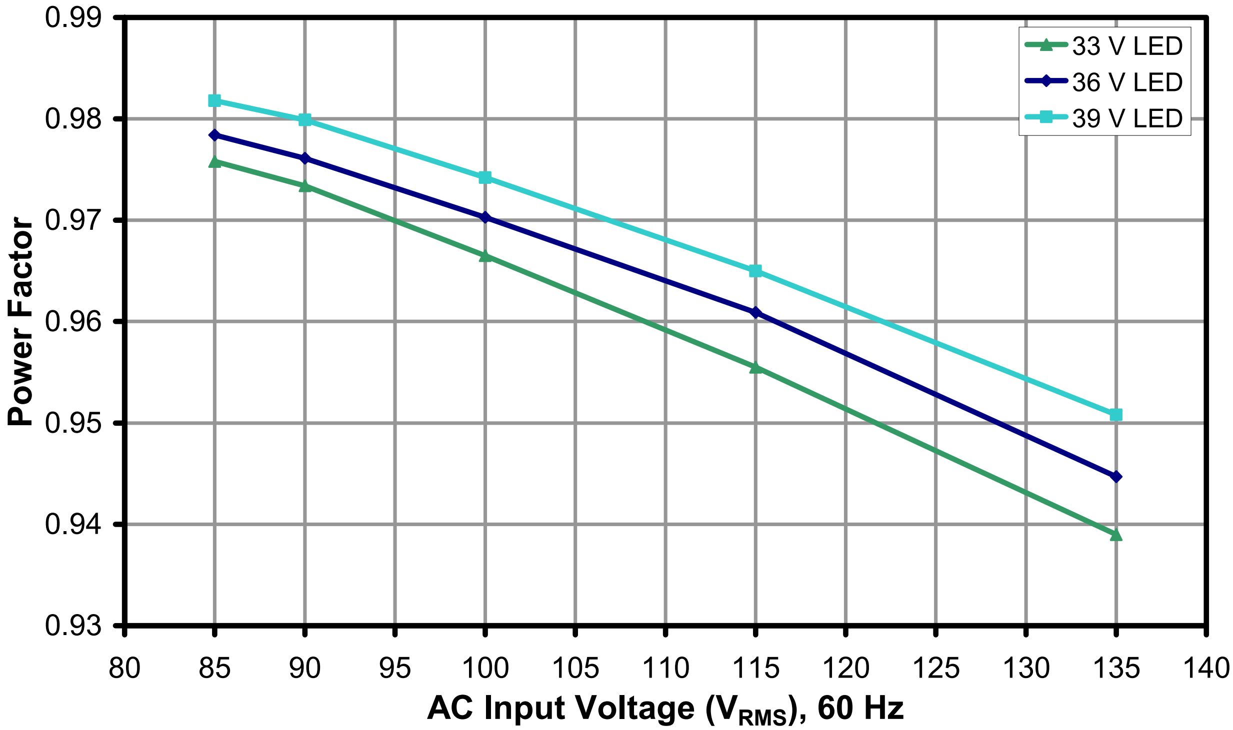

Figure 15 – High Power Factor within the Operating Range.

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10.4 %THD

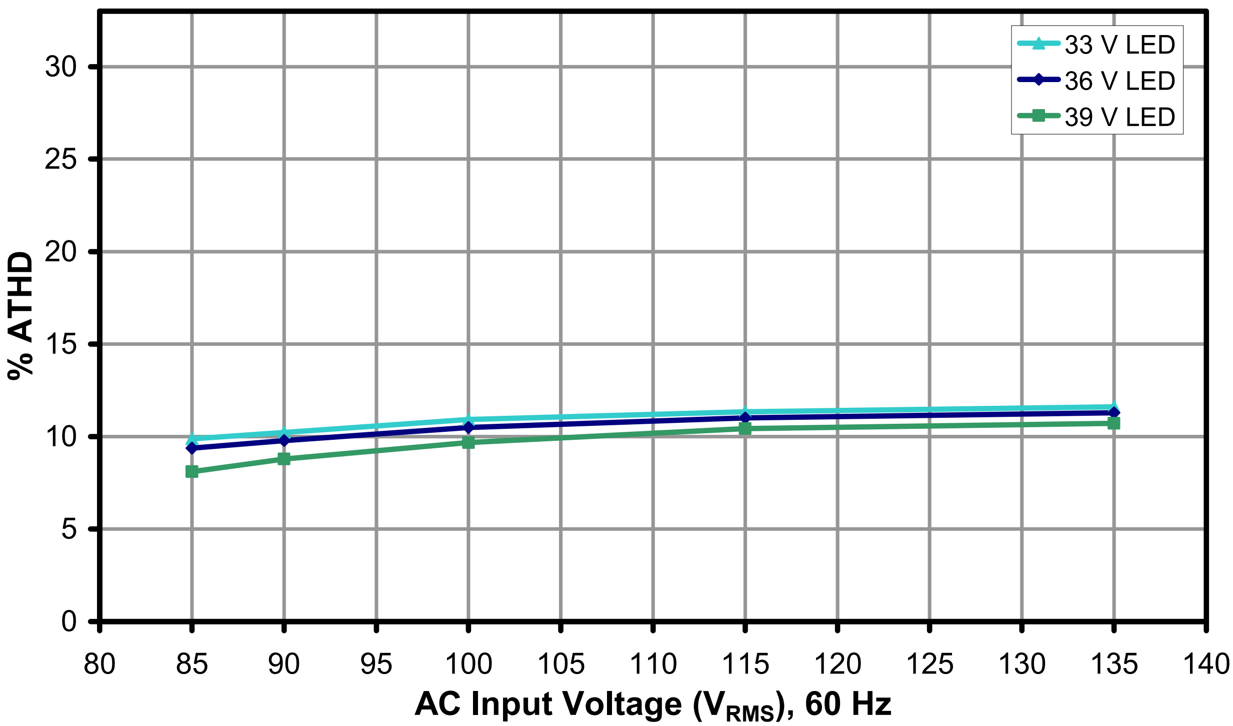

Figure 16 – Very Low %ATHD within the Operating Range.

10.5 Harmonic Measurements

VAC (V_{RMS})	Freq (Hz)	V (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)
115	**60**	**114.97**	**50.51**	**5.58000**
nth order	**mA content**	**Base Limit mA/W**	**Actual Limit**	**Remarks**
1	48.67			
3	1.38	3.40000	37.9440	Pass
5	1.67	1.90000	21.2040	Pass
7	2.09	1.00000	11.1600	Pass
9	2.20	0.50000	5.5800	Pass
11	2.36	0.35000	3.9060	Pass
13	1.82	0.29615	3.3051	Pass
15	1.67	0.25667	2.8644	Pass
17	1.00	0.22647	2.5274	Pass
19	0.79	0.20263	2.2614	Pass
21	0.40	0.18333	2.0460	Pass
23	0.10	0.16739	1.8681	Pass
25	0.24	0.15400	1.7186	Pass
27	0.24	0.14259	1.5913	Pass
29	0.49	0.13276	1.4816	Pass
31	0.33	0.12419	1.3860	Pass
33	0.18	0.11667	1.3020	Pass
35	0.19	0.11000	1.2276	Pass
38	0.10	0.10405	1.1612	Pass
39	0.27	0.09872	1.1017	Pass

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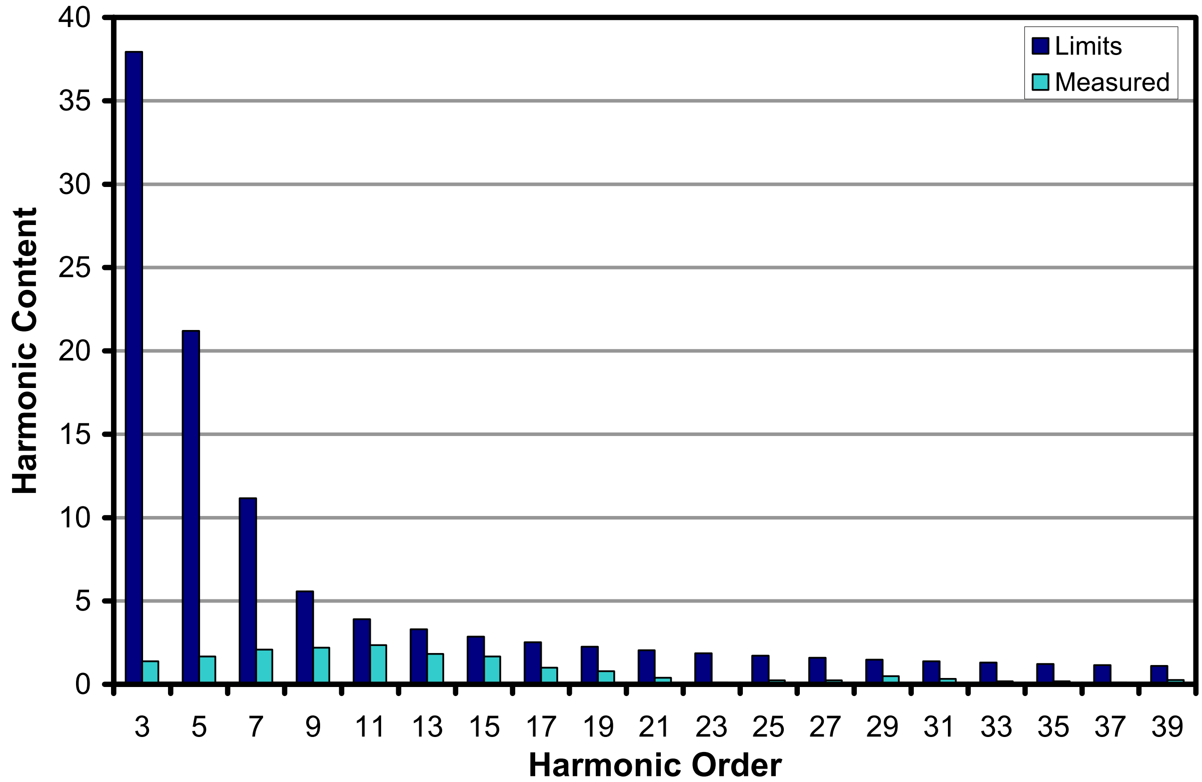

Figure 17 – Meets EN61000-3-2 Harmonics Contents Standards for <25 W Rating.

11 Thermal Performance

11.1 Equipment Used

Chamber:	Tenney Environmental Chamber Model No: TJR-17 942
AC Source:	Chroma Programmable AC Source Model No: 6415
Wattmeter:	Yokogawa Power Meter Model No: WT2000
Data Logger:	Monogram SN:1290492

Figure 18 – Thermal Chamber Set-up Showing Box Used to Prevent Airflow Over UUT.

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11.2 Thermal Results

Load: 36 V / 130 mA LED load. Ambient of 90 °C simulates operation inside sealed LED replacement enclosure.

Normal Operation	Device Temperature (ºC)					
Component	85 V/50 Hz		100 V/50Hz		115V/60Hz	
	Normal	OTP	Normal	OTP	Normal	OTP
Box Internal Ambient (ºC)	90	106	90	113	90	113
Bridge (BR1)	108	120	103	125	102	125
Blocking Diode (D1)	113	125	107	130	106	129
LNK458KG (U1)	120	134	112	134	111	134
Inductor Core (L3)	116	126	108	130	105	130
Output Diode (D2)	126	138	110	132	109	132

Table 1 – Thermal Data if U1 Exposed Pad is Soldered.

Normal Operation	Device Temperature (ºC)					
Component	85 V/50 Hz		100 V/50Hz		115V/60Hz	
	Normal	OTP	Normal	OTP	Normal	OTP
Box Internal Ambient (ºC)	90	104	90	107	90	107
Bridge (BR1)	108	118	104	120	104	120
Blocking Diode (D1)	112	124	109	126	110	126
LNK458KG (U1)	125	133	117	135	118	135
Inductor Core (L3)	115	124	108	126	110	126
Output Diode (D2)	122	127	112	129	113	129

Table 2 – Thermal Data if U1 Exposed Pad is Unsoldered.

12 Thermal Scans

The scan is conducted at ambient temperature of 25 ºC, 85 VAC / 47 Hz input and 35 V LED string load.

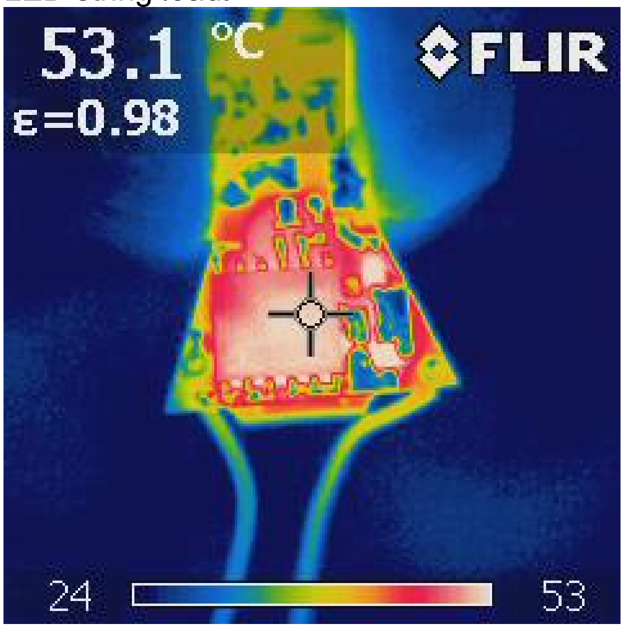

Figure 19 – U1 Case Temperature.

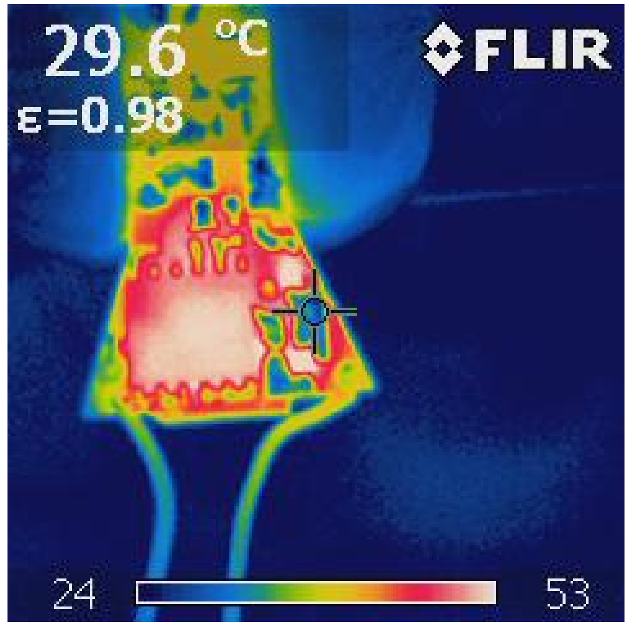

Figure 20 – D2 Case Temperature.

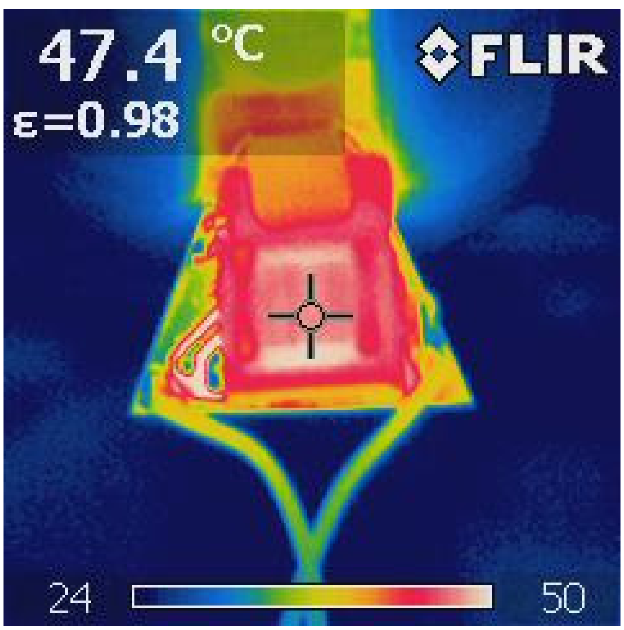

Figure 21 – L3 Temperature.

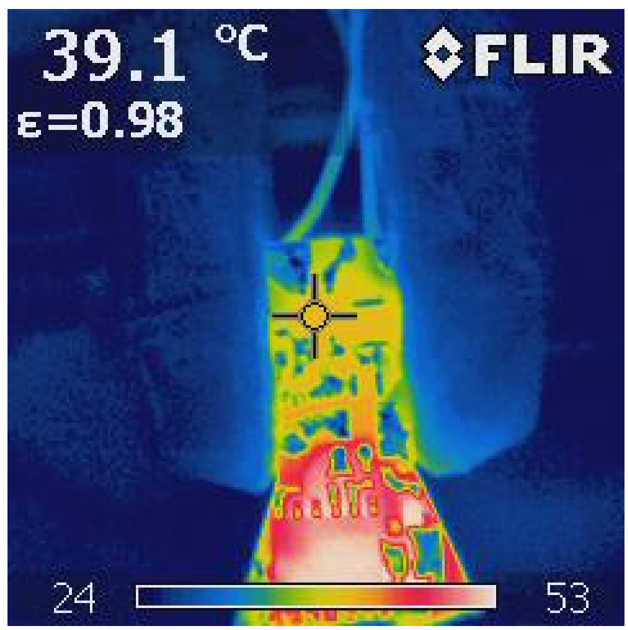

Figure 22 – BR1 Case Temperature.

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13 Waveforms

13.1 Drain Voltage and Current, Normal Operation

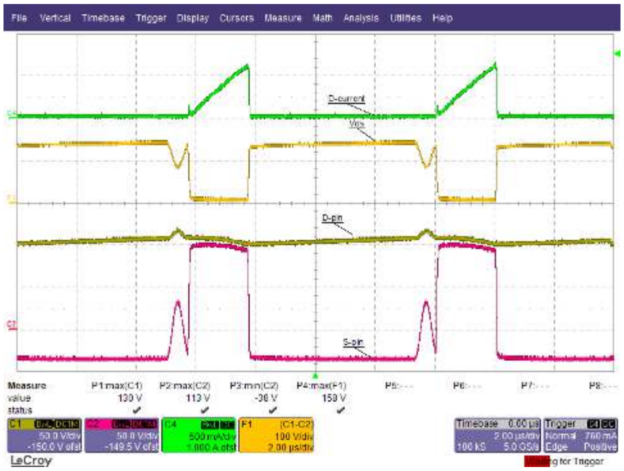

Figure 23 – 85 VAC / 47 Hz, 35 V LED String.
Ch1: V_{DRAIN}, 50 V / div.
Ch2: V_{SOURCE}, 50 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 2 µs / div.

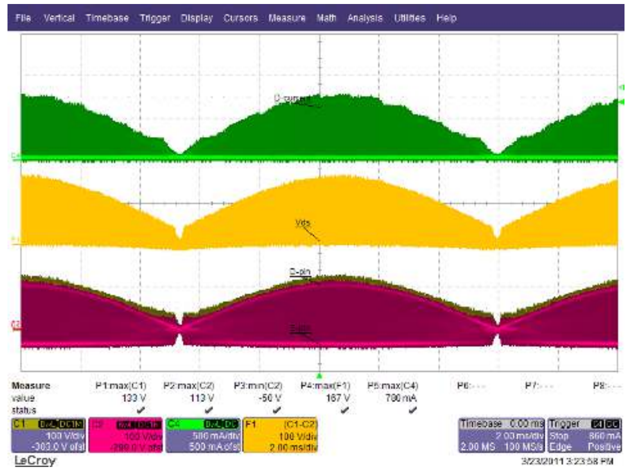

Figure 24 – 85 VAC / 47 Hz, 35 V LED String.
Ch1: V_{DRAIN}, 100 V / div.
Ch2: V_{SOURCE}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 2 ms / div.

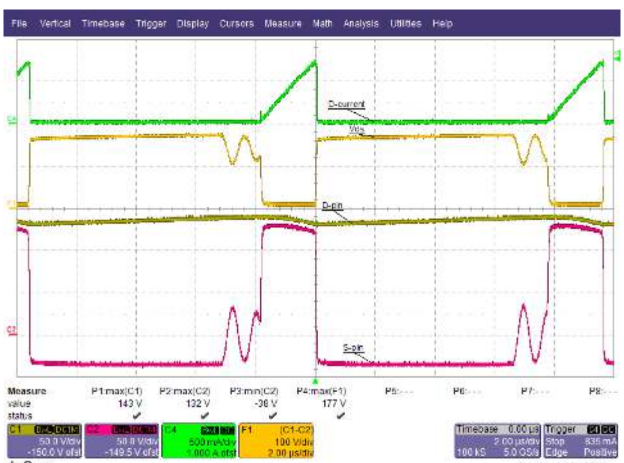

Figure 25 – 100 VAC / 50 Hz, 35 V LED String.
Ch1: V_{DRAIN}, 50 V / div.
Ch2: V_{SOURCE}, 50 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 2 µs / div.

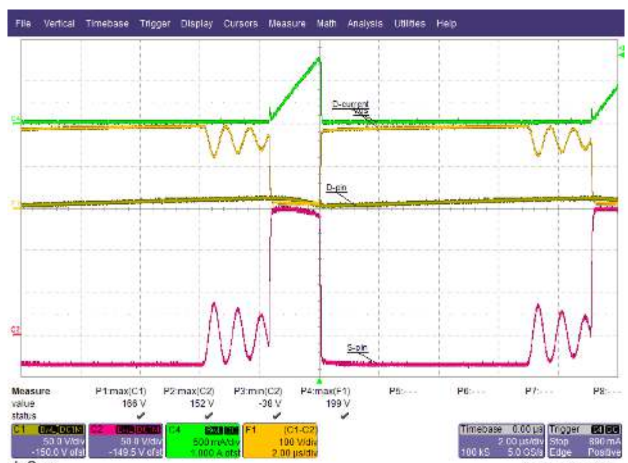

Figure 26 – 115 VAC / 60 Hz, 35 V LED String.
Ch1: V_{DRAIN}, 50 V / div.
Ch2: V_{SOURCE}, 50 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 2 µs / div.

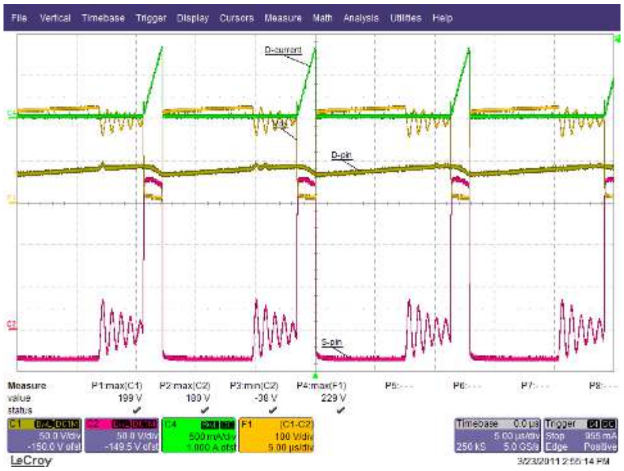

Figure 27 – 135 VAC / 63 Hz, 35 V LED String.
Ch1: V_{DRAIN}, 50 V / div.
Ch2: V_{SOURCE}, 50 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 5 μs / div.

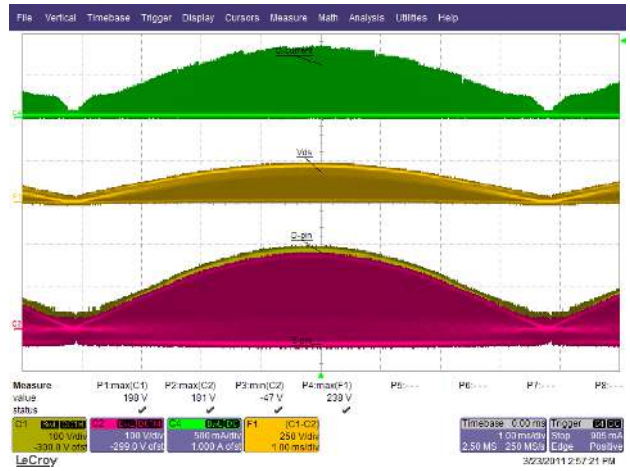

Figure 28 – 355 VAC / 63 Hz, 35 V LED String.
Ch1: V_{DRAIN}, 100 V / div.
Ch2: V_{SOURCE}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div
F1: $V_{D\text{-}S}$, 250 V / div., 1 ms / div.

13.2 Drain Voltage and Current Start-up Profile

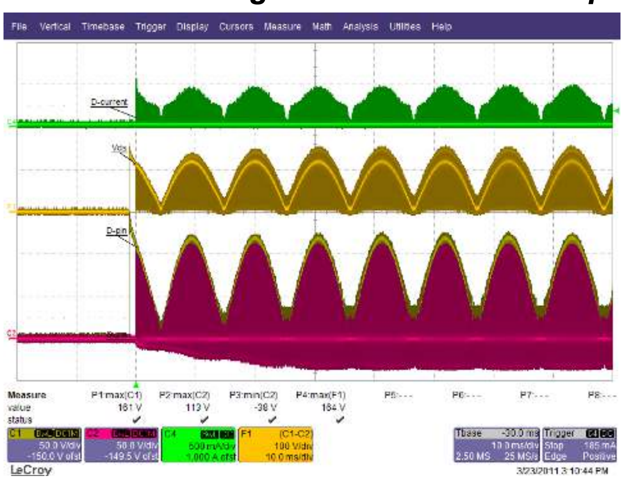

Figure 29 – 85 VAC / 47 Hz, 35 V LED String.
Ch1: V_{DRAIN}, 50 V / div.
Ch2: V_{SOURCE}, 50 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 10 ms / div.

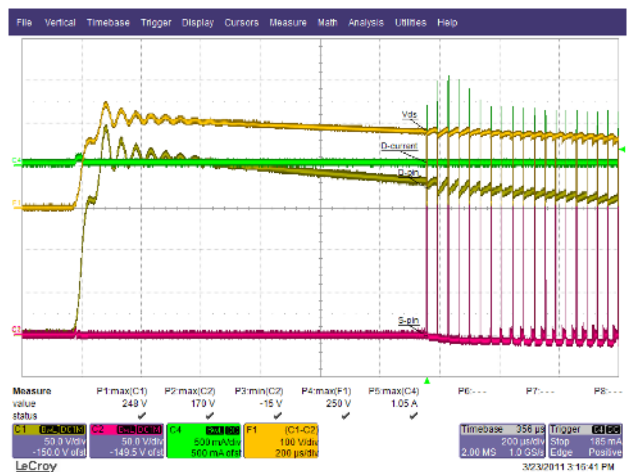

Figure 30 – 135 VAC / 63 Hz, 35 V LED String.
Ch1: V_{DRAIN}, 50 V / div.
Ch2: V_{SOURCE}, 50 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 200 μs / div.

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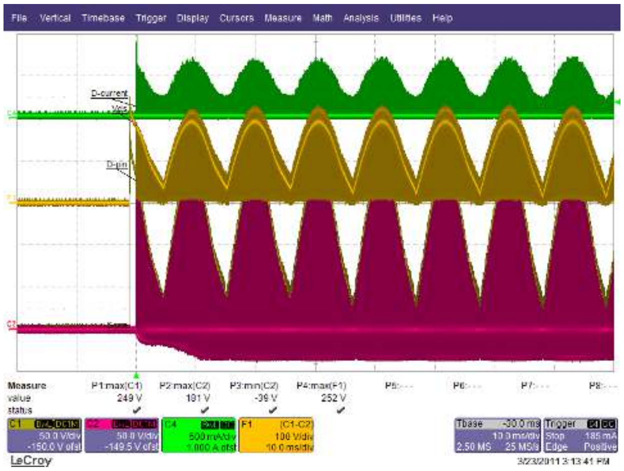

Figure 31 – 135 VAC / 63 Hz, 35 V LED String.
Ch1: V_{DRAIN}, 50 V / div.
Ch2: V_{SOURCE}, 50 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 10 ms / div.

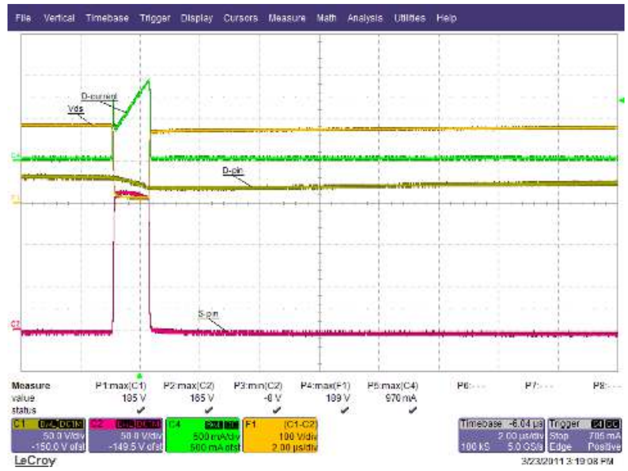

Figure 32 – 135 VAC / 63 Hz, 35 V LED String.
Ch1: V_{DRAIN}, 50 V / div.
Ch2: V_{SOURCE}, 50 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 2 µs / div.

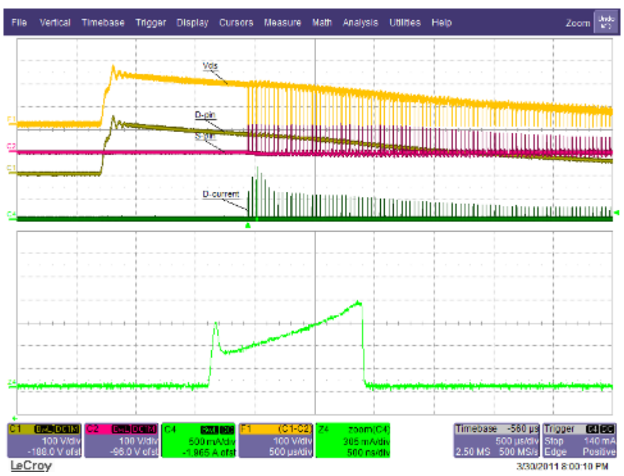

Figure 33 – 125 °C Start-up; 135 VAC / 63 Hz; 85° Phase Angle, 35 V LED String.
Ch1: V_{DRAIN}, 100 V / div.
Ch2: V_{SOURCE}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 500 µs / div.
Z4: I_{DRAIN}, 305 mA / div.; 500 ns / div.

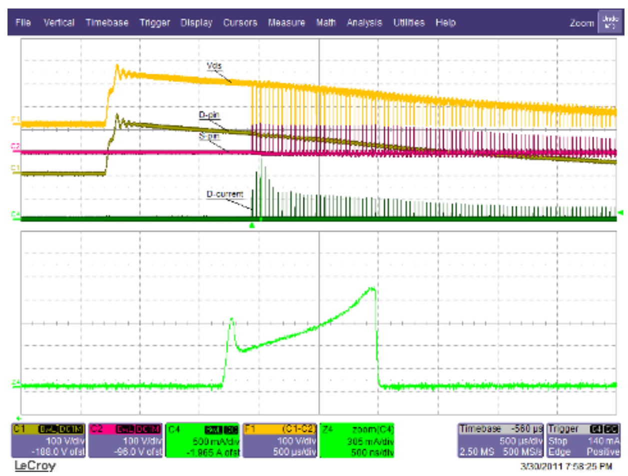

Figure 34 – 150 °C Start-up; 135 VAC / 63 Hz; 85° Phase Angle, 35 V LED String.
Ch1: V_{DRAIN}, 100 V / div.
Ch2: V_{SOURCE}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: $V_{D\text{-}S}$, 100 V / div., 500 µs / div.
Z4: I_{DRAIN}, 305 mA / div.; 500 ns / div.

13.3 Output Voltage Start-up Profile

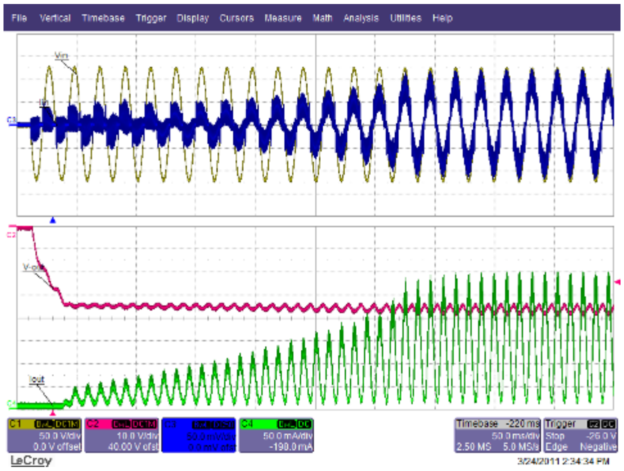

Figure 35 – 85 VAC / 47 Hz, 35 V LED String.
Ch1: V_{IN}, 50 V / div.
Ch2: V_{OUT}, 10 V / div.
Ch3: I_{IN}, 50 mA / div.
Ch4: I_{OUT}, 50 mA / div., 50 ms / div.

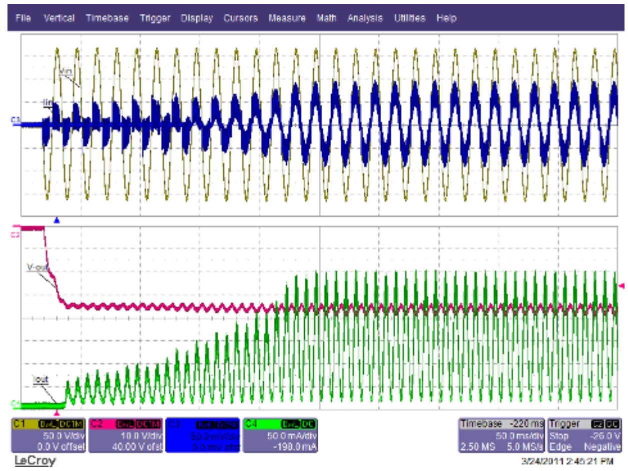

Figure 36 – 135 VAC / 63 Hz, 35 V LED String.
Ch1: V_{IN}, 50 V / div.
Ch2: V_{OUT}, 10 V / div.
Ch3: I_{IN}, 50 m A / div.
Ch4: I_{OUT}, 50 mA / div., 50 ms / div.

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13.4 Drain Voltage and Current Start-up Short Profile

Figure 37 – 135 VAC / 63 Hz, Output Shorted.
Ch1: V_{DRAIN}, 100 V / div.
Ch2: V_{SOURCE}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: V_{D-S}, 100 V / div., 1 s / div.

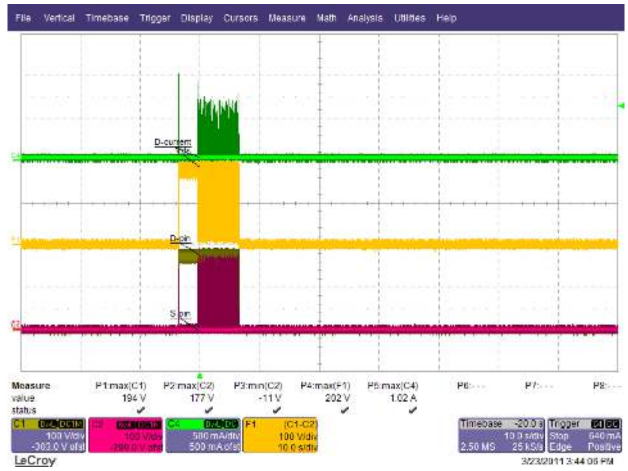

Figure 38 – 135 VAC / 63 Hz, Output Shorted.
Ch1: V_{DRAIN}, 100 V / div.
Ch2: V_{SOURCE}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: V_{D-S}, 100 V / div., 10 s / div.

Figure 39 – 135 VAC / 63 Hz, Output Shorted.
Ch1: V_{DRAIN}, 100 V / div.
Ch2: V_{SOURCE}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: V_{D-S}, 100 V / div., 20 ms / div.

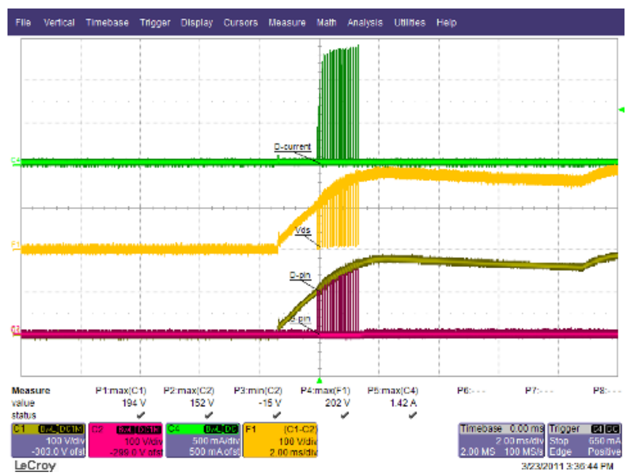

Figure 40 – 135 VAC / 63 Hz, Output Shorted.
Ch1: V_{DRAIN}, 100 V / div.
Ch2: V_{SOURCE}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
F1: V_{D-S}, 100 V / div., 2 ms / div.

13.5 Line Transient Response

Figure 41 – 115 VAC / 50 Hz,
300 ms On – 300 ms Off.
Load: 35V LED String.
Ch1: V_{IN}, 50 V / div.
Ch2: V_{OUT}, 10 V / div.
Ch4: I_{OUT}, 100 mA / div., 1 s / div.

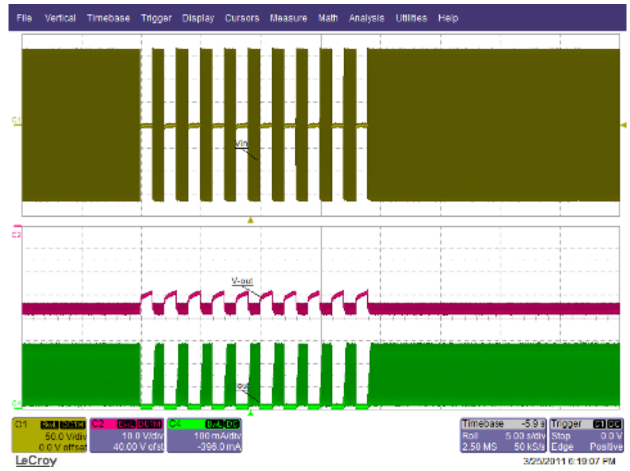

Figure 42 – 115 VAC / 50 Hz,
1 s On - 1 s Off.
Load: 35 V LED String.
Ch1: V_{IN}, 50 V / div.
Ch2: V_{OUT}, 10 V / div.
Ch4: I_{OUT}, 100 mA / div., 5 s / div.

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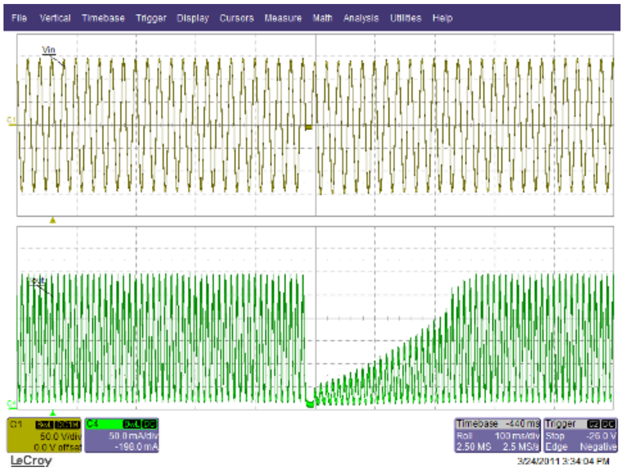

Figure 43 – 115 VAC / 50 Hz, 0.5 Cycle-Skip.
Load: 35 V LED String.
Ch1: V_{IN}, 50 V / div.
Ch3: I_{IN}, 50 mA / div,100 ms / div.

Figure 44 – 115 VAC / 50 Hz, 0.25 Cycle-Skip.
Load: 35 V LED String.
Ch1: V_{IN}, 50 V / div.
Ch3: I_{IN}, 50 mA / div.,100 ms / div.

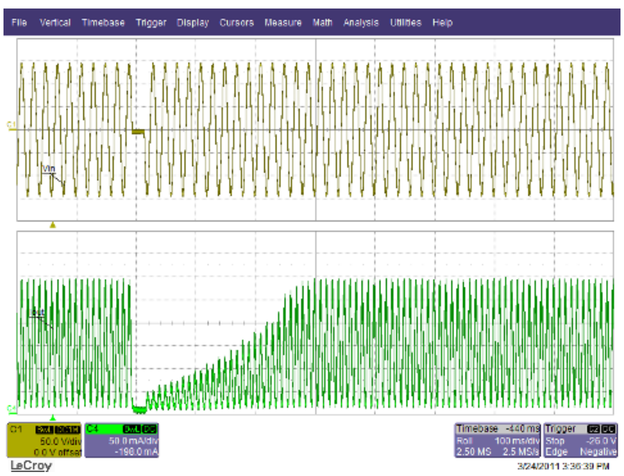

Figure 45 – 115 VAC / 50 Hz, 1 Cycle-Skip.
Load: 35 V LED String.
Ch1: V_{IN}, 50 V / div.
Ch3: I_{IN}, 50 mA / div.,100 ms / div.

Figure 46 – 115 VAC / 50 Hz, 2 Cycle-Skip.
Load: 35 V LED String.
Ch1: V_{IN}, 50 V / div.
Ch3: I_{IN}, 50 mA / div.,100 ms / div.

13.6 Brown-out

Input voltage slew rate of 0.1 V / s from 85-0-85 VAC / 50 Hz line input variation; no failure observed.

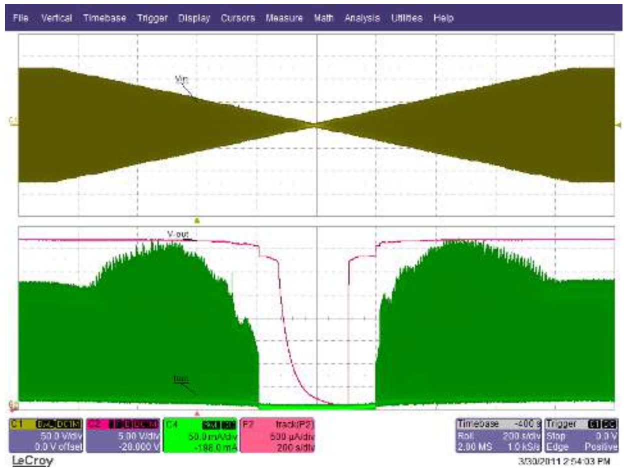

Figure 47 – 85 VAC / 50 Hz, 35 V LED String.
Below 75 VAC the peak current of the load is higher than normal but the average current is regulated at 130 mA.
Ch1: V_{IN}, 50 V / div.
Ch2: V_{OUT}, 5 V / div.
Ch3: I_{IN}, 50 mA / div.,200 s / div.

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13.7 Start-up No-load

This LED driver is protected by VR1 in case of no-load condition occurs in order to avoid leakage from the output capacitor. This protection is not auto-recover; replace VR1 in case this condition occurs.

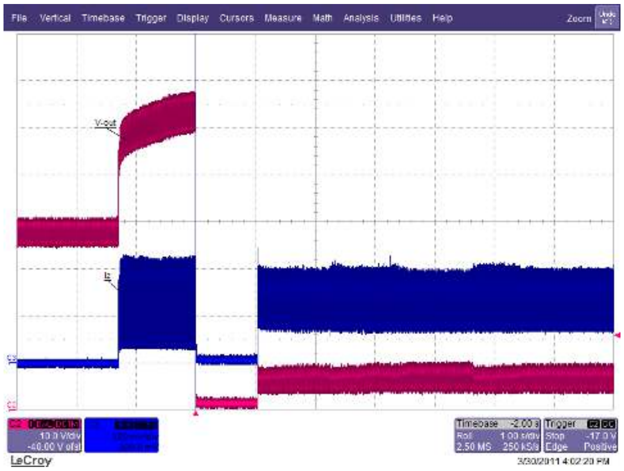

Figure 48 – 185 VAC / 63 Hz, Start-up No-load.
Ch2: V_{OUT}, 10 V / div.
Ch4: I_{OUT}, 100 mA / div., 1 s / div.

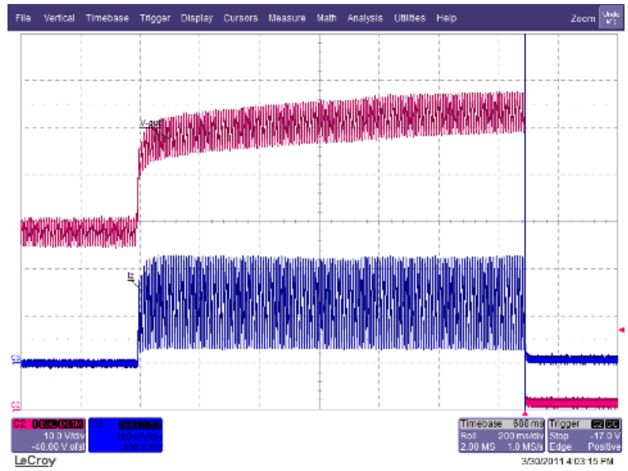

Figure 49 – 85 VAC / 63 Hz, Start-up No-load.
Ch2: V_{OUT}, 10 V / div.
Ch4: I_{OUT}, 100 mA / div., 200 ms / div.

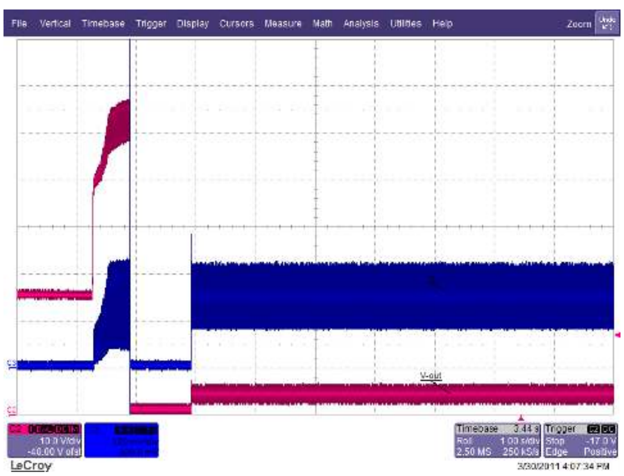

Figure 50 – 135 VAC / 63 Hz, Start-up No-load.
Ch2: V_{OUT}, 10 V / div.
Ch4: I_{OUT}, 100 mA / div., 1 s / div.

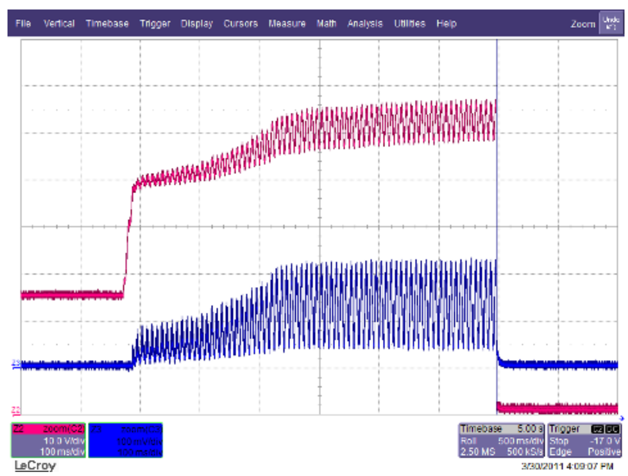

Figure 51 – 135 VAC / 63 Hz, Start-up No-load.
Ch2: V_{OUT}, 10 V / div.
Ch4: I_{OUT}, 100 mA / div., 500 ms / div.

13.8 Line Surge Waveform

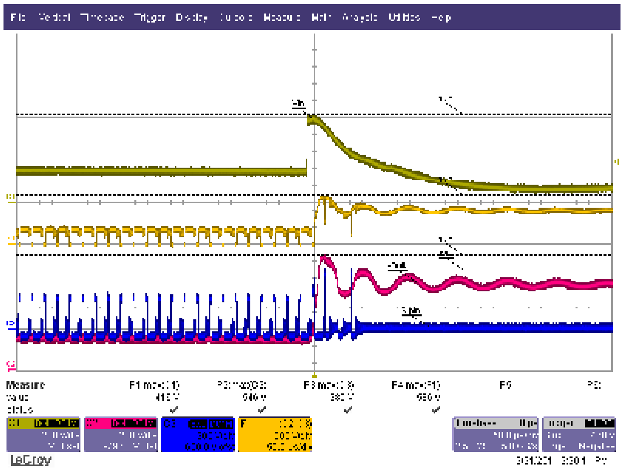

Figure 52 – 115 VAC / 60 Hz,
500 V Differential Surge.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{DRAIN}, 10 V / div.
Ch3: V_{SOURCE}, 10 V / div.
F1: V_{DS}, 500 V / div., 50 μs / div.

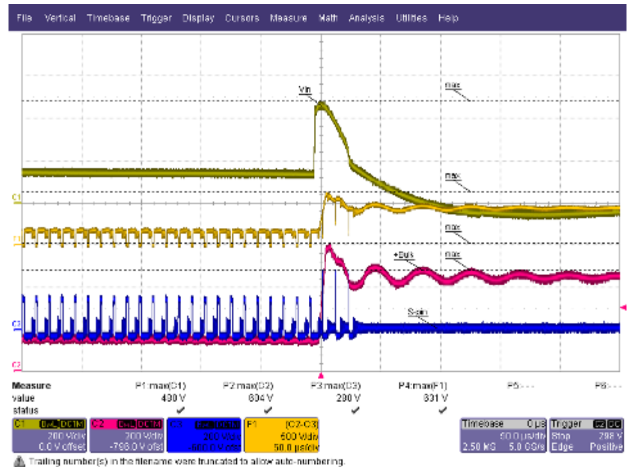

Figure 53 – 115 VAC / 60 Hz,
1 kV Differential Surge; VR2 Installed.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{DRAIN}, 10 V / div.
Ch3: V_{SOURCE}, 10 V / div.
F1: V_{DS}, 500V / div., 50 μs / div.

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14 Line Surge

Input voltage was set at 115 VAC / 60 Hz. Output was loaded with 35 V LED string and operation was verified following each surge event.

Differential input line 1.2 / 50 μs surge testing was completed on two test unit to IEC61000-4-5.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
Option 1: VR2 not installed				
+500	115	L to N	0	Pass
-500	115	L to N	0	Pass
+500	115	L to N	90	Pass
-500	115	L to N	90	Pass
Option 2: VR2 installed				
+1200	115	L to N	0	Pass
-1200	115	L to N	0	Pass
+1200	115	L to N	90	Pass
-1200	115	L to N	90	Pass

Differential input line ring surge testing was completed on two test unit to IEC61000-4-5.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
Option 1: VR2 not installed				
+2500	115	L to N	0	Pass
-2500	115	L to N	0	Pass
+2500	115	L to N	90	Pass
-2500	115	L to N	90	Pass
+3000	115	L to N	0	Pass
-3000	115	L to N	0	Pass
+3000	115	L to N	90	Pass
-3000	115	L to N	90	Pass

Unit passes under all test conditions.

15 Conducted EMI

15.1 Equipment:

Receiver:

Rohde & Schwartz
ESPI - Test Receiver (9 kHz – 3 GHz)
Model No: ESPI3

LISN:

Rohde & Schwartz
Two-Line-V-Network
Model No: ENV216

15.2 EMI Test Set-up

LED driver is placed in a conical metal housing (for self-ballasted lamps; CISPR15 Edition 7.2).

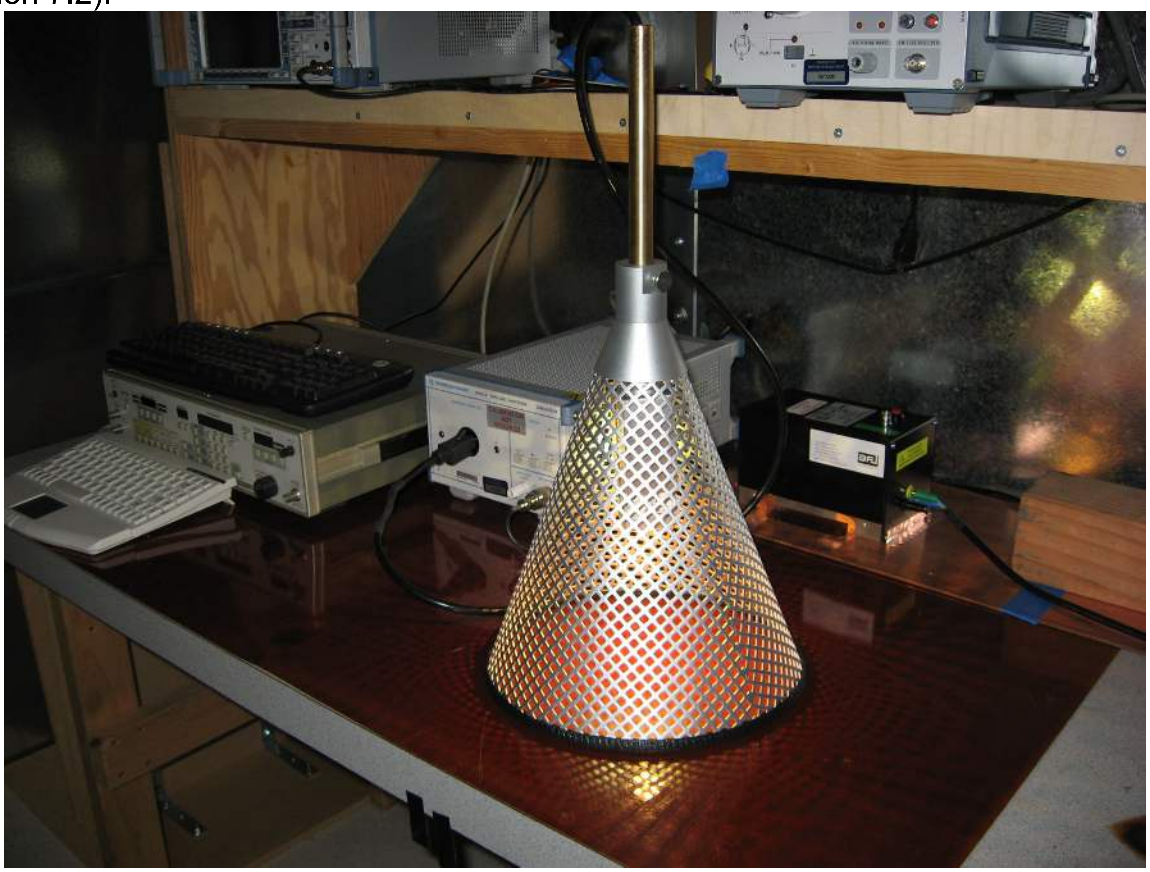

Figure 54 – Conducted Emissions Measurement Set-up
Showing Conical Ground Plane Inside which UUT was Mounted.

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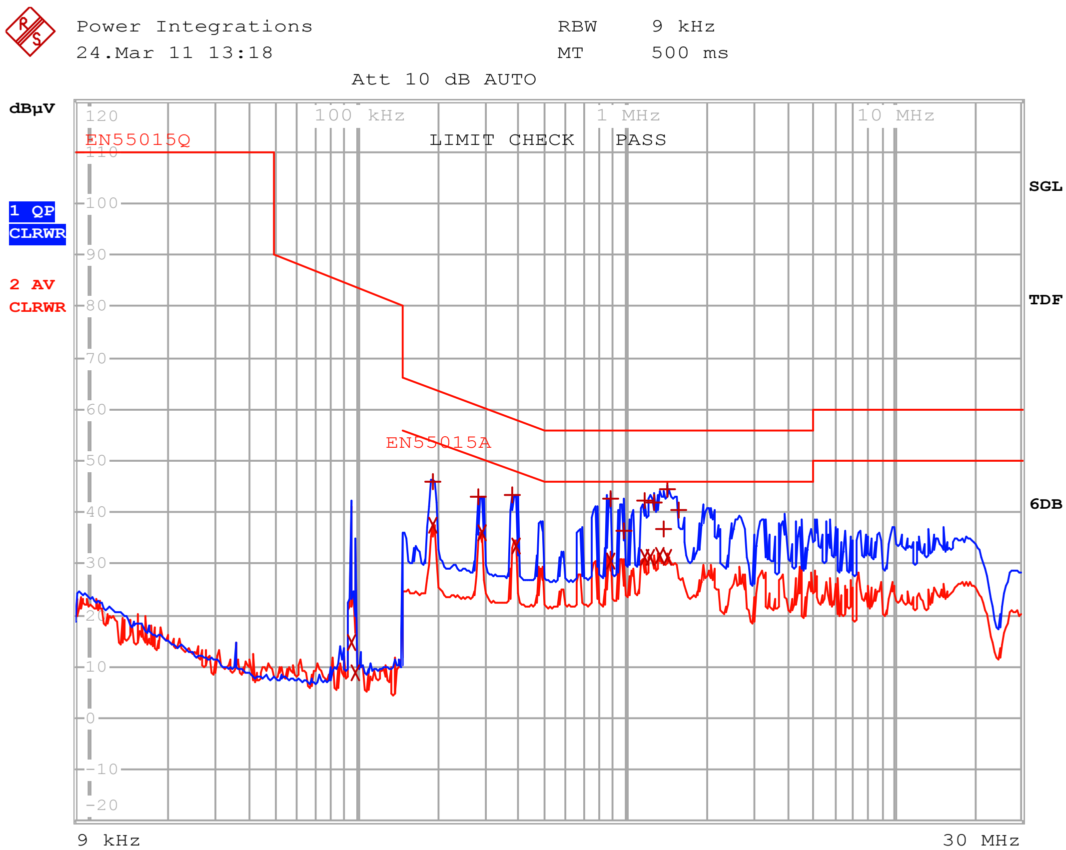

Figure 55 – Conducted EMI, Maximum Steady-State Load, 115 VAC, 60 Hz, and EN55015 Limits.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	95.14984736 kHz	14.69	L1 gnd	
2	Average	99.0133127137 kHz	8.86	N gnd	
1	Quasi Peak	190.46019728 kHz	45.86	N gnd	-18.15
2	Average	192.364799253 kHz	37.68	N gnd	-16.25
1	Quasi Peak	283.569280422 kHz	42.86	N gnd	-17.84
2	Average	289.269022958 kHz	36.17	N gnd	-14.36
1	Quasi Peak	378.424303998 kHz	43.21	N gnd	-15.09
2	Average	389.890938834 kHz	33.37	N gnd	-14.69
1	Quasi Peak	881.64914842 kHz	42.69	N gnd	-13.30
2	Average	881.64914842 kHz	30.42	N gnd	-15.57
1	Quasi Peak	983.628047757 kHz	36.36	N gnd	-19.63
1	Quasi Peak	1.17656420634 MHz	42.34	N gnd	-13.65
2	Average	1.17656420634 MHz	31.30	N gnd	-14.69
2	Average	1.23658080545 MHz	31.28	N gnd	-14.71
1	Quasi Peak	1.27405044044 MHz	41.86	N gnd	-14.13
2	Average	1.33903981723 MHz	31.57	N gnd	-14.42
1	Quasi Peak	1.37961406273 MHz	36.63	N gnd	-19.36
1	Quasi Peak	1.43563192593 MHz	44.42	N gnd	-11.57
2	Average	1.43563192593 MHz	31.34	N gnd	-14.65
1	Quasi Peak	1.57012949439 MHz	40.49	N gnd	-15.51

Figure 56 – Conducted EMI, Maximum Steady-State Load, 115 VAC, 60 Hz, and EN55015 Limits. Line and Neutral Scan Design Margin Measurement.

16 Revision History

Date	Author	Revision	Description & changes	Reviewed
08-Jun-11	JDC	1.0	Initial Release	Apps & Mktg

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