High-Speed CMOS QuickSwitch® 8-Bit Bus Switches

QS3244
QS32244

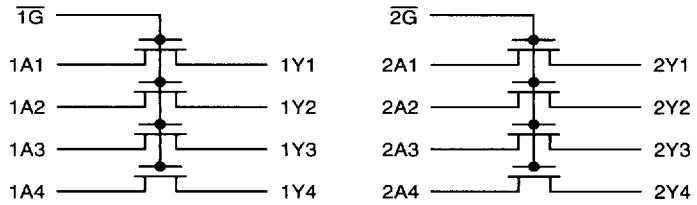
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Pin compatible to the 74F244, 74FCT244, and 74FCT244T
- Low power CMOS proprietary technology
- Zero propagation delay
- Zero added signal skew
- Zero ground bounce
- Available in 20-pin DIP, SOIC (SO), & QSOP

DESCRIPTION

The QS3244 and QS32244 provide a set of eight high-speed CMOS TTL-compatible bus switches in a pinout compatible with 74FCT244, 74F244, 74ALS/AS/LS244 8-bit drivers. The low ON resistance (5 Ω) of the 3244 allows inputs to be connected outputs without adding propagation delay and without generating additional ground bounce noise. The two enable ($\overline{nG}$) signals turn the switches on similar to the $\overline{nG}$ signals of the 74'244. The QS32244 device includes 25Ω series termination resistors.

FUNCTIONAL BLOCK DIAGRAM

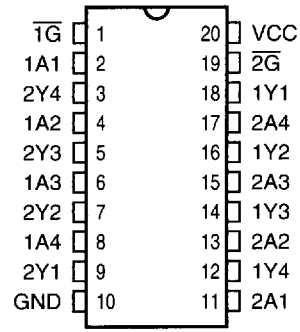


PIN DESCRIPTION

Name	Description
$\overline{1G}/\overline{2G}$	Output Enable
An	Data I/Os
Yn	Data I/Os

PIN CONFIGURATION (All Pins Top View)

PDIP, SOIC (SO), QSOP



FUNCTION TABLE

$\overline{1G}$	$\overline{2G}$	1A, 1Y I/Os	2A, 2Y I/Os
H	H	Disconnected	Disconnected
L	H	1An = 1Yn	Disconnected
H	L	Disconnected	2An = 2Yn
L	L	1An=1Yn	2An=2Yn

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Switch Voltage Vs	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC	QSOP	PDIP	Unit
Control Pins	3	3	4	pF
QuickSwitch Channels	8	8	8	pF

Note: Capacitance is characterized but not tested and are typical values.

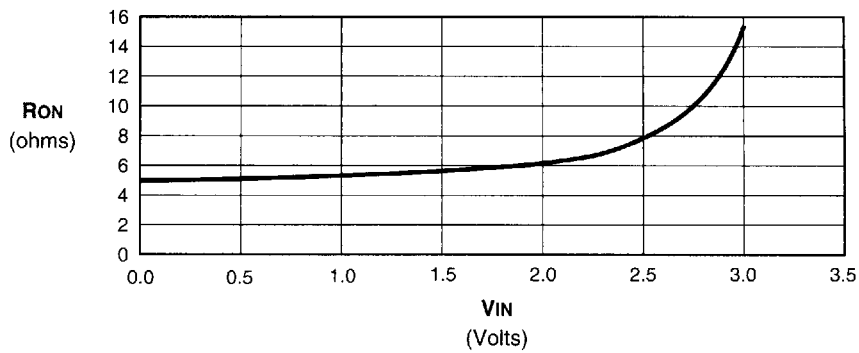
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions		Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
$\lvert I_{IN} \rvert$	Input Leakage Current(2)	0 ≤ V_{IN} ≤ Vcc		—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Current (Hi-Z)	0 ≤ A, Y ≤ Vcc		—	—	5	µA
R_{ON}	Switch ON Resistance(3,4)	Vcc = Min., V_{IN} = 0.0V	3244	—	5	7	Ω
		I_{ON} = 30 mA	32244	20	28	40	
R_{ON}	Switch ON Resistance(3,4)	Vcc = Min., V_{IN} = 2.4V	3244	—	10	15	Ω
		I_{ON} = 15 mA	32244	20	35	48	

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. During input/output leakage, testing all pins are at a HIGH or LOW state, and the $\overline{G}$ controls are HIGH.
3. Measured by voltage drop between A and Y pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,Y) pins.
4. R_{ON} guaranteed but not tested.

Typical ON Resistance vs V_{IN} at 4.75 Vcc (QS3244 Only)



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc = Max., V_{IN} = GND or Vcc, f = 0	2.5	mA
ΔI_{CC}	Power Supply Current[2] per Input HIGH	Vcc = Max., V_{IN} = 3.4V, f = 0 per Control Input	3.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[3]	Vcc = Max., A and Y Pins Open, Controls Inputs Toggling @ 50% Duty Cycle	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A and Y pins do not contribute to Icc.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and Y inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

		QS3244			QS32244			
Symbol	Description	Min	Typ	Max	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay[2,3] An to Yn	—	—	0.25	—	—	2.0	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay[1] $\overline{1G}$, $\overline{2G}$ to Yn	0.5	—	5.6	0.5	—	5.6	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay[1,2] $\overline{1G}$, $\overline{2G}$ to Yn	0.5	—	5.2	0.5	—	5.2	ns
Q_{CI}	Charge Injection, Typical[4,5]	—	1.5	—	—	1.5	—	pC

Notes:
1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Measured at switch turn off, A to Y, C_{LOAD} = 50 pF in parallel with 10 mΩ scope probe, V_{IN} at I = 0.0V.
5. Characterized parameter but not tested.