



# STW45NM50FD

N-channel 500 V, 0.07  $\Omega$ , 45 A, TO-247  
FDmesh™ Power MOSFET (with fast diode)

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STW45NM50FD	500 V	< 0.1 $\Omega$	45 A

- 100% avalanche tested
- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance

## Application

- Switching applications

## Description

The FDmesh™ associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.

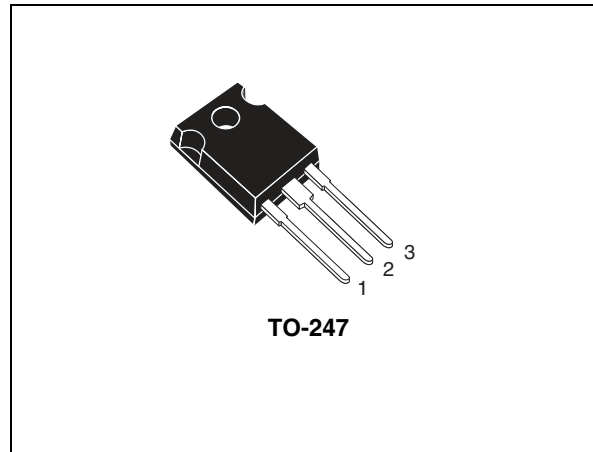


Figure 1. Internal schematic diagram

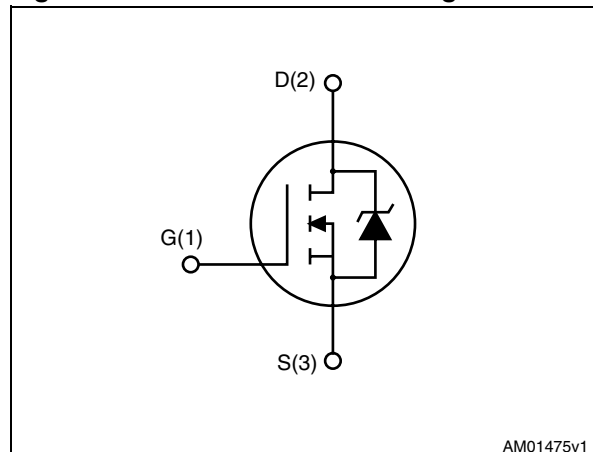


Table 1. Device summary

Order code	Marking	Package	Packaging
STW45NM50FD	W45NM50FD	TO-247	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	500	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	45	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	28.4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	180	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	417	W
	Derating factor	2.08	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	20	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-65 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 45\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\%V_{(BR)DSS}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.3	$^\circ\text{C}/\text{W}$
$R_{thj-a}$	Thermal resistance junction-ambient max	30	$^\circ\text{C}/\text{W}$
$T_I$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 4. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	22.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	800	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$	500			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating @ } 125\text{ °C}$			10 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 22.5\text{ A}$		0.07	0.10	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 22.5\text{ A}$	-	20		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	3600 1260 80		pF pF pF
$C_{oss\ eq.}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0$ to $400\text{ V}$	-	350		pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400\text{ V}$ , $I_D = 45\text{ A}$ $V_{GS} = 10\text{ V}$ <a href="#">Figure 14</a>	-	92 22 40	120	nC nC nC
$R_G$	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 test signal level = 20 mV open drain	-	2		$\Omega$

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=250\text{ V}$ , $I_D=22.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ <a href="#">Figure 15</a>	-	26.5 107.5	-	ns ns
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage rise time Fall time Cross-over time	$V_{DD}=400\text{ V}$ , $I_D=45\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ <a href="#">Figure 15</a>	-	21.6 87.7 110.9	-	ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		45	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		180	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=45\text{ A}$ , $V_{GS}=0$	-		1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=45\text{ A}$ , $V_{DD}=100\text{ V}$ $di/dt=100\text{ A}/\mu\text{s}$ , <a href="#">(see Figure 18)</a>	-	200 1600 16		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=45\text{ A}$ , $T_j=150\text{ }^\circ\text{C}$ $di/dt=100\text{ A}/\mu\text{s}$ , $V_{DD}=100\text{ V}$ , <a href="#">(see Figure 18)</a>	-	324 4017 24.8		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

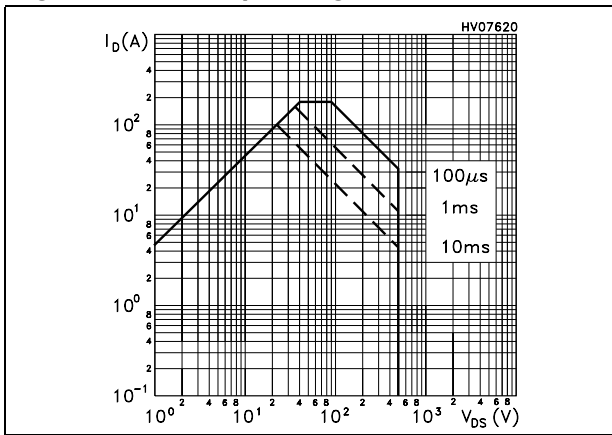


Figure 3. Thermal impedance

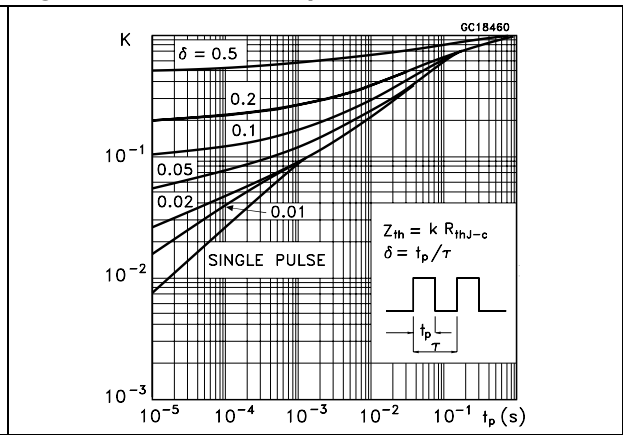


Figure 4. Output characteristics

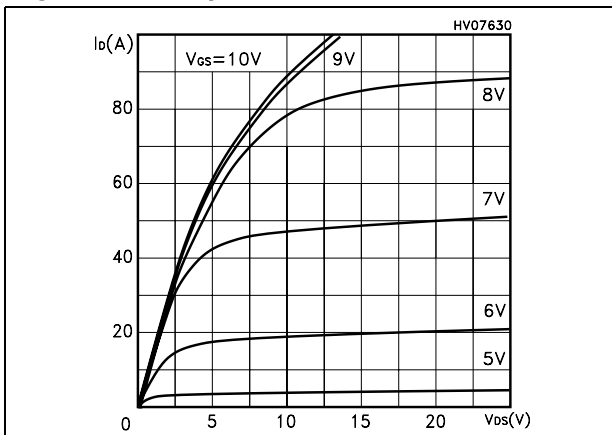


Figure 5. Transfer characteristics

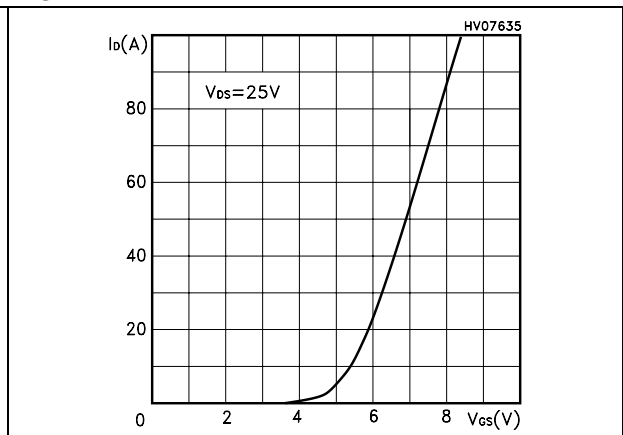


Figure 6. Transconductance

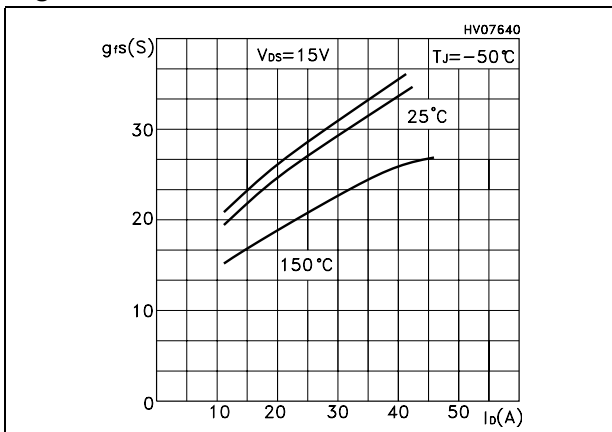


Figure 7. Static drain-source on resistance

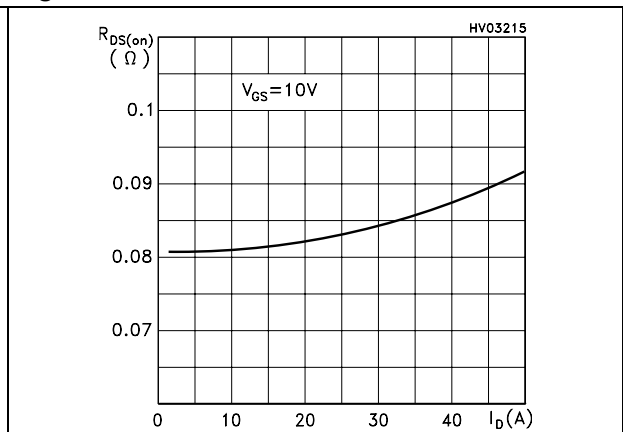


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

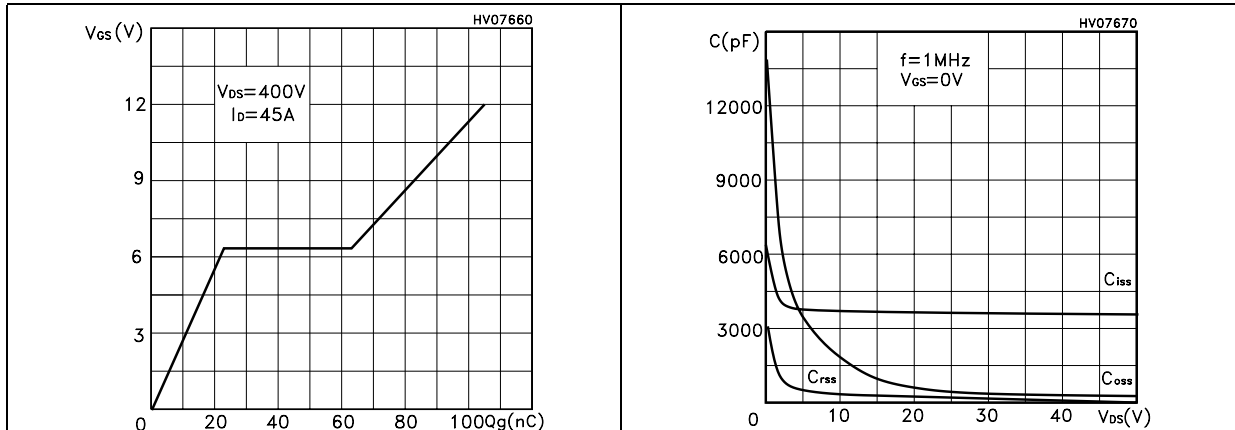


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

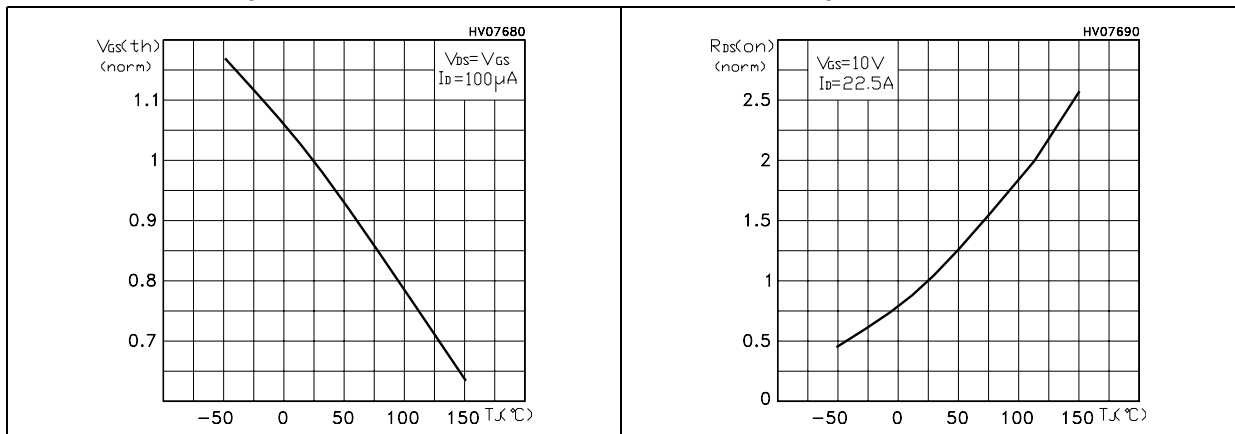
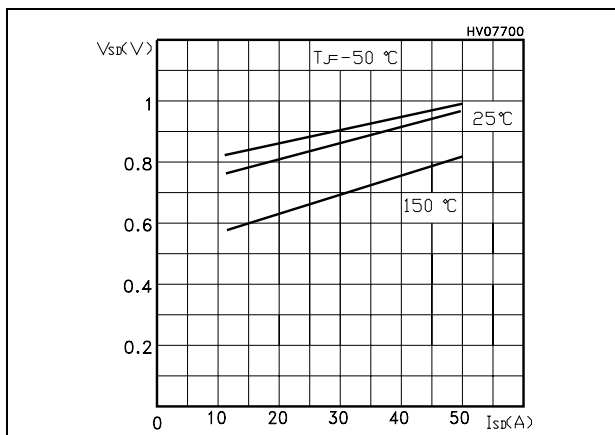
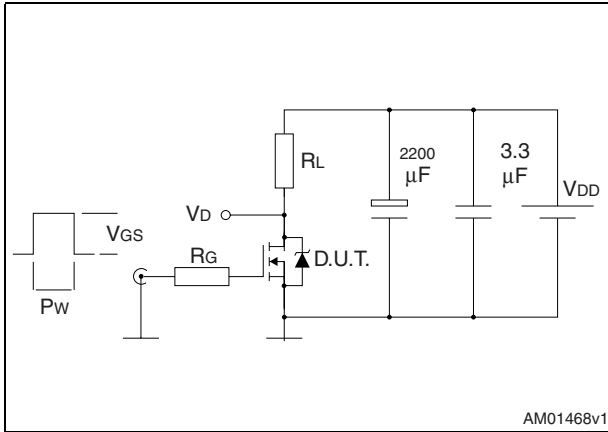


Figure 12. Source-drain diode forward characteristics



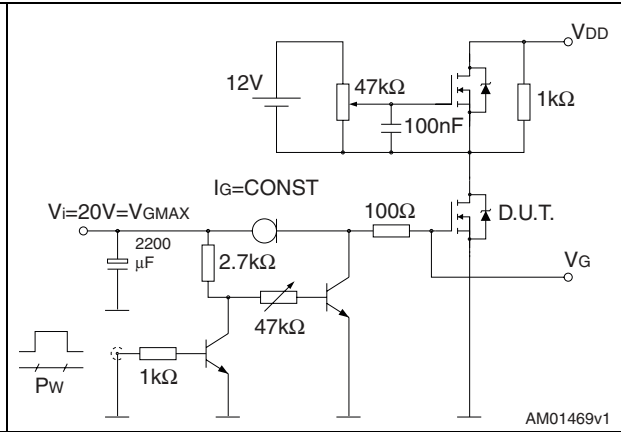
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



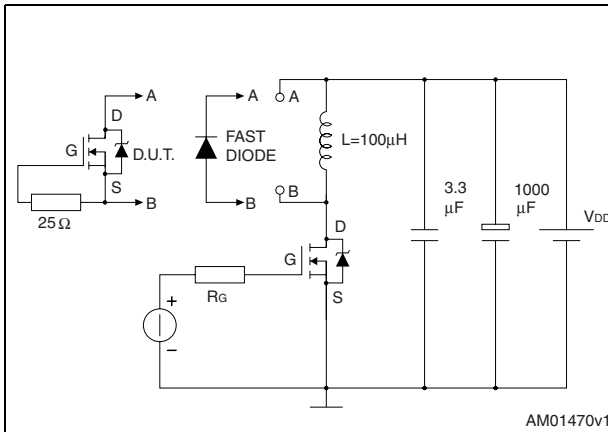
AM01468v1

**Figure 14. Gate charge test circuit**



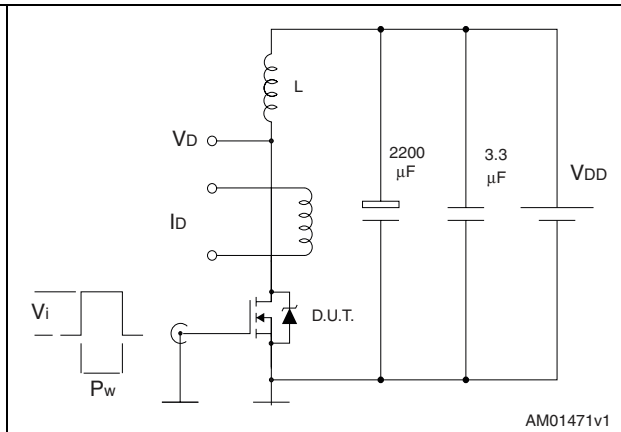
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**Figure 15. Test circuit for inductive load switching and diode recovery times**



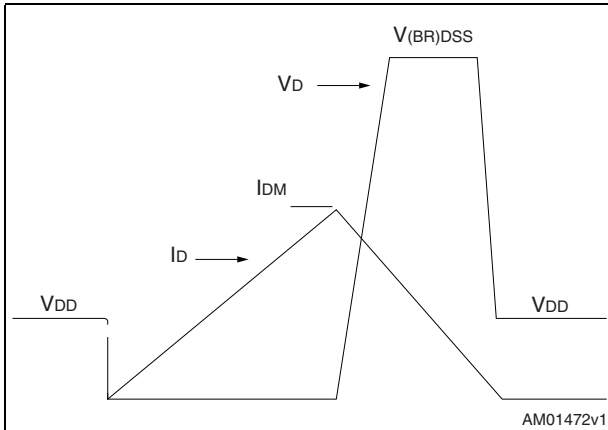
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**Figure 16. Unclamped inductive load test circuit**



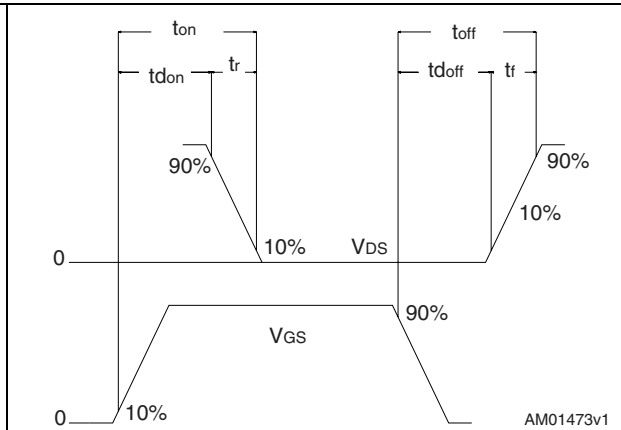
AM01471v1

**Figure 17. Unclamped inductive waveform**



AM01472v1

**Figure 18. Switching time waveform**



AM01473v1

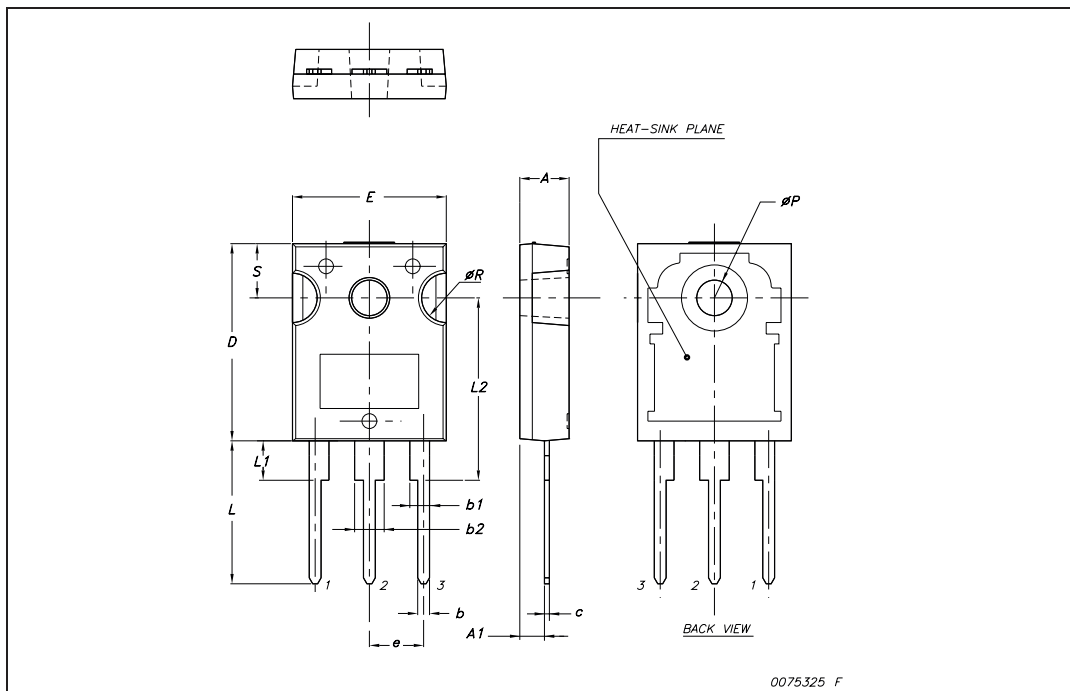


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
05-Apr-2005	8	Modified value on <i>Source drain diode</i>
26-Apr-2006	9	New template
23-Jul-2009	10	Modified values on <i>Switching times</i>

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