

## Product Summary

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX T <sub>C</sub> = +25°C
60V	6.2mΩ @ V <sub>GS</sub> = 10V	82A
	8.5mΩ @ V <sub>GS</sub> = 4.5V	70A

## Description and Applications

This MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- Synchronous Rectifier
- DC-DC Converters
- Power Management

## Features

- 100% Unclamped Inductive Switching (UIS) Test in Production — Ensures More Reliable and Robust End Application.
- High Conversion Efficiency
- Low R<sub>DS(ON)</sub>—Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- Wettable Flank for Improved Optical Inspection
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

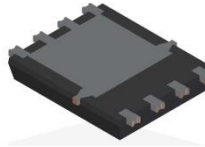
## Mechanical Data

- Case: PowerDI<sup>®</sup> 5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish—Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 **Ⓔ3**
- Weight: 0.097 grams (Approximate)

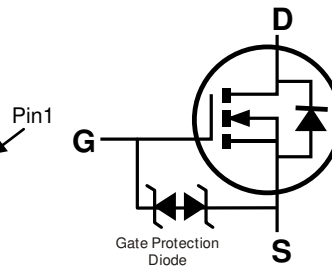
PowerDI5060-8 (SWP) (Type Q)



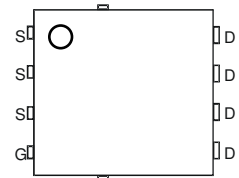
Top View



Bottom View



Internal Schematic



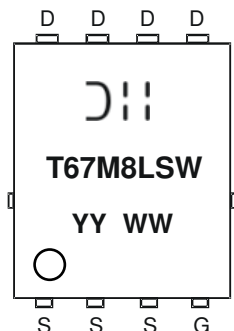
Top View  
Pin Configuration

## Ordering Information (Note 4)

Part Number	Case	Packaging
DMT67M8LPSW-13	PowerDI5060-8 (SWP) (Type Q)	2500 / Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



DII = Manufacturer's Marking  
 T67M8LSW = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY = Last Two Digits of Year (ex: 19 = 2019)  
 WW = Week Code (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	60	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = 10V	I <sub>D</sub>	T <sub>A</sub> = +25°C	17.3
		T <sub>A</sub> = +70°C	13.8
Continuous Drain Current (Note 6) V <sub>GS</sub> = 10V	I <sub>D</sub>	T <sub>C</sub> = +25°C	82
		T <sub>C</sub> = +70°C	65.6
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	320	A
Maximum Continuous Body Diode Forward Current (Note 6)	I <sub>S</sub>	82	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)	I <sub>SM</sub>	320	A
Avalanche Current, L = 0.3mH	I <sub>AS</sub>	23.7	A
Avalanche Energy, L = 0.3mH	E <sub>AS</sub>	84.5	mJ

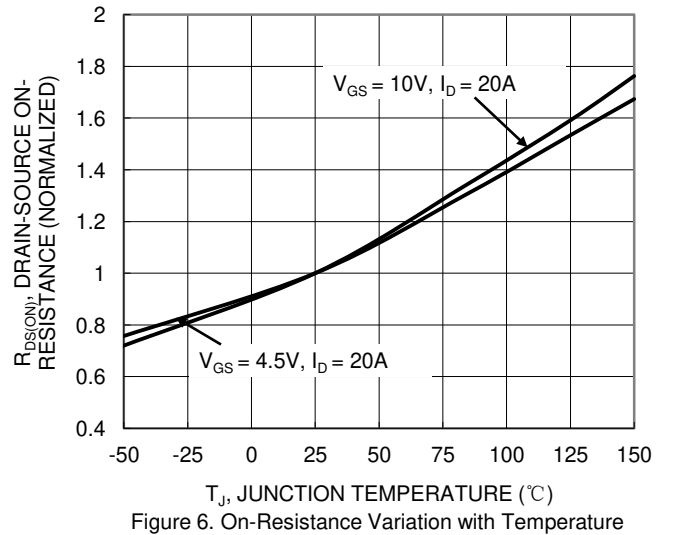
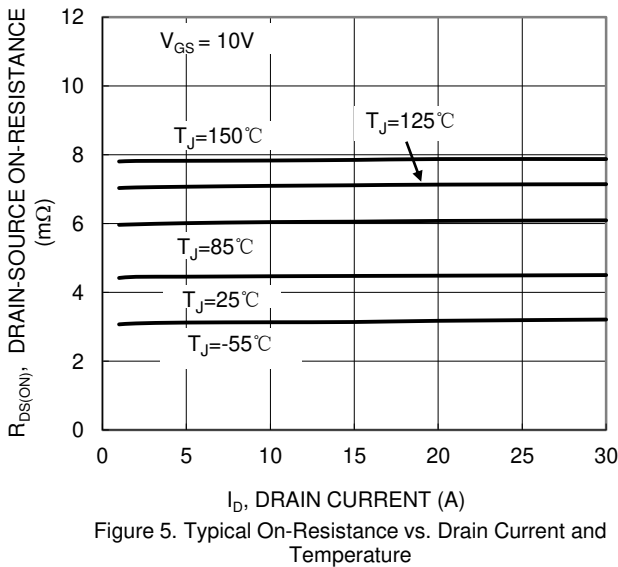
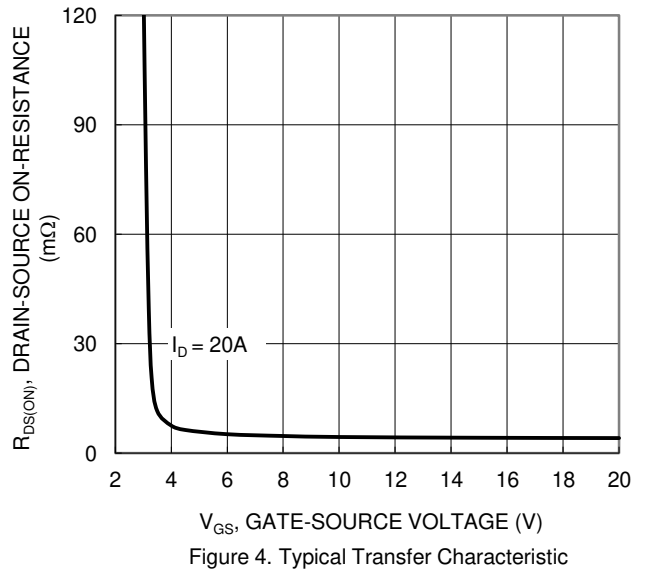
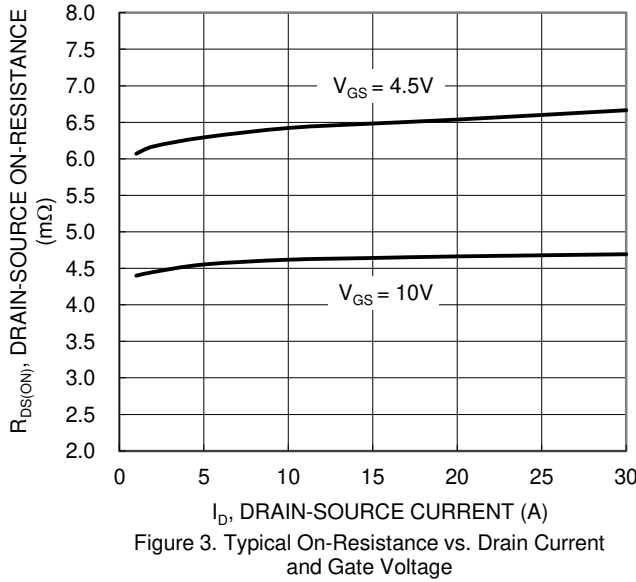
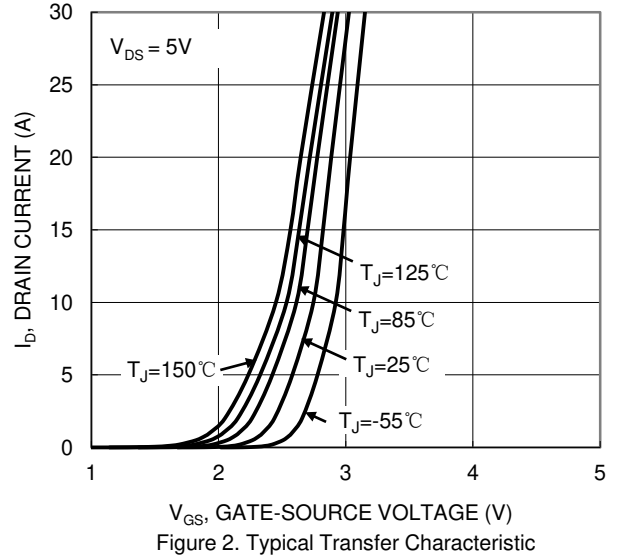
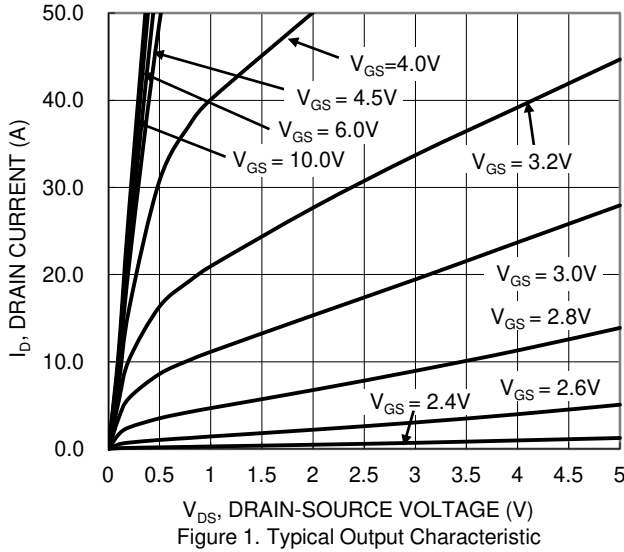
**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	2.8	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	45	°C/W
Total Power Dissipation (Note 6)	P <sub>D</sub>	62.5	W
Thermal Resistance, Junction to Case (Note 6)	R <sub>θJC</sub>	2	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1mA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	µA	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±10	µA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1.2	1.64	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	4.4	6.2	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A
		—	6.2	8.5		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 20A
Diode Forward Voltage	V <sub>SD</sub>	—	0.7	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iSS</sub>	—	2130	—	pF	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V, f = 1MHz
Output Capacitance	C <sub>oSS</sub>	—	786	—		
Reverse Transfer Capacitance	C <sub>rSS</sub>	—	70	—		
Gate Resistance	R <sub>g</sub>	—	0.6	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	—	20	—	nC	V <sub>DS</sub> = 30V, I <sub>D</sub> = 20A
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	—	37.5	—		
Gate-Source Charge	Q <sub>gs</sub>	—	5.4	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	9.5	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	5.5	—	ns	V <sub>DD</sub> = 30V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A, R <sub>g</sub> = 3Ω
Turn-On Rise Time	t <sub>R</sub>	—	6.8	—		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	22.1	—		
Turn-Off Fall Time	t <sub>F</sub>	—	10.8	—		
Reverse Recovery Time	t <sub>RR</sub>	—	26.9	—	ns	I <sub>F</sub> = 20A, di/dt = 300A/µs
Reverse Recovery Charge	Q <sub>RR</sub>	—	56.8	—		

- Notes:
- Device mounted on FR-4 substrate PCB, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
  - Thermal resistance from junction to soldering point (on the exposed drain pad).
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to product testing.



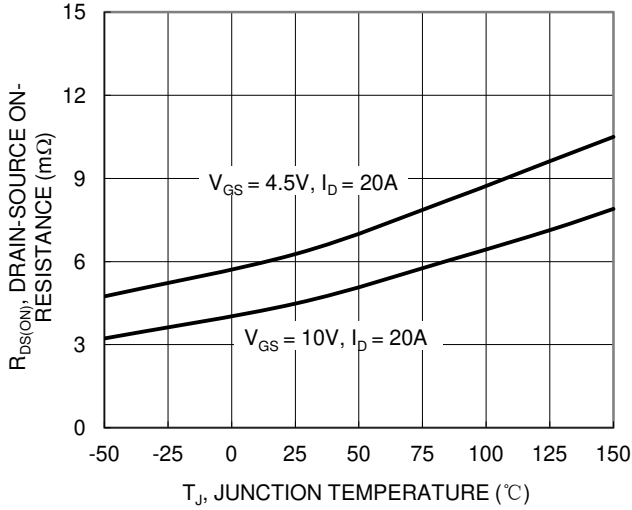


Figure 7. On-Resistance Variation with Temperature

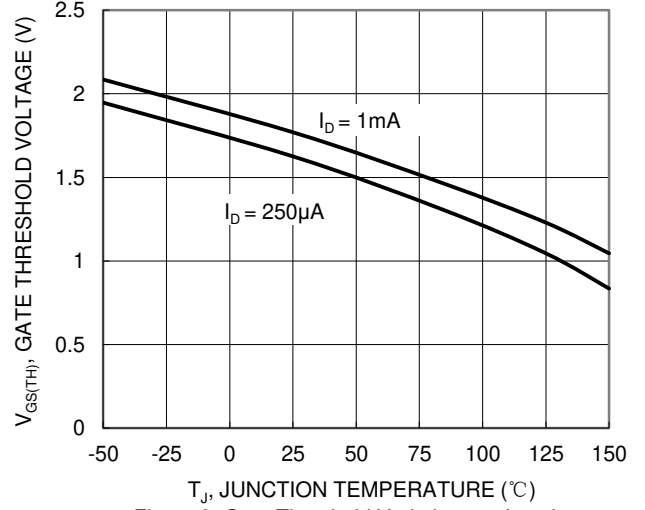


Figure 8. Gate Threshold Variation vs. Junction Temperature

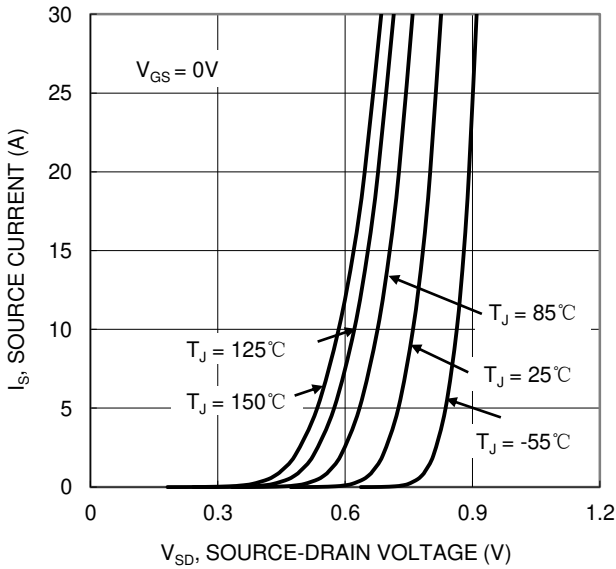


Figure 9. Diode Forward Voltage vs. Current

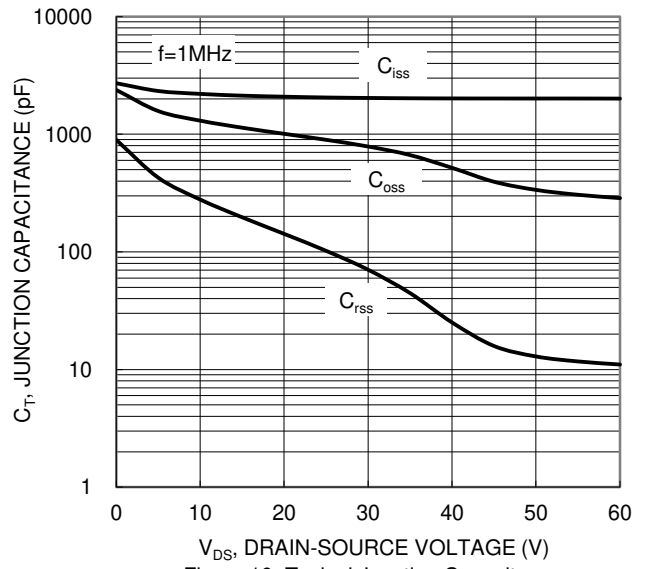


Figure 10. Typical Junction Capacitance

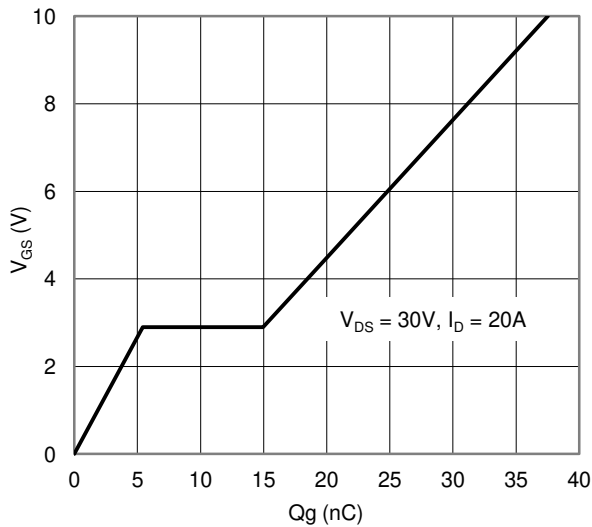


Figure 11. Gate Charge

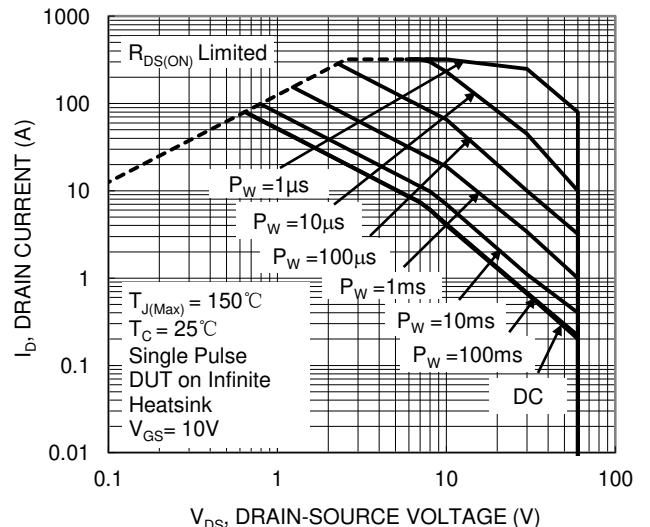


Figure 12. SOA, Safe Operation Area

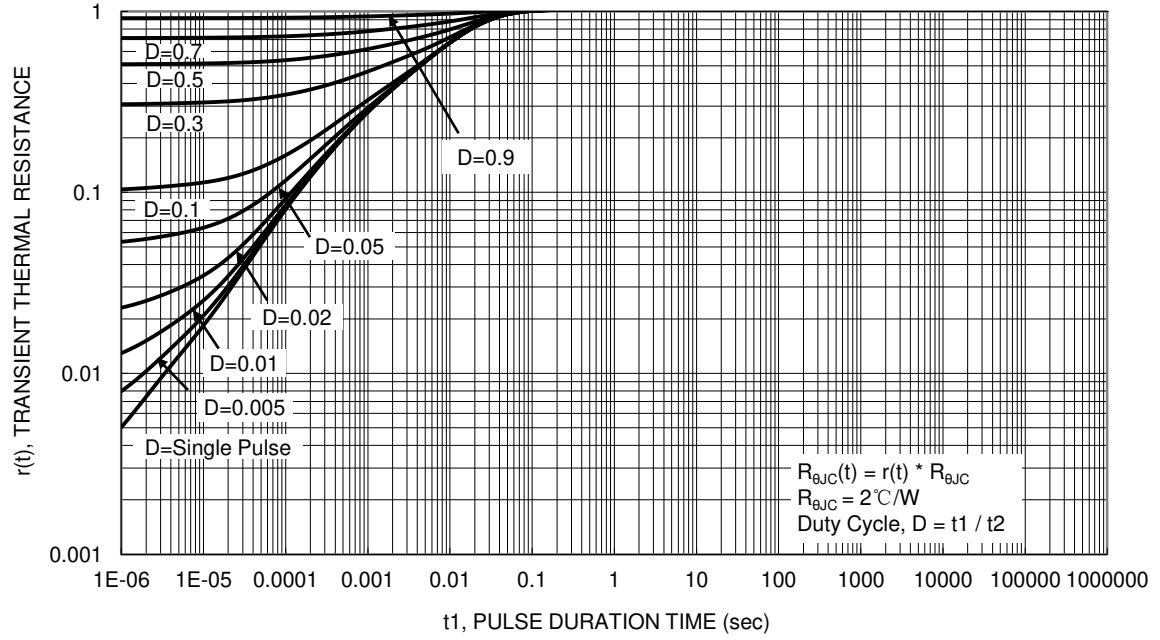
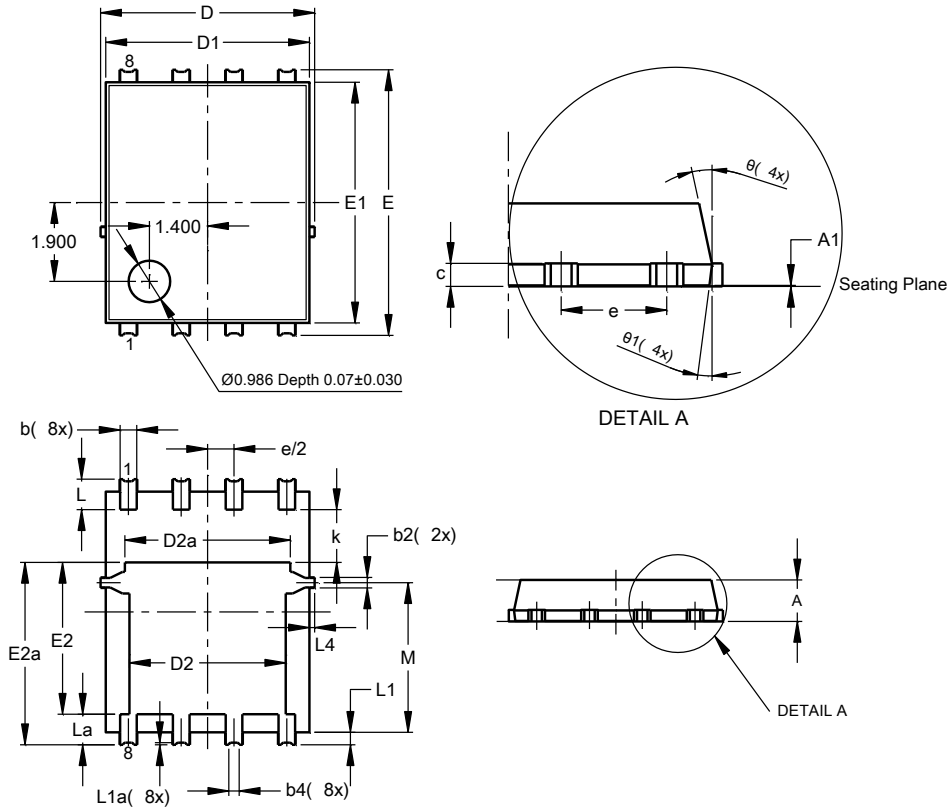


Figure 13. Transient Thermal Resistance

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI5060-8 (SWP) (Type Q)**

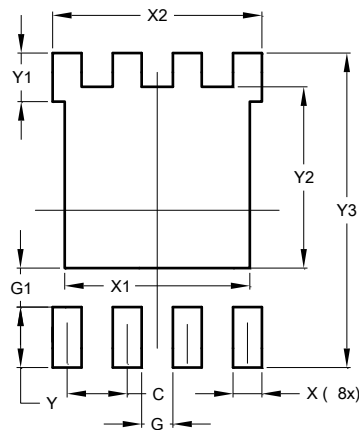


PowerDI5060-8 (SWP) (Type Q)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI5060-8 (SWP) (Type Q)**



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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