Dual, Wide Bandwidth Analog Switches

Features

- Single-Supply Operation (+2V to +6V)
- Rail-to-Rail Analog Signal Dynamic Range
- Low On-Resistance (7.2-Ohms with 5V supply) Minimizes Distortion and Error Voltages
- On-Resistance Flatness, 3Ohm typ.
- Low Charge Injection Reduces Glitch Errors. Q = 1.6pC typ.
- High Speed. t_{ON} = 7ns typ.
- Wide –3dB Bandwidth: 326 MHz
- High-Current Channel Capability: >100mA
- TTL/CMOS Logic Compatible
- Low Power Consumption (5µW typ.)
- Small MSOP-8 package minimizes board area

Applications

- Audio, Video Switching and Routing
- Battery-Powered Communication Systems
- Computer Peripherals
- Telecommunications
- Portable Instrumentation
- Mechanical Relay Replacement
- Cell Phones
- PDAs

Description

The PI5A126/PI5A127 are dual SPST (single-pole single-throw) analog switches designed for single supply operation. These high-precision devices are ideal for low-distortion audio, video, signal switching and routing.

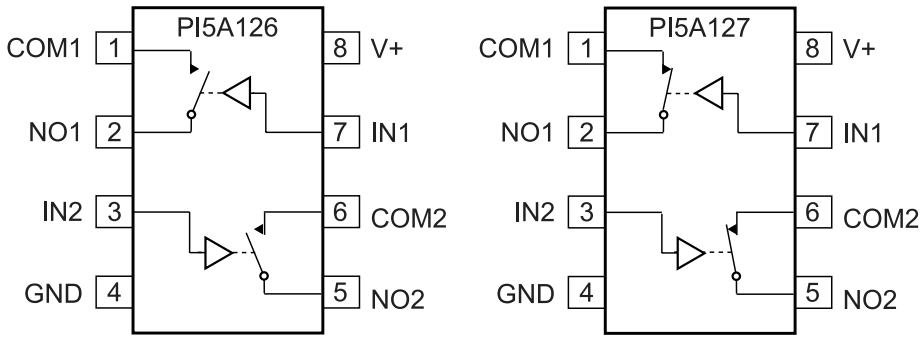
The PI5A126 is a normally open (NO) switch. The switch is open when IN is LOW. The PI5A127 is a normally closed (NC) switch.

Each switch conducts current equally well in either direction when on. When off, they block voltages up to V+.

These switches are fully specified with +5V and +3.3V supplies. With +5V, they guarantee <10 -ohm ON-resistance. On-resistance matching between channels is within 2 ohms. On-resistance flatness is less than 5 ohms over the specified range. These switches also guarantee fast switching speeds (t_{ON} < 20ns).

These products are available in 8-pin SOIC and MSOP plastic packages for operation over the industrial temperature range (–40°C to +85°C).

Functional Diagrams, Pin Configurations and Truth Tables



Top View

Switches shown for logic "0" input

Logic	PI5A126	PI5A127
1	ON	OFF
0	OFF	ON

Absolute Maximum Ratings

Voltages Referenced to GND
V_+ ..... –0.5V to +7V
V_{IN}, V_{COM}, V_{NC}, V_{NO} (Note 1) ..... –0.5V to V++2V
..... or 30mA, whichever occurs first
Current (any terminal except COM,NO,NC) 30mA
Current, COM, NO, NC 100mA
(Pulsed at 1ms, 10% duty cycle) 120mA

Thermal Information

Continuous Power Dissipation
-6 (derate 7mW/ºC above +70ºC) 550mW
Storage Temperature ..... –65°C to +150ºC
Lead Temperature (soldering, 10s) ..... +300ºC

Note 1:
Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +5V Supply

(V+ = +5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp. (°C)	Min.(2)	Typ.(1)	Max.(2)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}		Full	0		V+	V
On Resistance	R_{ON}	V+ = 4.5V, I_{COM} = –30mA, V_{NO} or V_{NC} = +2.5V	25		7.2	10	Ω
			Full			12	
On-Resistance Match Between Channels(4)	ΔR_{ON}		25		0.20	2	
			Full			4	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V+ = 5V, I_{COM} = –30mA, V_{NO} or V_{NC} = 1V, 2.5V, 4V	25		2.72	3.5	
			Full			4	
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 0V, V_{NO} or V_{NC} = 4.5V	25		0.18		nA
			Full	–200		200	
COM Off Leakage Current(6)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = + 4.5V, V_{NO} or V_{NC} = ± 0V	25		0.20		
			Full	–200		200	
COM On Leakage Current(6)	$I_{COM(ON)}$	V+ = 5.5V , V_{COM} = +4.5V V_{NO} or V_{NC} = +4.5V	25		0.20		
			Full	–200		200	

Electrical Specifications - Single +5V Supply (continued)

(V+ = + 5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Logic Input							
Input High Voltage	V_{IH}	Guaranteed logic High Level	Full	2			V
Input Low Voltage	V_{IL}	Guaranteed logic Low Level				0.8	
Input Current with Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V		–1	0.005	1	
Input Current with Voltage Low	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		–1	0.005	1	
Dynamic							
Turn-On Time	t_{ON}	V_{CC} = 5V, Figure 1	25		7	15	ns
			Full			20	
Turn-Off Time	t_{OFF}		25		1	7	
			Full			10	
Charge Injection(3)	Q	C_L = 1nF, Vgen = 0V, Rgen = 0Ω, Figure 2	25		1.6	10	pC
Off Isolation	OIRR	R_L = 50Ω, C_L = 5pF, f = 10MHz, Figure 3			–43		dB
Crosstalk	Xtalk	R_L = 50Ω, C_L = 5pF, f = 10 MHz, Figure 4			–43		
NC or NO Capacitance	C(off)	f = 1kHz, Figure 5			5.5		pF
COM Off Capacitance	Ccom(off)				5.5		
COM On Capacitance	Ccom(on)	f = 1kHz, Figure 6			13		
-3dB Bandwidth	BW	R_L = 50Ω, Figure 7	Full		326		MHz
Distortion	D	R_L = 10			0.2		%
Supply							
Power-Supply Range	V+		Full	2		6	V
Positve Supply Current	I+	V+ = 5.5V, V_{IN} = 0V or V_{CC}, V+ All Channels on or off				1	µA

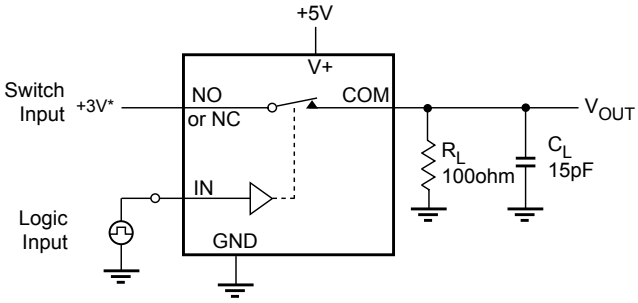
Notes:

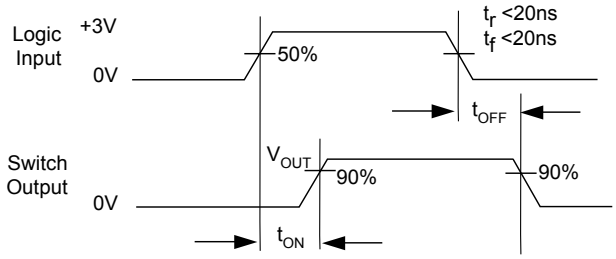
1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of ON-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 3.

Electrical Specifications - Single +3.3V Supply ($V+ = +3.3V \pm 10\%$, GND = 0V, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$)

Parameter	Symbol	Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ = 3V, I_{COM} = –30mA, V_{NO} or V_{NC} = 1.5V	25		12	18	Ω
			Full			22	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 3.3V, I_{COM} = –30mA, V_{NO} or V_{NC} = 0.8V, 2.5V	25		1	1	
			Full			2	
On-Resistance Flatness(3,5)	$R_{FLAT(ON)}$		25		3.5	4	
			Full			5	
Dynamic							
Turn-On Time	t_{ON}	V+ = 3.3V, V_{NO} or V_{NC} = 1.5V, Figure 1	25		14	25	ns
			Full			40	
Turn-Off Time	t_{OFF}		25		4.5	12	
			Full			20	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		1.3	10	pC
Supply							
Supply Current	I+	V+ = 3.6V, V_{IN} = 0V or V+ All Channels on or off	Full			1	∝A

Test Circuits/Timing Diagrams



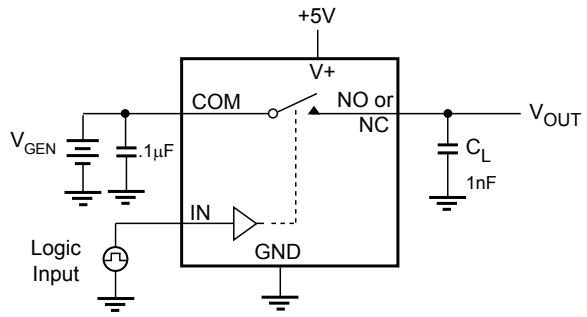


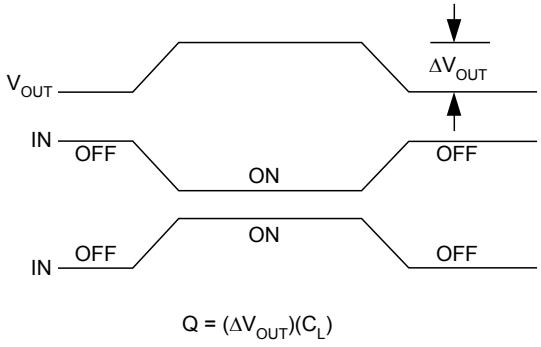
C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

$$V_{OUT} = V_{NO}\left(\frac{R_L}{R_{L+}R_{ON}}\right)$$

LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC
* 1.5V FOR 3.3V SUPPLY

Figure 1. Switching Time





$$Q = (\Delta V_{OUT})(C_L)$$

Figure 2. Charge Injection

Test Circuits/Timing Diagrams (continued)

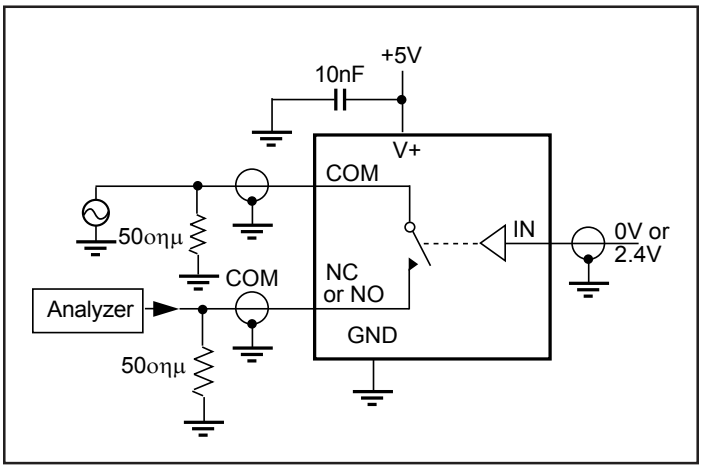


Figure 3. Off Isolation

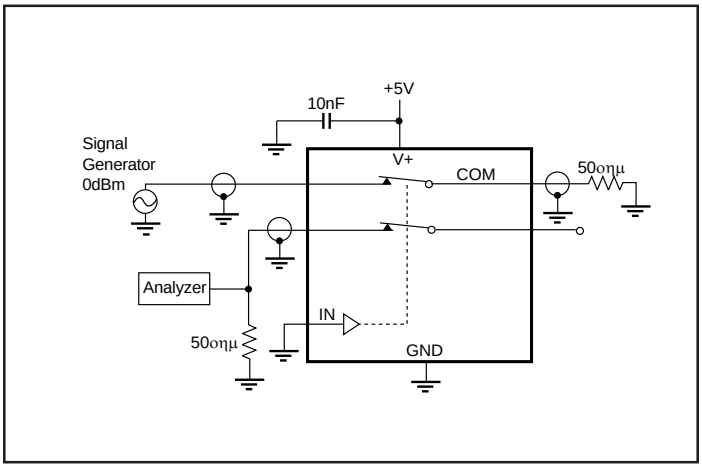


Figure 4. Crosstalk

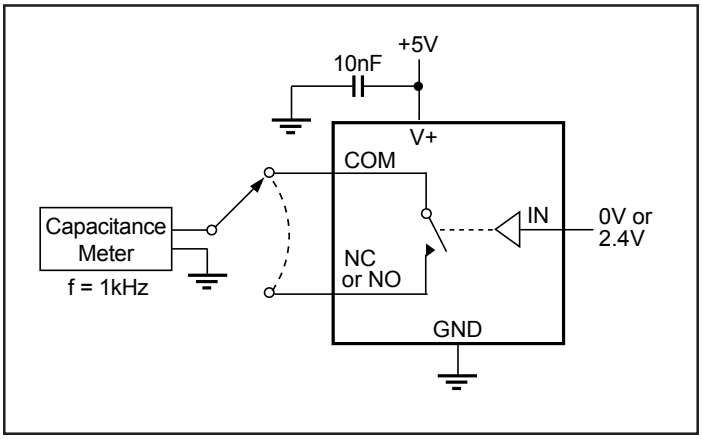


Figure 5. Channel-Off Capacitance

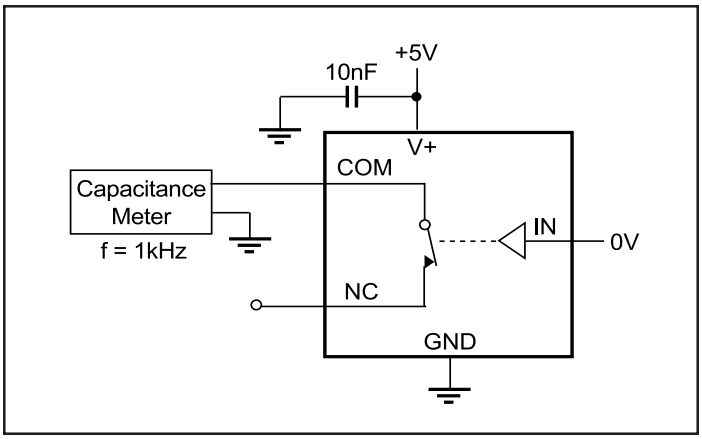


Figure 6. Channel-On Capacitance

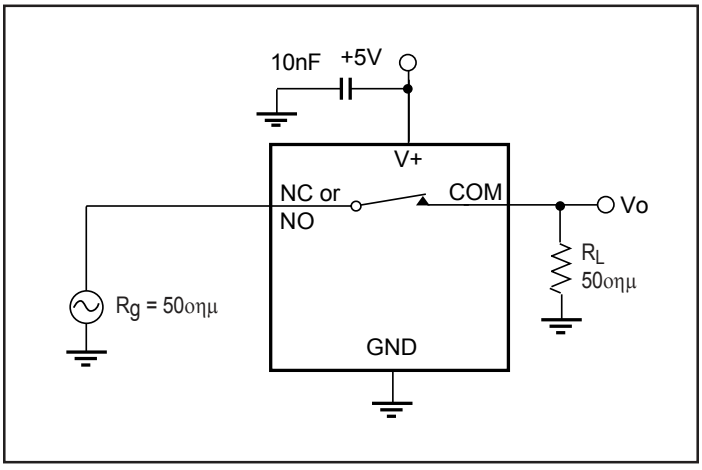


Figure 7. Bandwidth

Ordering Information

P/N	Package
PI5A126W	Narrow SOIC-8
PI5A126UX	MSOP-8
PI5A127W	Narrow SOIC-8
PI5A127UX	MSOP-8