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Kind regards,

Team Nexperia

### INTEGRATED CIRCUITS

## DATA SHEET

# **74F00**Quad 2-input NAND gate

Product specification

1990 Oct 04

IC15 Data Handbook





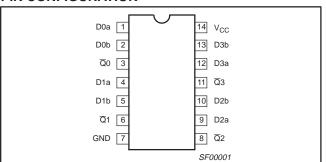
74F00

#### **FEATURE**

• Industrial temperature range available (-40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F00	3.4ns	4.4mA

### **PIN CONFIGURATION**



### **ORDERING INFORMATION**

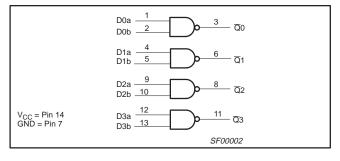
	C	ORDER CODE	
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to +70°C	INDUSTRIAL RANGE $V_{CC}$ = 5V ±10%, $T_{amb}$ = -40°C to +85°C	PKG DWG #
14-pin plastic DIP	N74F00N	174F00N	SOT27-1
14-pin plastic SO	N74F00D	I74F00D	SOT108-1

### INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
Qn	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

### **LOGIC DIAGRAM**



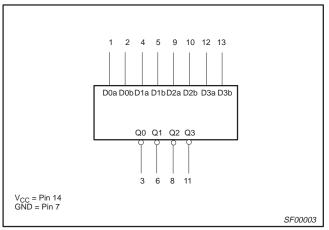
### **FUNCTION TABLE**

INP	UTS	OUTPUT
Dna	Dnb	Qn
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

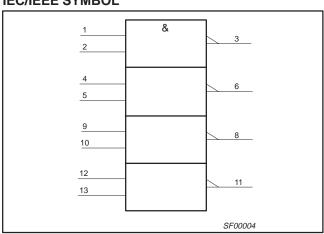
### NOTES:

H = High voltage level L = Low voltage level

### **LOGIC SYMBOL**



### **IEC/IEEE SYMBOL**



74F00

#### ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V <sub>CC</sub>	Supply voltage		−0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V	
I <sub>IN</sub>	Input current		-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in high output state	–0.5 to V <sub>CC</sub>	V	
I <sub>OUT</sub>	Current applied to output in low output state		40	mA
T <sub>amb</sub>	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T <sub>stg</sub>	Storage temperature range	-	-65 to +150	°C

### **RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	PARAMETER						
			MIN	NOM	MAX			
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V			
V <sub>IH</sub>	High-level input voltage	2.0			V			
$V_{IL}$	Low-level input voltage			0.8	V			
I <sub>Ik</sub>	Input clamp current				-18	mA		
I <sub>OH</sub>	High-level output current				-1	mA		
I <sub>OL</sub>	Low-level output current				20	mA		
T <sub>amb</sub>	Operating free air temperature range	Commercial range	0		+70	°C		
		Industrial range	-40		+85	°C		

### DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITION	NS <sup>1</sup>		LIMITS		UNIT
					MIN	TYP <sup>2</sup>	MAX	
V <sub>OH</sub>	High-level output voltage		$V_{CC} = MIN, V_{IL} = MAX$	±10%V <sub>CC</sub>	2.5			V
			V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±5%V <sub>CC</sub>	2.7	3.4		V
V <sub>OL</sub>	Low-level output voltage		$V_{CC} = MIN, V_{IL} = MAX$	±10%V <sub>CC</sub>		0.30	0.50	V
			$V_{IH} = MIN, I_{OI} = MAX$		0.30	0.50	V	
V <sub>IK</sub>	Input clamp voltage		$V_{CC} = MIN, I_I = I_{IK}$		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum voltage	input	$V_{CC} = MAX, V_I = 7.0V$				100	μΑ
I <sub>IH</sub>	High-level input current		$V_{CC} = MAX, V_I = 2.7V$				20	μΑ
I <sub>IL</sub>	Low-level input current		$V_{CC} = MAX, V_I = 0.5V$				-0.6	mA
Ios	Short-circuit output curren	ıt <sup>3</sup>	$V_{CC} = MAX$	-60		-150	mA	
Icc	Supply current (total)	I <sub>CCH</sub>	$V_{CC} = MAX$	V <sub>IN</sub> = GND	·	1.9	2.8	mA
		I <sub>CCL</sub>	$V_{CC} = MAX$	V <sub>IN</sub> = 4.5V	·	6.8	10.2	mA

### NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
   All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- 3. Not more than one output should be shorted at a time. For testing IOS, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{\mbox{\scriptsize OS}}$  tests should be performed last.

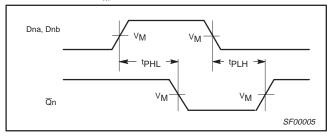
74F00

#### **AC ELECTRICAL CHARACTERISTICS**

			LIMITS							
SYMBOL	PARAMETER	TEST CONDITION	$V_{CC}$ = +5.0V $T_{amb}$ = +25°C $C_L$ = 50pF, $R_L$ = 500 $\Omega$			T <sub>amb</sub> = 0°0	0V ± 10% C to +70°C R <sub>L</sub> = 500Ω	$V_{CC} = +5.$ $T_{amb} = -40^{\circ}$ $C_{L} = 50 pF$	UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dna, Dnb to Qn	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	2.0 1.5	6.5 6.0	ns

### **AC WAVEFORMS**

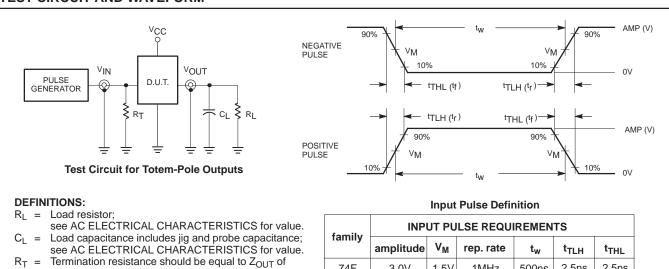
For all waveforms,  $V_M = 1.5V$ .



Waveform 1. Propagation delay for inverting outputs

### **TEST CIRCUIT AND WAVEFORM**

pulse generators.



74F

3.0V

1.5V

1MHz

500ns

2.5ns

SF00006

2.5ns

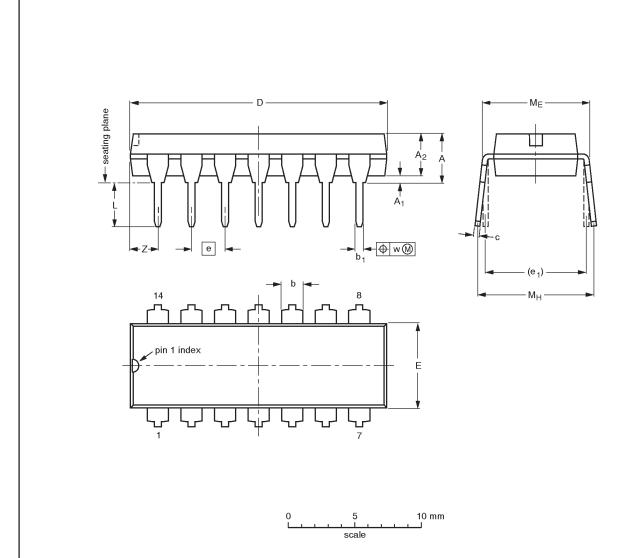
Philips Semiconductors Product specification

### Quad 2-input NAND gate

74F00

### DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	e <sub>1</sub>	L	ME	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

#### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

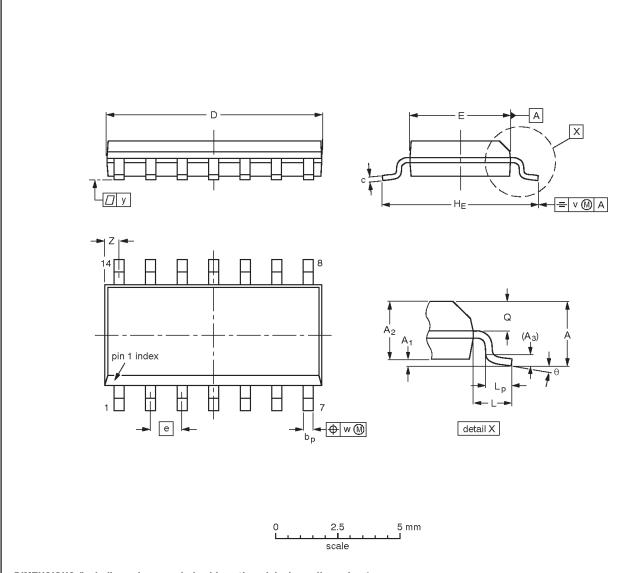
OUTLINE REFERENCES				EUROPEAN	ISSUE DATE		
VERSION	VERSION IEC		EIAJ	PROJECTION	ISSUE DATE		
SOT27-1	050G04	MO-001AA				<del>92-11-17</del> 95-03-11	

1990 Oct 04 5

74F00

### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	А3	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075		0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

### Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT108-1	076E06S	MS-012AB				<del>95-01-23</del> 97-05-22

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Philips Semiconductors Product specification

### Quad 2-input NAND gate

74F00

**NOTES** 

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#### Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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<sup>[1]</sup> Please consult the most recently issued datasheet before initiating or completing a design.

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