FAST CMOS 1-TO-10 CLOCK DRIVER

IDT74FCT807BT/CT

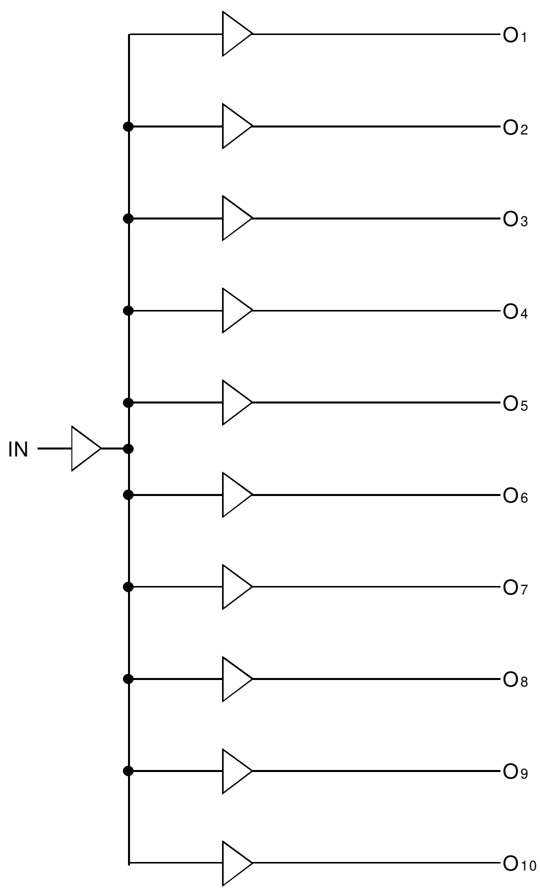
FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 250ps (max.)
- Very low duty cycle distortion < 350ps (max.)
- High speed: propagation delay < 2.5ns (max.)
- 100MHz operation
- TTL compatible inputs and outputs
- TTL level output voltage swings
- 1:10 fanout
- Output rise and fall time < 1.5ns (max)
- Low input capacitance: 4.5pF typical
- High drive: -32mA I_{OH}, +48mA I_{OL}
- Available in QSOP, SSOP, and SOIC packages

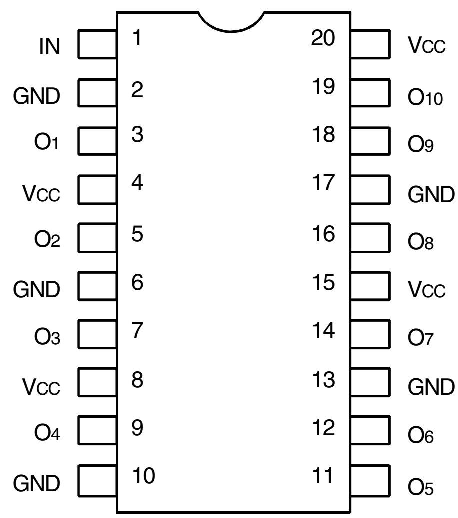
DESCRIPTION:

The FCT807T clock driver is built using advanced dual metal CMOS technology. This low skew clock driver features 1:10 fanout, providing minimal loading on the preceding drivers. The FCT807T offers low capacitance inputs with hysteresis for improved noise margins. TTL level outputs and multiple power and grounds reduce noise. The device also features -32/48mA drive capability for driving low impedance traces.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP/ SOIC/ SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
IN	Inputs
Ox	Outputs

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, Industrial: T_A = -40°C to +85°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current (Input pins)	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current(4)	V_{CC} = Max., V_O = GND(3)		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –15mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –32mA	2	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	—	0.3	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤4.5V		—	—	±1	µA
V_H	Input Hysteresis for all inputs	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[3]	V_{CC} = Max. Input Toggling 50% Duty Cycle Outputs Open	V_{IN} = V_{CC} V_{IN} = GND	—	0.4	0.6	mA/MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Input Toggling 50% Duty Cycle Outputs Open f_I = 50MHz	V_{IN} = V_{CC} V_{IN} = GND	—	20	30.5[4]	mA
			V_{IN} = 3.4V V_{IN} = GND	—	20.3	31.3[4]	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$

   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})

   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

   D_H = Duty Cycle for TTL Inputs High

   N_T = Number of TTL Inputs at D_H

   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

   f_O = Output Frequency

   N_O = Number of Outputs at f_O

   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL(3,4)

Symbol	Parameter	Conditions(1)	FCT807BT Min.(2)	FCT807BT Max.	FCT807CT Min.(2)	FCT807CT Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay	50Ω to $V_{CC}/2$, C_L = 10pF (See figure 1) or 50Ω ac termination, C_L = 10pF (See figure 2) f ≤100MHz Outputs connected in groups of two	1.3	2.7	1.3	2.5	ns
t_R	Output Rise Time		—	1.5	—	1.5	ns
t_F	Output Fall Time		—	1.5	—	1.5	ns
$t_{SK(O)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.25	ns
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)		—	0.5	—	0.35	ns
$t_{SK(T)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	0.9	—	0.65	ns

Symbol	Parameter	Conditions(1)	FCT807BT Min.(2)	FCT807BT Max.	FCT807CT Min.(2)	FCT807CT Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay	C_L = 30pF f ≤67MHz (See figure 3)	1.5	3.8	1.5	3.5	ns
t_R	Output Rise Time		—	1.5	—	1.5	ns
t_F	Output Fall Time		—	1.5	—	1.5	ns
$t_{SK(O)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.25	ns
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)		—	0.5	—	0.35	ns
$t_{SK(T)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	0.9	—	0.75	ns

Symbol	Parameter	Conditions(1)	FCT807BT Min.(2)	FCT807BT Max.	FCT807CT Min.(2)	FCT807CT Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay	C_L = 30pF f ≤40MHz (See figure 4)	1.5	3.8	1.5	3.5	ns
t_R	Output Rise Time		—	1.5	—	1.5	ns
t_F	Output Fall Time		—	1.5	—	1.5	ns
$t_{SK(O)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.35	ns
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)		—	0.6	—	0.45	ns
$t_{SK(T)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1	—	0.75	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK}(t)$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL(3,4)

Symbol	Parameter	Conditions(1)	FCT807BT Min.(2)	FCT807BT Max.	FCT807CT Min.(2)	FCT807CT Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay	50Ω to $V_{CC}/2$, C_L = 10pF (See figure 1) or 50Ω ac termination, C_L = 10pF (See figure 2) f ≤100MHz Outputs connected in groups of two	1.3	2.9	1.3	2.7	ns
t_R	Output Rise Time		—	1.5	—	1.5	ns
t_F	Output Fall Time		—	1.5	—	1.5	ns
$t_{SK(O)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.35	ns
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)		—	0.6	—	0.45	ns
$t_{SK(T)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	0.9	—	0.65	ns

Symbol	Parameter	Conditions(1)	FCT807BT Min.(2)	FCT807BT Max.	FCT807CT Min.(2)	FCT807CT Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay	C_L = 30pF f ≤67MHz (See figure 3)	1.5	4	1.5	3.7	ns
t_R	Output Rise Time		—	1.5	—	1.5	ns
t_F	Output Fall Time		—	1.5	—	1.5	ns
$t_{SK(O)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.35	ns
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)		—	0.6	—	0.45	ns
$t_{SK(T)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	0.9	—	0.75	ns

Symbol	Parameter	Conditions(1)	FCT807BT Min.(2)	FCT807BT Max.	FCT807CT Min.(2)	FCT807CT Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay	C_L = 30pF f ≤40MHz (See figure 4)	1.5	4	1.5	3.7	ns
t_R	Output Rise Time		—	1.5	—	1.5	ns
t_F	Output Fall Time		—	1.5	—	1.5	ns
$t_{SK(O)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.45	ns
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)		—	0.7	—	0.55	ns
$t_{SK(T)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1	—	0.75	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK}(t)$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS

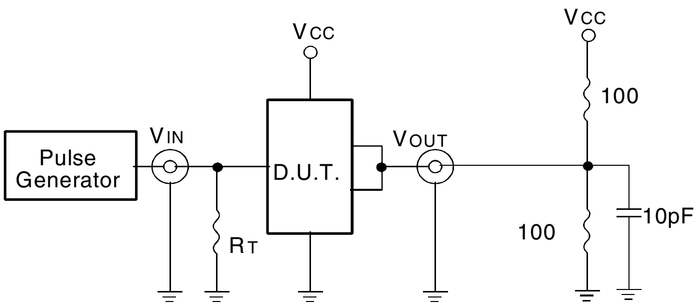


Fig. 1: 50Ω to VCC/2, CL = 10pF

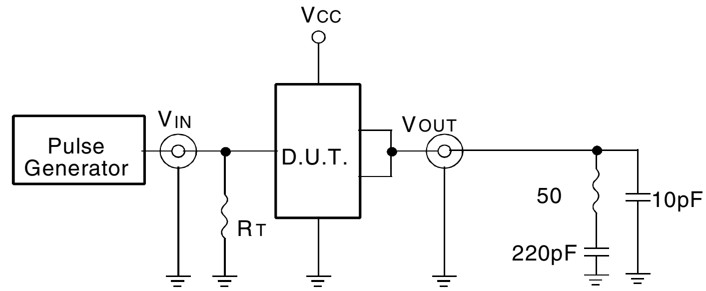


Fig. 2: 50Ω AC Termination, CL = 10pF

The capacitor value for AC termination is determined by the operating frequency. For very low frequencies a higher capacitor value should be selected.

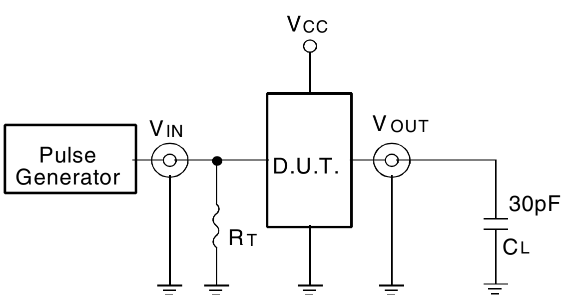


Fig. 3: CL = 30pF Circuit

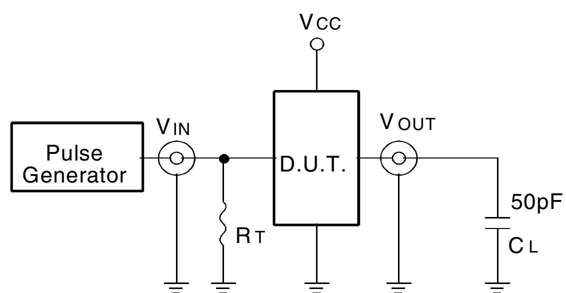


Fig. 4: CL = 50pF Circuit

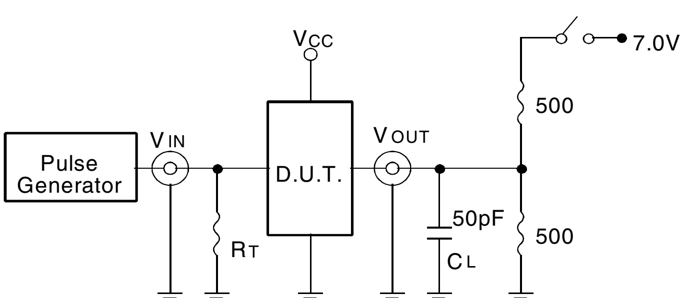


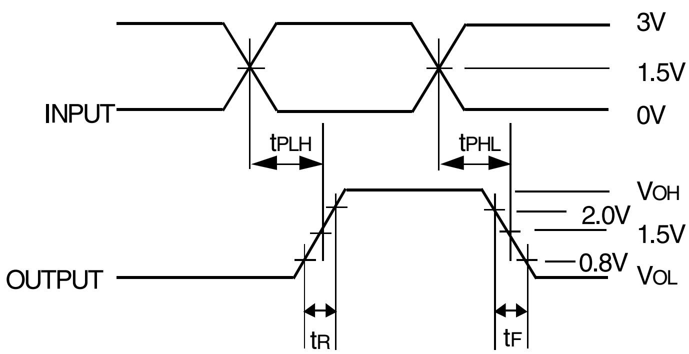
Fig. 5: Enable and Disable Time Circuit

SWITCH POSITION

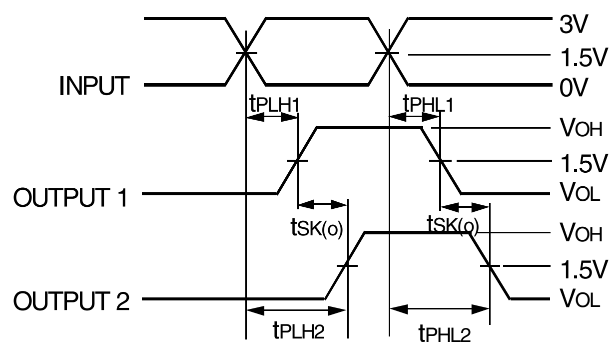
Test	Switch
Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

TEST WAVEFORMS

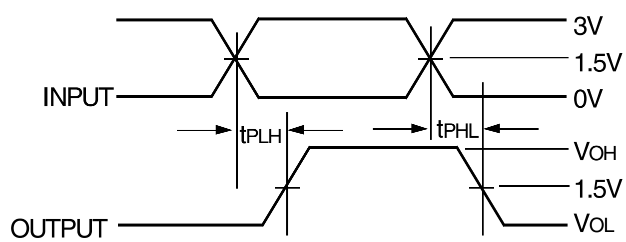


Package Delay



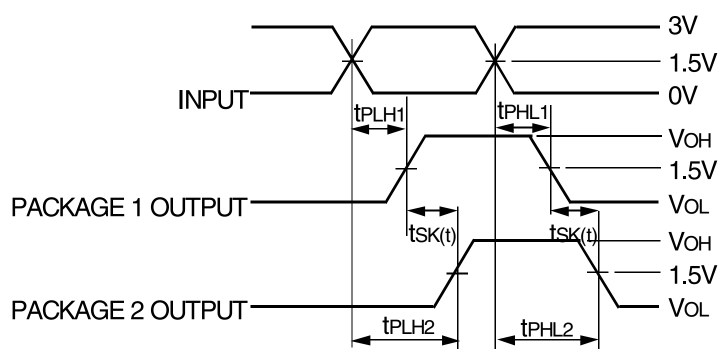
$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Output Skew - $t_{SK(O)}$



$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

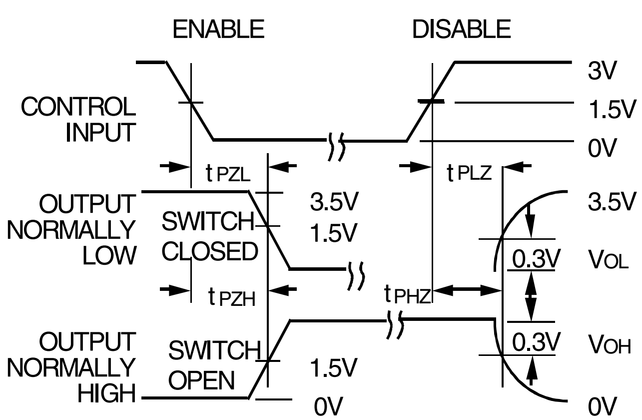
Pulse Skew - $t_{SK(P)}$



$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Part-to-Part Skew - $t_{SK(T)}$

NOTE:
1. Package 1 and Package 2 are same device type and speed grade.



Enable and Disable Times

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤1.0MHz; t_F ≤2.5ns; t_R ≤2.5ns

ORDERING INFORMATION

[redacted]74FCT XXXX X X

Device Type / Package / Temp. Range

Temp. Range

Blank	Commercial (0°C to +70°C)
I	Industrial (-40°C to +85°C)

Package

[redacted]

SOG	SOIC - Green

[redacted]

PYG	SSOP - Green

[redacted]

QG	QSOP - Green

Device Type

807BT 807CT	1-to-10 Clock Driver

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