

# FAST CMOS 1-TO-10 CLOCK DRIVER

# IDT74FCT807BT/CT

## **FEATURES:**

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 250ps (max.)
- Very low duty cycle distortion < 350ps (max.)
- High speed: propagation delay < 2.5ns (max.)
- 100MHz operation
- · TTL compatible inputs and outputs
- TTL level output voltage swings
- 1:10 fanout
- Output rise and fall time < 1.5ns (max)
- · Low input capacitance: 4.5pF typical
- High drive: -32mA IoH, +48mA IoL
- · Available in QSOP, SSOP, and SOIC packages

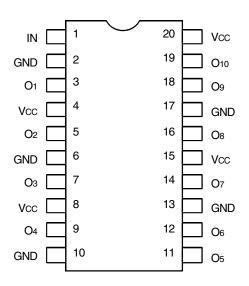
## **DESCRIPTION:**

The FCT807T clock driver is built using advanced dual metal CMOS technology. This low skew clock driver features 1:10 fanout, providing minimal loading on the preceding drivers. The FCT807T offers low capacitance inputs with hysteresis for improved noise margins. TTL level outputs and multiple power and grounds reduce noise. The device also features -32/48mA drive capability for driving low impedance traces.

# FUNCTIONAL BLOCK DIAGRAM

# O1 O2 O2 O3 O3 O4 O6 O7 O8 O9 O9

# **PIN CONFIGURATION**



QSOP/ SOIC/ SSOP TOP VIEW

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COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES

MAY 2010

# ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +7	V
Tstg	Storage Temperature	-65 to +150	°C
lout	DC Output Current	-60 to +120	mA

#### NOTE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause
permanent damage to the device. This is a stress rating only and functional operation
of the device at these or any other conditions above those indicated in the operational
sections of this specification is not implied. Exposure to absolute maximum rating
conditions for extended periods may affect reliability.

# CAPACITANCE ( $T_A = +25^{\circ}C$ , f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Тур.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	рF
Соит	Output Capacitance	Vout = 0V	5.5	8	рF

#### NOTE:

1. This parameter is measured at characterization but not tested.

## **PIN DESCRIPTION**

Pin Names	Description
IN	Inputs
Ох	Outputs

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA =  $0^{\circ}$ C to  $+70^{\circ}$ C, Industrial: TA =  $-40^{\circ}$ C to  $+85^{\circ}$ C, Vcc = 5V  $\pm$  5%

Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
Input HIGH Level (Input pins)	Guaranteed Logic HIGH	Level	2	_	_	V
Input LOW Level	Guaranteed Logic LOW	Level	_	_	0.8	V
Input HIGH Current (Input pins)	Vcc = Max.	VI = 2.7V	_	_	±1	μΑ
Input LOW Current (Input pins)	Vcc = Max.	VI = 0.5V	_	_	±1	μΑ
High Impedance Output Current	Vcc = Max.	Vo = 2.7V	_	_	±1	μА
(3-State Output pins)		Vo = 0.5V	_	_	±1	]
Input HIGH Current	Vcc = Max., VI = Vcc	(Max.)	_	_	±1	μА
Clamp Diode Voltage	VCC = Min., IIN = -18m	Vcc = Min., IIN = -18mA		-0.7	-1.2	V
Short Circuit Current <sup>(4)</sup>	Vcc = Max., Vo = GNE	<b>)</b> (3)	-60	-120	-225	mA
Output HIGH Voltage	Vcc = Min.	Iон = −15mA	2.4	3.3	_	V
	VIN = VIH or VIL	Iон = -32mA	2	3	_	1
Output LOW Voltage	Vcc = Min.	IoL = 48mA	_	0.3	0.55	V
	VIN = VIH or VIL					
Input/Output Power Off Leakage	VCC = 0V, VIN or VO ≤	4.5V	_	_	±1	μА
Input Hysteresis for all inputs	_	_		150	_	mV
Quiescent Power Supply Current	Vcc = Max., Vin = GNE	Vcc = Max., Vin = GND or Vcc		5	500	μА
	Input HIGH Level (Input pins) Input LOW Level Input HIGH Current (Input pins) Input LOW Current (Input pins) High Impedance Output Current (3-State Output pins) Input HIGH Current Clamp Diode Voltage Short Circuit Current <sup>(4)</sup> Output HIGH Voltage Output LOW Voltage Input/Output Power Off Leakage Input Hysteresis for all inputs	Input HIGH Level (Input pins)  Input LOW Level  Input HIGH Current (Input pins)  Input LOW Current (Input pins)  Input LOW Current (Input pins)  Input LOW Current (Input pins)  Vcc = Max.  High Impedance Output Current  (3-State Output pins)  Input HIGH Current  Vcc = Max., VI = Vcc  Clamp Diode Voltage  Vcc = Min., In = −18m/  Vcc = Min.  Vin = Vih or Vil.  Input High Voltage  Vcc = OV, Vin or Vo ≤  Input Hysteresis for all inputs  —	Input HIGH Level (Input pins)       Guaranteed Logic HIGH Level         Input LOW Level       Guaranteed Logic LOW Level         Input HIGH Current (Input pins)       Vcc = Max.       VI = 2.7V         Input LOW Current (Input pins)       Vcc = Max.       VI = 0.5V         High Impedance Output Current (3-State Output pins)       Vcc = Max.       Vo = 2.7V         Input HIGH Current       Vcc = Max., VI = Vcc (Max.)         Clamp Diode Voltage       Vcc = Min., In = -18mA         Short Circuit Current(4)       Vcc = Min.       IOH = -15mA         Output HIGH Voltage       Vcc = Min.       IOH = -32mA         Output LOW Voltage       Vcc = Min.       IOL = 48mA         VIN = VIH or VIL       Input Youtput Power Off Leakage       Vcc = 0V, VIN or Vo ≤4.5V         Input Hysteresis for all inputs       —	Input HIGH Level (Input pins)   Guaranteed Logic HIGH Level   2	Input HIGH Level (Input pins)   Guaranteed Logic HIGH Level   2	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

- 1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- 2. Typical values are at Vcc = 5V, +25°C ambient.
- 3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- 4. Duration of the condition should not exceed one second.

# POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Con	ditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
Δlcc	Quiescent Power Supply Current	Vcc = Max.		_	0.5	2	mA
	TTL Inputs HIGH	VIN = 3.4V	_				
ICCD	Dynamic Power Supply Current <sup>(3)</sup>	Vcc = Max.	VIN = VCC	_	0.4	0.6	mA/MHz
		Input Toggling	VIN = GND				
		50% Duty Cycle					
		Outputs Open					
Ic	Total Power Supply Current <sup>(5)</sup>	Vcc = Max.	VIN = VCC	_	20	30.5 <sup>(4)</sup>	mA
		Input Toggling	VIN = GND				
		50% Duty Cycle					
		Outputs Open	VIN = 3.4V	_	20.3	31.3 <sup>(4)</sup>	
		fı = 50MHz	VIN = GND				

- 1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- 2. Typical values are at Vcc = 5V, +25°C ambient.
- 3. Per TTL driven input (VIN = 3.4V); all other inputs at Vcc or GND.
- 4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- 5. Values for these conditions are examples of the lc formula. These limits are guaranteed but not tested.
- 6. IC = IQUIESCENT + INPUTS + IDYNAMIC
  - $IC = ICC + \Delta ICC DHNT + ICCD (foNo)$
  - Icc = Quiescent Current (IccL, IccH and Iccz)
  - $\Delta Icc$  = Power Supply Current for a TTL High Input (VIN = 3.4V)
  - DH = Duty Cycle for TTL Inputs High
  - NT = Number of TTL Inputs at DH
  - ICCD = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
  - fo = Output Frequency
  - No = Number of Outputs at fo
  - All currents are in milliamps and all frequencies are in megahertz.

# SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL (3,4)

			FCT8	07BT	FCT8	807CT	
Symbol	Parameter	Conditions <sup>(1)</sup>	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Unit
tPLH tPHL	Propagation Delay	$50\Omega$ to Vcc/2, CL = 10pF	1.3	2.7	1.3	2.5	ns
tR	Output Rise Time	(See figure 1) or 50Ωac	_	1.5	_	1.5	ns
tF	Output Fall Time	termination,	_	1.5	_	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)	CL = 10pF (See figure 2)	_	0.5	_	0.25	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( tphl-tplh )	f ≤100MHz Outputs connected in groups of two	_	0.5	_	0.35	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	groups of two	_	0.9	_	0.65	ns

			FCT8	807BT	FCT8	07CT	
Symbol	Parameter	Conditions <sup>(1)</sup>	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Unit
tPLH	Propagation Delay	CL = 30pF	1.5	3.8	1.5	3.5	ns
tPHL		f ≤67MHz					
tR	Output Rise Time	(See figure 3)	_	1.5	_	1.5	ns
tF	Output Fall Time		_	1.5	_	1.5	ns
tsk(o)	Output skew: skew between outputs of all banks of		_	0.5	_	0.25	ns
	same package (inputs tied together)						
tsk(P)	Pulse skew: skew between opposite transitions		_	0.5	_	0.35	ns
	of same output ( tPHL—tPLH )						
tsk(T)	Package skew: skew between outputs of different		_	0.9	_	0.75	ns
	packages at same power supply voltage,						
	temperature, package type and speed grade						

			FCT8	07BT	FCT8	07CT	
Symbol	Parameter	Conditions <sup>(1)</sup>	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Unit
tPLH .	Propagation Delay	CL = 30pF f ≤40MHz	1.5	3.8	1.5	3.5	ns
tPHL		-					
tR	Output Rise Time	(See figure 4)	_	1.5	_	1.5	ns
tF	Output Fall Time		_	1.5	_	1.5	ns
tsk(o)	Output skew: skew between outputs of all banks of		_	0.5	_	0.35	ns
	same package (inputs tied together)						
tsk(P)	Pulse skew: skew between opposite transitions		_	0.6	_	0.45	ns
	of same output ( tPHL-tPLH )						
tsk(T)	Package skew: skew between outputs of different		_	1	_	0.75	ns
	packages at same power supply voltage,						
	temperature, package type and speed grade						

- 1. See test circuits and waveforms.
- 2. Minimum limits are guaranteed but not tested on Propagation Delays.
- 3. tPLH, tPHL, tSK(t) are production tested. All other parameters guaranteed but not production tested.
- 4. Propagation delay range indicated by Min. and Max. limit is due to Vcc, operating temperature and process parameters. These propagation delay limits do not imply skew.

# SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL (3,4)

			FCT8	07BT	FCT8	807CT	
Symbol	Parameter	Conditions <sup>(1)</sup>	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Unit
tPLH tPHL	Propagation Delay	$50\Omega$ to Vcc/2, CL = 10pF	1.3	2.9	1.3	2.7	ns
tR	Output Rise Time	(See figure 1) or 50Ωac	_	1.5	_	1.5	ns
tF	Output Fall Time	termination,  CL = 10pF  (See figure 2)	_	1.5		1.5	ns
tsk(0)	Output skew: skew between outputs of all banks of same package (inputs tied together)			0.6	_	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( tphl-tplh )	f ≤100MHz Outputs connected in groups of two		0.6	-	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	g. 3353 01 two	_	0.9	_	0.65	ns

			FCT8	807BT	FCT8	807CT	
Symbol	Parameter	Conditions <sup>(1)</sup>	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Unit
tPLH tPHL	Propagation Delay	CL = 30pF f ≤67MHz	1.5	4	1.5	3.7	ns
tr	Output Rise Time	(See figure 3)	_	1.5	_	1.5	ns
tF	Output Fall Time		_	1.5	_	1.5	ns
tsk(o)	Output skew: skew between outputs of all banks of same package (inputs tied together)		_	0.6	_	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( tphl-tplh )		_	0.6	_	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		_	0.9	_	0.75	ns

			FCT8	07BT	FCT8	07CT	
Symbol	Parameter	Conditions <sup>(1)</sup>	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Unit
tPLH	Propagation Delay	CL = 30pF	1.5	4	1.5	3.7	ns
tPHL		f ≤40MHz					
tR	Output Rise Time	(See figure 4)	_	1.5	_	1.5	ns
tF	Output Fall Time		_	1.5		1.5	ns
tsk(o)	Output skew: skew between outputs of all banks of		_	0.6	_	0.45	ns
	same package (inputs tied together)						
tsk(P)	Pulse skew: skew between opposite transitions		_	0.7	_	0.55	ns
	of same output ( tPHL—tPLH )						
tsk(T)	Package skew: skew between outputs of different		_	1	_	0.75	ns
	packages at same power supply voltage,						
	temperature, package type and speed grade						

- 1. See test circuits and waveforms.
- 3. tPLH, tPHL, tSK(t) are production tested. All other parameters guaranteed but not production tested.
- 4. Propagation delay range indicated by Min. and Max. limit is due to Vcc, operating temperature and process parameters. These propagation delay limits do not imply skew.

# **TEST CIRCUITS**

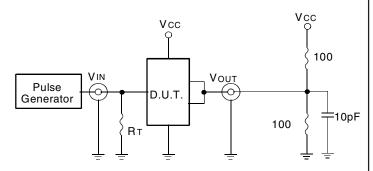


Fig. 1:  $50\Omega$  to Vcc/2, CL = 10pF

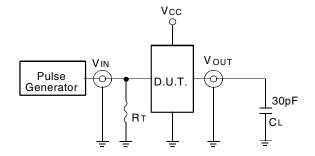


Fig. 3: CL = 30pF Circuit

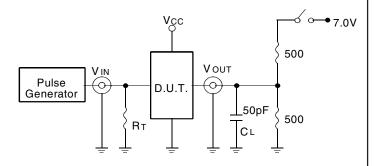


Fig. 5: Enable and Disable Time Circuit

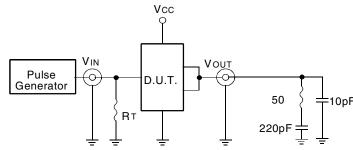


Fig. 2:  $50\Omega$  AC Termination, CL = 10pF

The capacitor value for AC termination is determined by the operating frequency. For very low frequencies a higher capacitor value should be selected.

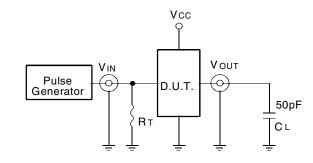


Fig. 4: CL = 50pF Circuit

# **SWITCH POSITION**

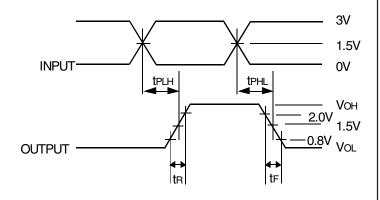
Test	Switch
Disable LOW	6V
Enable LOW	
Disable HIGH	GND
Enable HIGH	

#### **DEFINITIONS:**

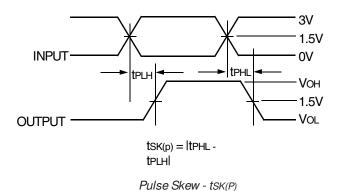
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to Zout of the Pulse Generator.

# **TEST WAVEFORMS**



Package Delay



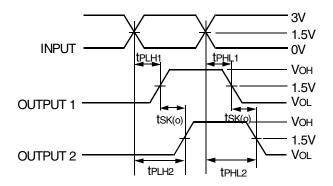
**ENABLE** DISABLE 3V CONTROL 1.5V **INPUT** 0V t PZL t PLZ **OUTPUT** 3.5V 3.5V SWITCH: **NORMALLY** 1.5V **CLOSED** LOW Vol **→** t PZH t PHZ **OUTPUT** 0.3V Vон **SWITCH NORMALLY** 1.5V **OPEN** HIGH 0V

# NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH

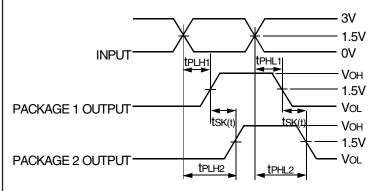
Enable and Disable Times

2. Pulse Generator for All Pulses: Rate  $\leq$ 1.0MHz; tF  $\leq$ 2.5ns; tR  $\leq$ 2.5ns



tSK(o) = |tPLH2 - tPLH1| or |tPHL2 - tPHL1|

Output Skew - tsk(0)



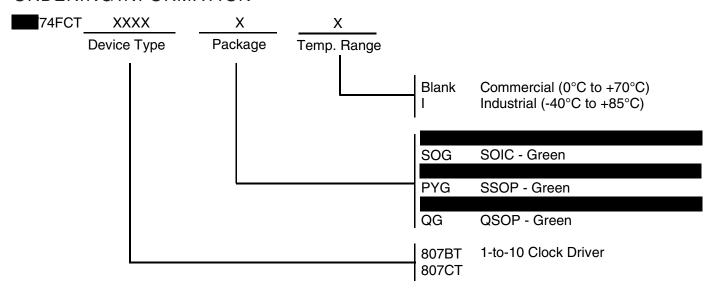
tSK(t) = |tPLH2 - tPLH1| or |tPHL2 - tPHL1|

Part-to-Part Skew - tsk(T)

#### NOTE:

1. Package 1 and Package 2 are same device type and speed grade.

# **ORDERING INFORMATION**



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