

Complementary Switch FET Drivers

 Check for Samples: [UC1714](#), [UC1715](#), [UC2714](#), [UC2715](#), [UC3714](#), [UC3715](#)

FEATURES

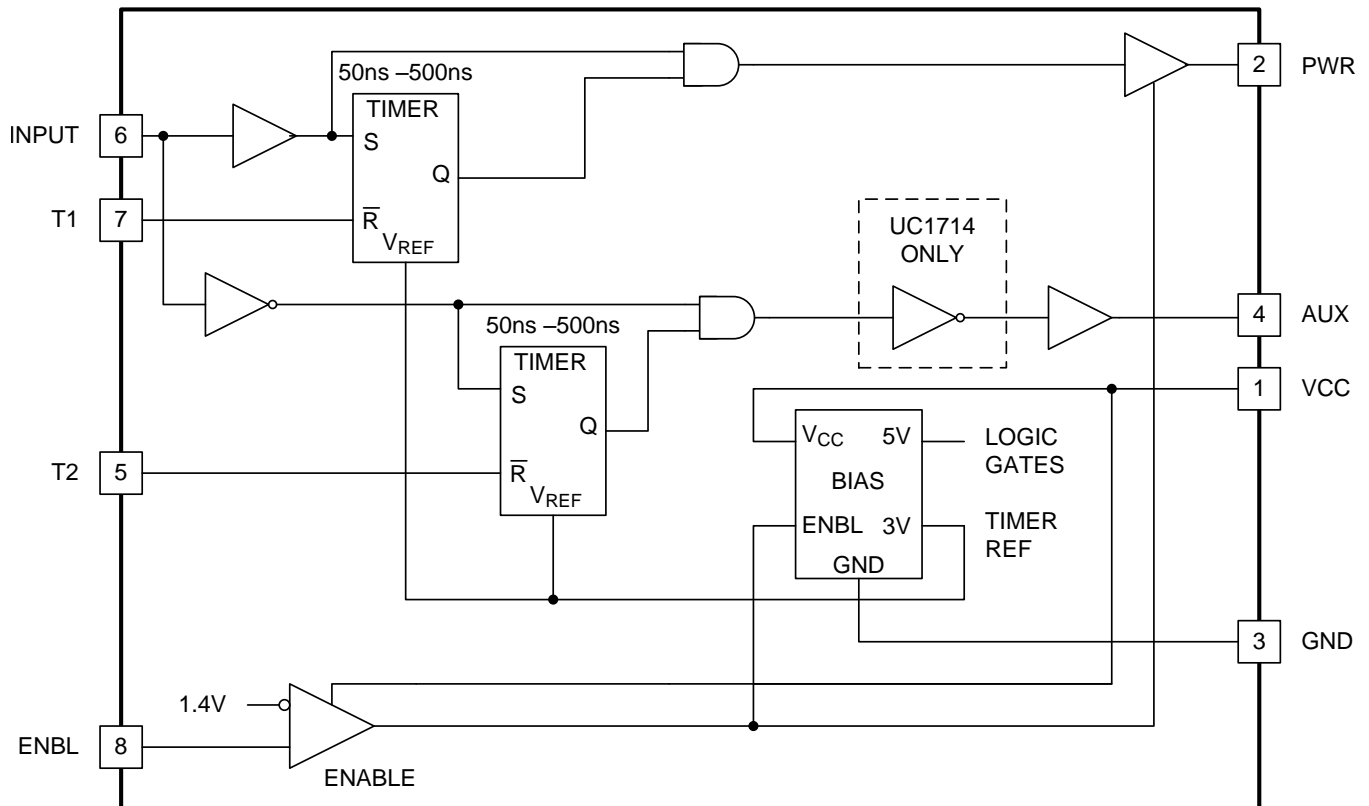
- **Single Input (PWM and TTL Compatible)**
- **High-Current Power FET Driver, 1-A Source and 2-A Sink**
- **Auxiliary Output FET Driver, 0.5-A Source and 1-A Sink**
- **Time Delays Between Power and Auxiliary Outputs Independently Programmable from 50 to 500-ns**
- **Time Delay or True Zero-Voltage Operation Independently Configurable for Each Output**
- **Switching Frequency to 1 MHz**
- **Typical 50-ns Propagation Delays**
- **ENBL Pin Activates 220- μ A Sleep Mode**
- **Power Output is Active-Low in Sleep Mode**
- **Synchronous Rectifier Driver**

DESCRIPTION

These two families of high speed drivers are designed to provide drive waveforms for complementary switches. Complementary switch configurations are commonly used in synchronous rectification circuits and active clamp/reset circuits, which provide zero voltage switching. In order to facilitate the soft switching transitions, independently programmable delays between the two output waveforms are provided on these drivers. The delay pins also have true-zero voltage-sensing capability which allows immediate activation of the corresponding switch when zero voltage is applied. These devices require a PWM-type input to operate and interface with commonly available PWM controllers.

In the UC1714 series, the AUX output is inverted to allow driving a p-channel MOSFET. In the UC1715 series, the two outputs are configured in a true complementary fashion.

BLOCK DIAGRAM



Pin numbers refer to J, N and D packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Auxiliary Driver IOH	continuous		-100	mA
	peak		-500	mA
Auxiliary Driver IOL	continuous		200	mA
	peak		1	A
Input Voltage Range (INPUT, ENBL)		-0.3	20	V
Power Driver IOH	continuous		-200	mA
	peak		-1	A
Power Driver IOL	continuous		400	mA
	peak		2	A
V _{CC}	Supply voltage		20	V
Lead Temperature (Soldering 10 seconds)			300	°C
Operating Junction Temperature ⁽³⁾			150	°C
Storage Temperature Range		-65	150	°C

- (1) Consult the Packaging Section at the end of this datasheet for thermal limitations and specifications of packages.
- (2) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (3) Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC} = 15 V, ENBL ≥ 2 V, R_{T1} = 100 kΩ from T1 to GND, R_{T2} = 100 kΩ from T2 to GND, and -55°C < T_A < 125°C for the UC1714 and UC1715, -40°C < T_A < 85°C for the UC2714 and UC2715, and 0°C < T_A < 70°C for the UC3714 and UC3715, T_A = T_J

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall						
V _{CC}			7		20	V
I _{CC}	Nominal	ENBL = 2 V		18	24	mA
	Sleep mode	ENBL = 0.8 V		200	300	μA
Power Driver (PWR)						
	Pre turn-on PWR output, low	V _{CC} = 0 V, I _{OUT} = 10 mA, ENBL at 0.8 V		0.3	1.6	V
V _{PWR}	PWR output low, sat.	INPUT = 0.8 V, I _{OUT} = 40 mA		0.3	0.8	V
		INPUT = 0.8 V, I _{OUT} = 400 mA		2.1	2.8	
V _{CC} - V _{PWR}	PWR output high, sat.	INPUT = 2 V, I _{OUT} = -20 mA		2.1	3	V
		INPUT = 2 V, I _{OUT} = -200 mA		2.3	3	
	Rise time	C _L = 2200 pF		30	60	ns
	Fall time	C _L = 2200 pF		25	60	ns
	T1 Delay, AUX to PWR	INPUT rising edge, R _{T1} = 10 kΩ ⁽¹⁾	20	35	80	ns
		INPUT rising edge, R _{T1} = 100 kΩ ⁽¹⁾	350	500	700	
	PWR Prop Delay	INPUT falling edge, 50% ⁽²⁾		35	100	ns
Auxiliary Driver (AUX)						
V _{AUX}	AUX output low, sat.	V _{IN} = 2 V, I _{OUT} = 20 mA		0.3	0.8	V
		V _{IN} = 2 V, I _{OUT} = 200 mA		1.8	2.6	
V _{CC} - V _{AUX}	AUX output high, sat.	V _{IN} = 0.8 V, I _{OUT} = -10 mA		2.1	3	V
		V _{IN} = 0.8 V, I _{OUT} = -100 mA		2.3	3	
	Rise Time	C _L = 1000 pF		45	60	ns

- (1) T1 delay is defined from the 50% point of the transition edge of AUX to the 10% of the rising edge of PWR. T2 delay is defined from the 90% of the falling edge of PWR to the 50% point of the transition edge of AUX.
- (2) Propagation delay times are measured from the 50% point of the input signal to the 10% point of the output signal's transition with no load on outputs.

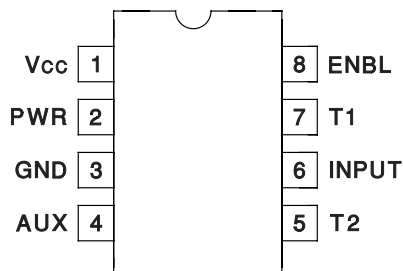
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, $V_{CC} = 15\text{ V}$, $ENBL \geq 2\text{ V}$, $R_{T1} = 100\text{ k}\Omega$ from T1 to GND, $R_{T2} = 100\text{ k}\Omega$ from T2 to GND, and $-55^\circ\text{C} < T_A < 125^\circ\text{C}$ for the UC1714 and UC1715, $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ for the UC2714 and UC2715, and $0^\circ\text{C} < T_A < 70^\circ\text{C}$ for the UC3714 and UC3715, $T_A = T_J$

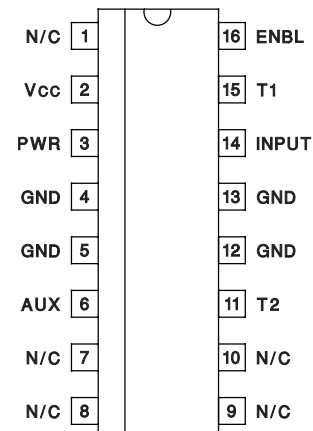
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Fall Time	$C_L = 1000\text{ pF}$		30	60	ns
	T2 Delay, PWR to AUX	INPUT falling edge, $R_{T2} = 10\text{ k}\Omega^{(1)}$	20	50	80	ns
		INPUT falling edge, $R_{T2} = 100\text{ k}\Omega^{(1)}$	250	350	550	
	AUX Prop Delay	INPUT rising edge, 50% ⁽²⁾		35	80	ns
Enable (ENBL)						
	Input Threshold		0.8	1.2	2	V
I_{IH}	Input Current	$ENBL = 15\text{ V}$		1	10	μA
I_{IL}	Input Current	$ENBL = 0\text{ V}$		-1	-10	μA
T1						
	Current Limit	$T1 = 0\text{ V}$		-1.6	-2	mA
	Nominal Voltage at T1		2.7	3	3.3	V
	Minimum T1 Delay	$T1 = 2.5\text{ V}^{(1)}$		40	70	ns
T2						
	Current Limit	$T2 = 0\text{ V}$		-1.2	-2	mA
	Nominal Voltage at T2		2.7	3	3.3	V
	Minimum T2 Delay	$T2 = 2.5\text{ V}^{(1)}$		50	100	ns
Input (INPUT)						
	Input Threshold		0.8	1.4	2	V
I_{IH}	Input Current	$INPUT = 15\text{ V}$		1	10	μA
I_{IL}	Input Current	$INPUT = 0\text{ V}$		-5	-20	μA

DEVICE INFORMATION

**DIL-8, SOIC-8; J or N, D Packages
(TOP VIEW)**



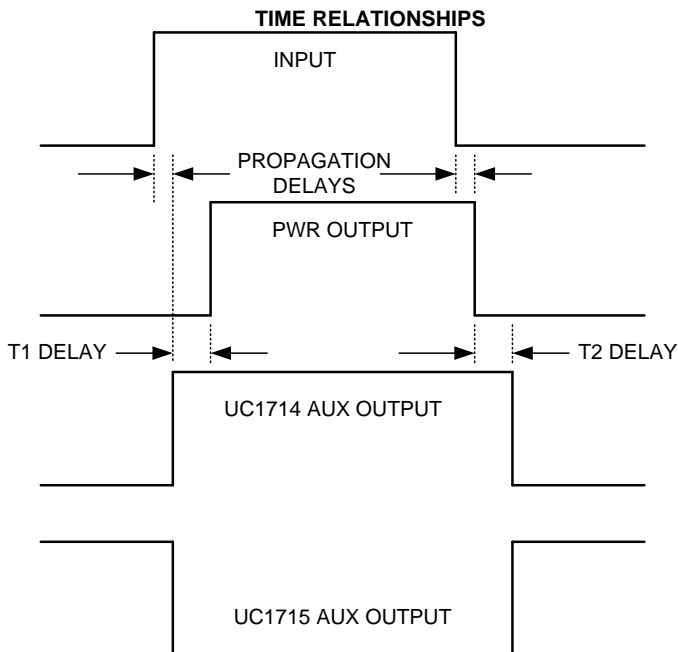
**SOIC-16; DP Package
(TOP VIEW)**



PIN DESCRIPTIONS

- AUX** The AUX switches immediately at the rising edge of INPUT but waits through the T2 delay after the falling edge of INPUT before switching. AUX is capable of sourcing 0.5 A and sinking 1 A of drive current. See the Time Relationships diagram below ([Figure 1](#)) for the differences between the UC1714 and UC1715 for INPUT, MAIN, and AUX. During sleep mode, AUX is inactive with a high impedance.
- ENBL** The ENBL input switches at TTL logic levels (approximately 1.2 V), and the input range is from 0 to 20 V. The ENBL input places the device into sleep mode when it is a logical low. The current into VCC during the sleep mode is typically 220 μ A.
- GND** This is the reference pin for all input voltages and the return point for all device currents. GND carries the full peak sinking current from the outputs. Any tendency for the outputs to ring below GND voltage must be damped or clamped such that GND remains the most negative potential.
- INPUT** The input switches at TTL logic levels (approximately 1.4 V) but the allowable range is from 0 to 20 V, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output.
Note that if the input signal comes from a controller with FET drive capability, this signal provides another option. INPUT and PWR provide a delay only at the leading edge while INPUT and AUX provide the delay at the trailing edge.
- PWR** The PWR output waits for the T1 delay after the rising edge of INPUT before switching on, but switches off immediately at the falling edge of INPUT (neglecting propagation delays). This output is capable of sourcing 1 A and sinking 2 A of peak gate-drive current. PWR output includes a passive, self-biased circuit which holds this pin active low, when $ENBL \leq 0.8V$ regardless of the voltage of VCC.
- T1** A resistor to ground programs the time delay between the AUX switch turnoff and PWR turnon.
- T2** This pin functions in the same way as T1 but controls the time delay between PWR turnoff and activation of the AUX switch.
- T1, T2** The resistor on each of these pins sets the charging current on internal timing capacitors to provide independent time control. The nominal voltage level at each pin is 3 V and the current is internally limited to 1 mA. The total delay from INPUT to each output includes a propagation delay in addition to the programmable timer but because the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays. The relationship of the time delay vs. RT is shown in the [TYPICAL CHARACTERISTICS](#) curves (see [Figure 2](#)). Either or both pins are alternatively used for voltage sensing in lieu of delay programming, which is done by pulling the timer pins below their nominal voltage level which immediately activates the timer output.
- VCC** The V_{CC} input range is from 7 to 20 V. This pin must be bypassed with a capacitor to GND consistent with peak load current demands.

TYPICAL CHARACTERISTICS



(2) T1 delay is defined from the 50% point of the transition edge of AUX to the 10% of the rising edge of PWR. T2 delay is defined from the 90% of the falling edge of PWR to the 50% point of the transition edge of AUX.

Figure 1.

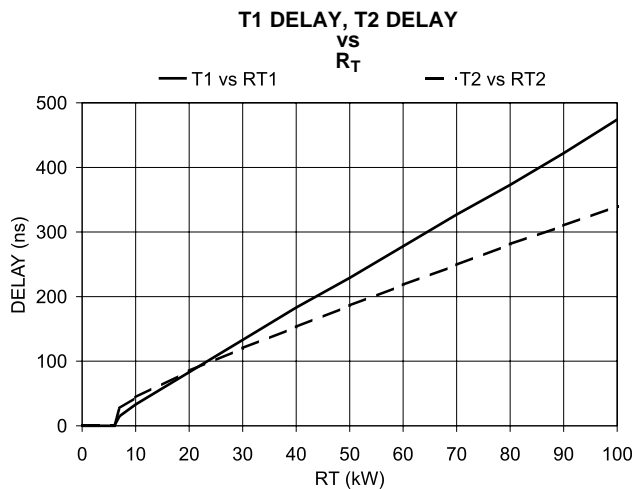


Figure 2.

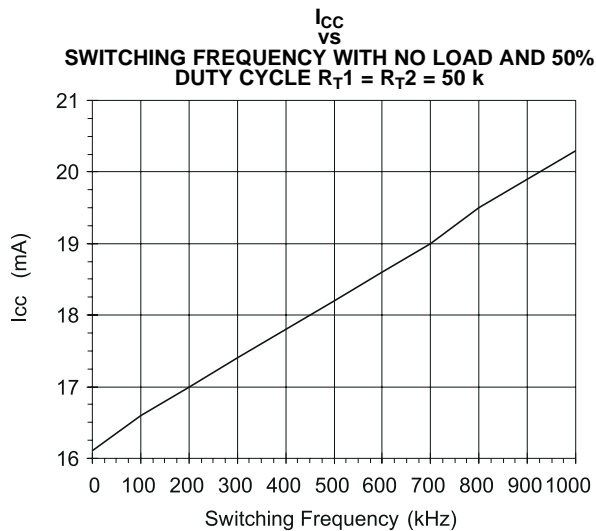


Figure 3.

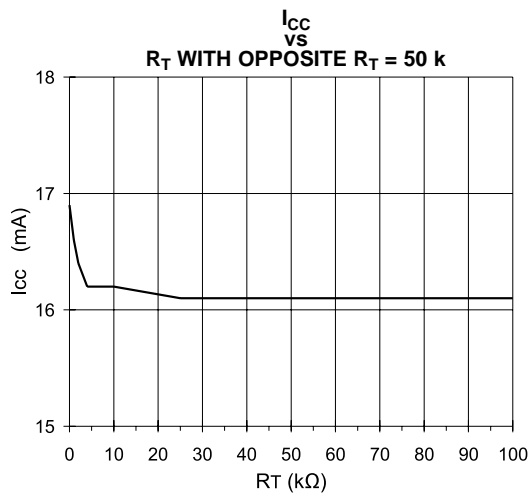


Figure 4.

TYPICAL CHARACTERISTICS (continued)

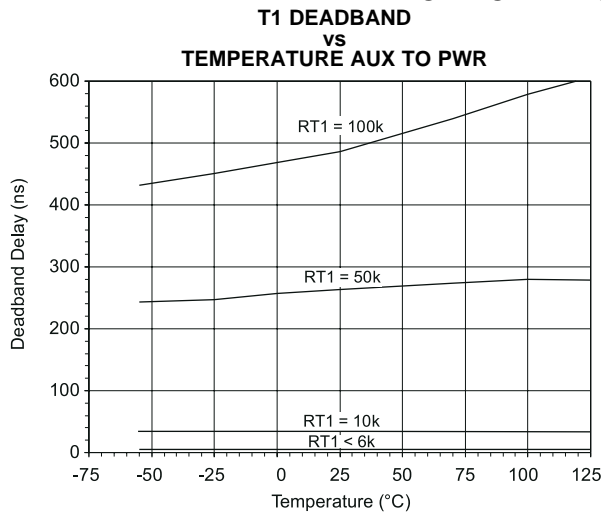


Figure 5.

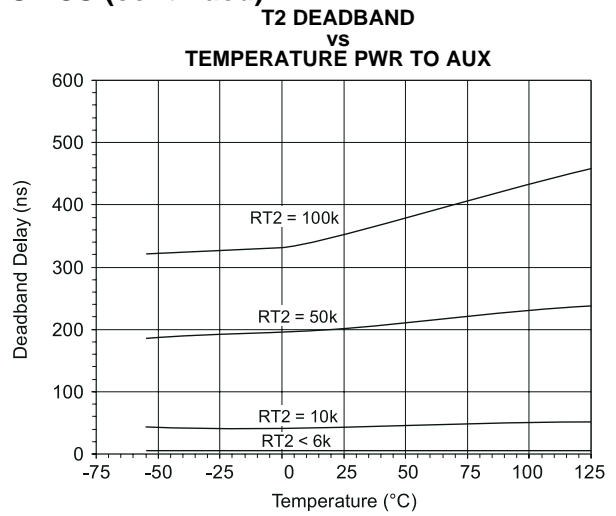


Figure 6.

TYPICAL APPLICATIONS

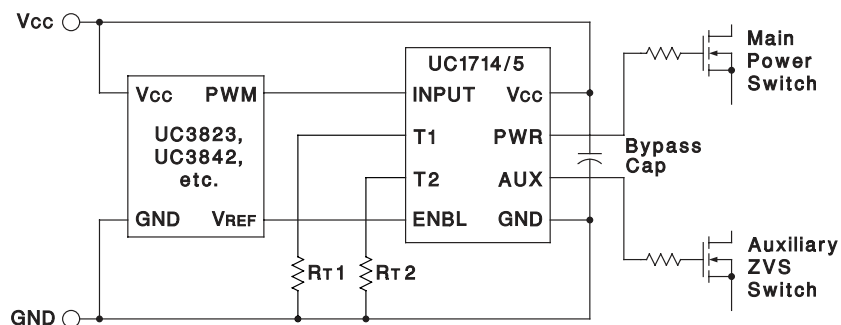


Figure 7. Typical Application With Timed Delays

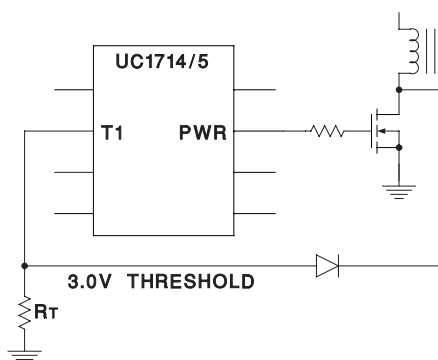
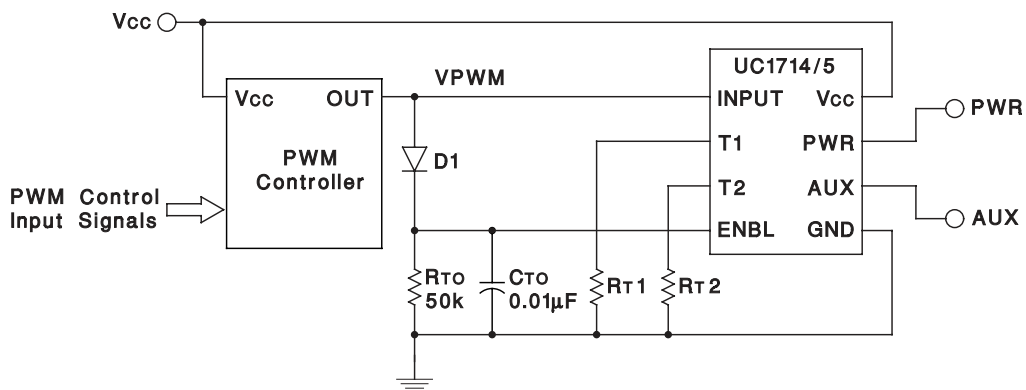


Figure 8. Using The Timer Input For Zero-Voltage Sensing



Wake-up occurs with the first pulse while turnoff is determined by the (RTO CTO) time constant.

Figure 9. Self-Actuated Sleep Mode With The Absence Of An Input PWM Signal

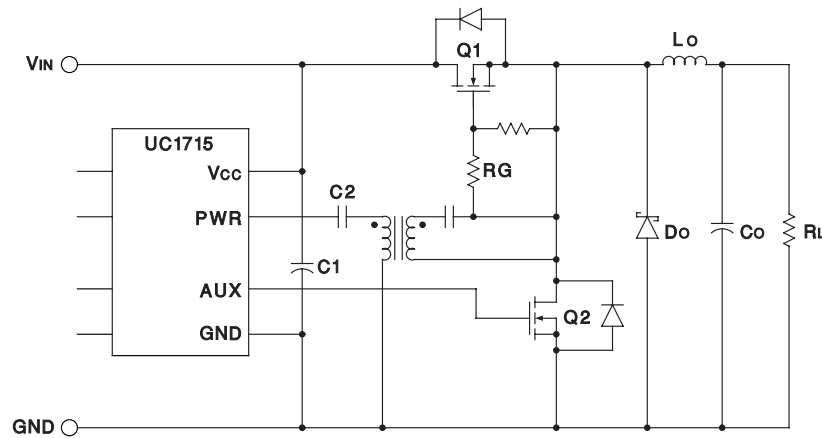
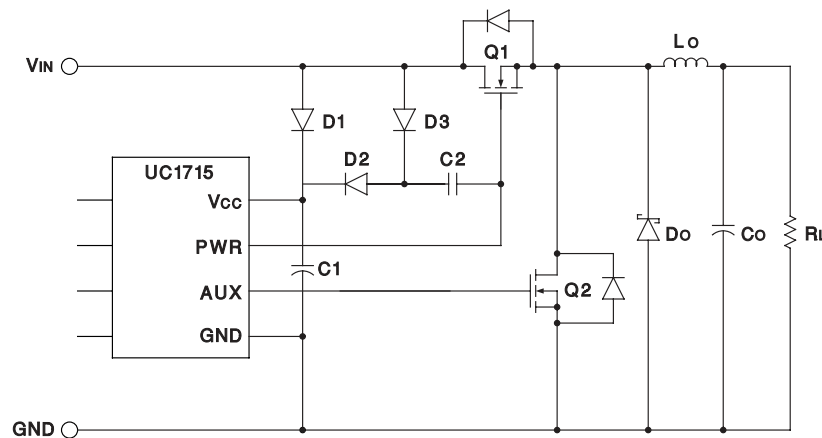
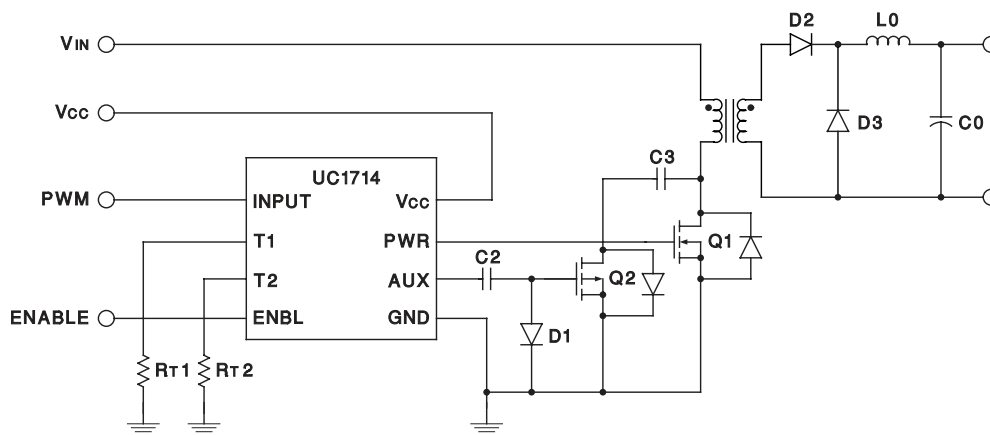


Figure 10. Using The UC1715 As A Complementary Synchronous Rectifier Switch Driver With N-Channel FETs



V_{IN} is limited to 10 V as V_{CC} rises to approximately $2V_{IN}$.

Figure 11. Synchronous Rectifier Application With A Charge Pump To Drive The High-Side N-Channel Buck Switch



With active reset provided by the UC1714 driving an N-channel switch (Q1) and a P-channel auxiliary switch (Q2).

Figure 12. Typical Forward Converter Topology

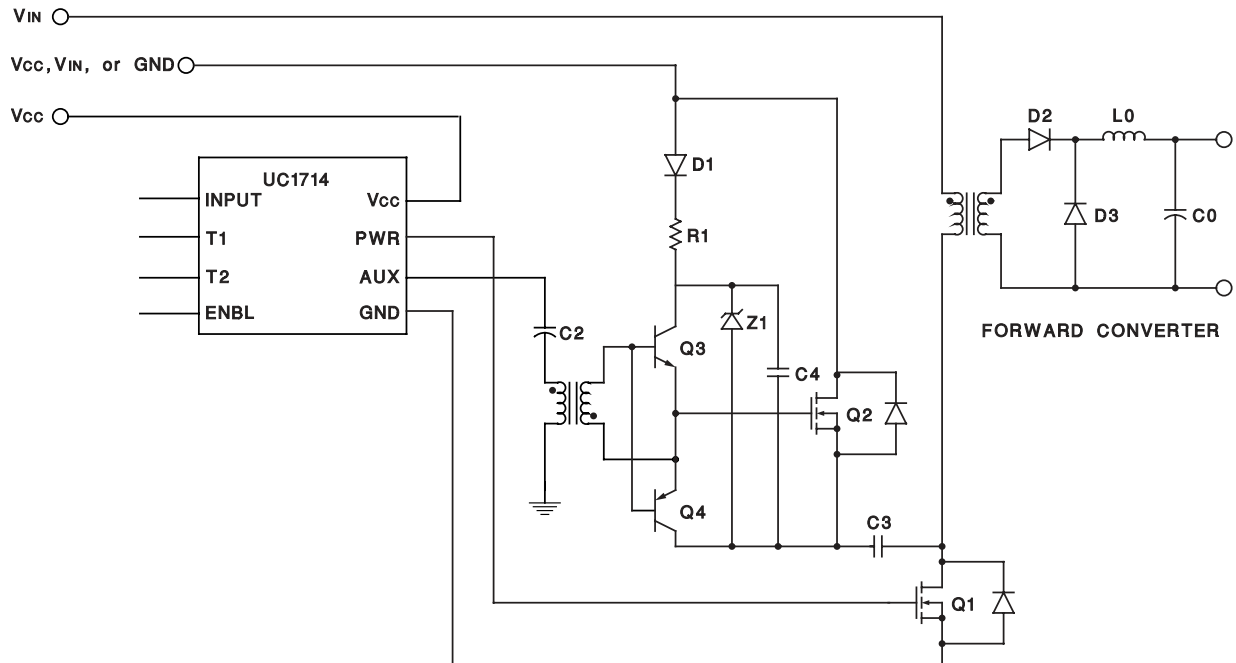


Figure 13. Using An N-Channel Active Reset Switch With A Floating Drive Command

REVISION HISTORY

Changes from Revision A (January 2002) to Revision B	Page
• Added TI's general <i>Absolute Maximum Ratings</i> table note to end of Absolute Maximum table	2
• Changed ENBL $\geq 0.8V$ to ENBL $\leq 0.8V$ in PWR pin description	4
• Changed layout from Unitrode Products datasheet to TI datasheet	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC1714J	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI	-55 to 125		
UC1715J	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI	-55 to 125		
UC1715J883B	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI	-55 to 125		
UC2714D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	-40 to 85	UC2714D	Samples
UC2714DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	-40 to 85	UC2714D	Samples
UC2714DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	-40 to 85	UC2714D	Samples
UC2714J	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI	-40 to 85		
UC2714N	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2714N	
UC2715D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	-40 to 85	UC2715D	Samples
UC2715DP	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2715DP	Samples
UC2715DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2715D	Samples
UC2715DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2715D	Samples
UC2715N	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2715N	
UC2715NG4	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2715N	
UC3714D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	0 to 70	UC3714D	Samples
UC3714DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	0 to 70	UC3714D	Samples
UC3714DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	0 to 70	UC3714D	Samples
UC3714N	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3714N	
UC3715D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3715D	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3715DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3715D	Samples
UC3715DP	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	UC3715DP	
UC3715DPG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
UC3715DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	0 to 70	UC3715D	Samples
UC3715N	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3715N	
UC3715NG4	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3715N	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1714, UC1715, UC2714, UC2714M, UC3714, UC3715 :

- Catalog: [UC3714](#), [UC3715](#), [UC2714](#)

- Military: [UC2714M](#), [UC1714](#), [UC1715](#)

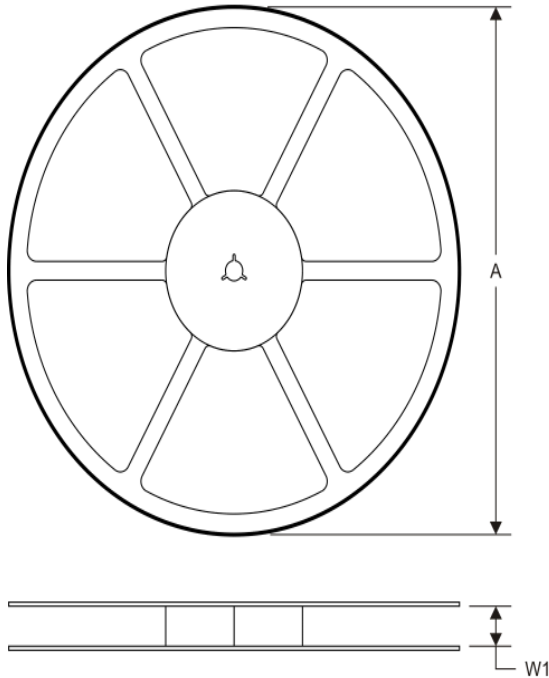
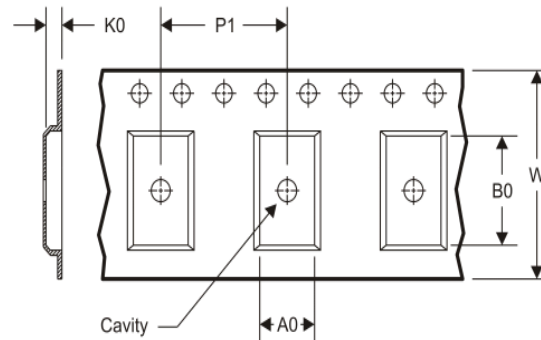
- Space: [UC1715-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2714DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2715DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3714DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3715DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2714DTR	SOIC	D	8	2500	367.0	367.0	35.0
UC2715DTR	SOIC	D	8	2500	367.0	367.0	35.0
UC3714DTR	SOIC	D	8	2500	367.0	367.0	35.0
UC3715DTR	SOIC	D	8	2500	367.0	367.0	35.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com