



ALPHA & OMEGA
SEMICONDUCTOR

AOCA24108E

12V Common-Drain Dual N-Channel MOSFET

General Description

- Trench Power MOSFET Technology
- Low $R_{SS(ON)}$
- With ESD protection to improve battery performance and safety
- Common drain configuration for design simplicity
- RoHS and Halogen-Free Compliant

Product Summary

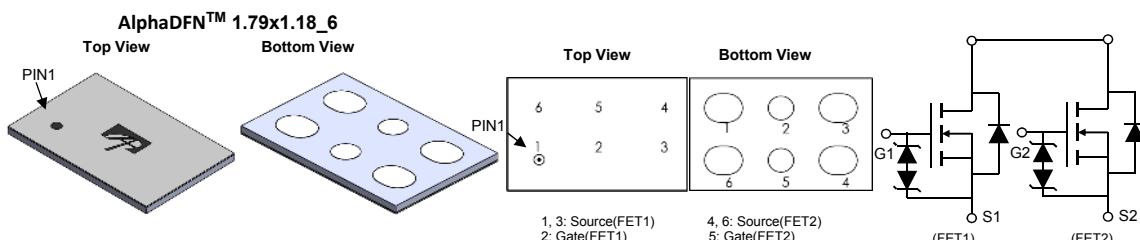
V_{SS}	12V
$R_{SS(ON)}$ (at $V_{GS}=4.5V$)	< 7.5mΩ
$R_{SS(ON)}$ (at $V_{GS}=3.8V$)	< 8mΩ
$R_{SS(ON)}$ (at $V_{GS}=3.1V$)	< 9mΩ
$R_{SS(ON)}$ (at $V_{GS}=2.5V$)	< 11mΩ

Applications

- Battery protection switch
- Mobile device battery charging and discharging

Typical ESD protection

HBM Class 1C



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOCA24108E	AlphaDFN™ 1.79x1.18_6	Tape & Reel	8000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Rating	Units
Source-Source Voltage	V_{SS}	12	V
Gate-Source Voltage	V_{GS}	± 8	V
Source Current(DC) ^{Note1} $T_A=25^\circ\text{C}$	I_S	14	A
Source Current(Pulse) ^{Note2}	I_{SM}	100	
Power Dissipation ^{Note1} $T_A=25^\circ\text{C}$	P_D	2.2	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typical	Units
Maximum Junction-to-Ambient $t \leq 10\text{s}$	$R_{\theta JA}$	45	°C/W
Maximum Junction-to-Ambient Steady-State		55	°C/W

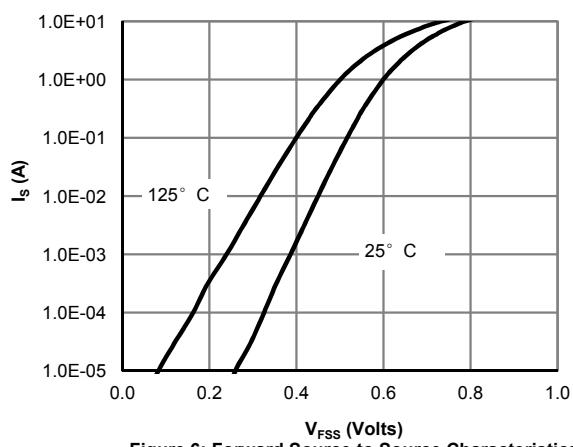
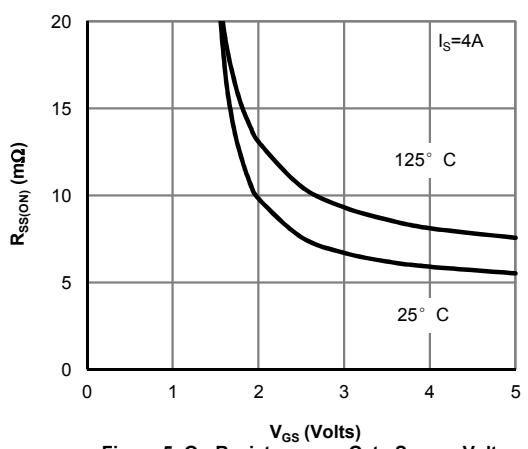
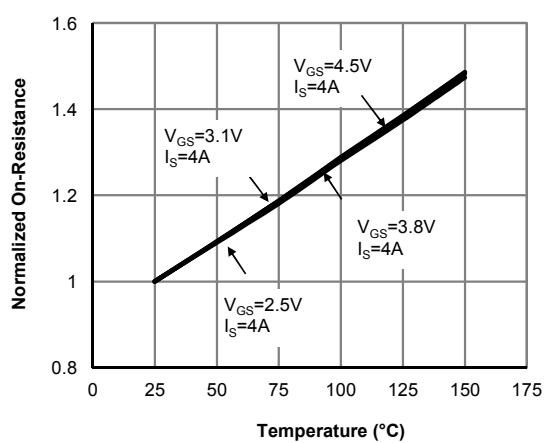
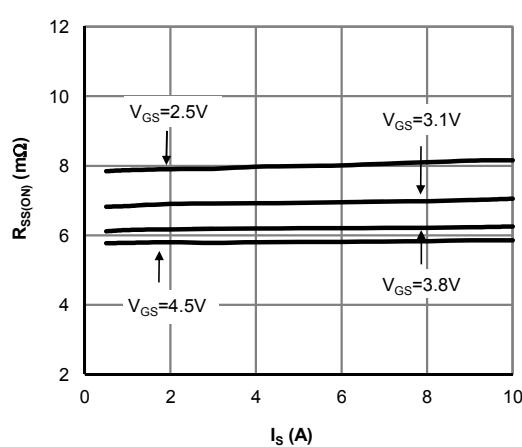
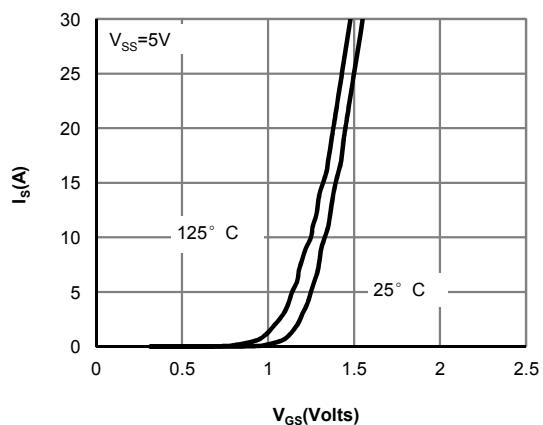
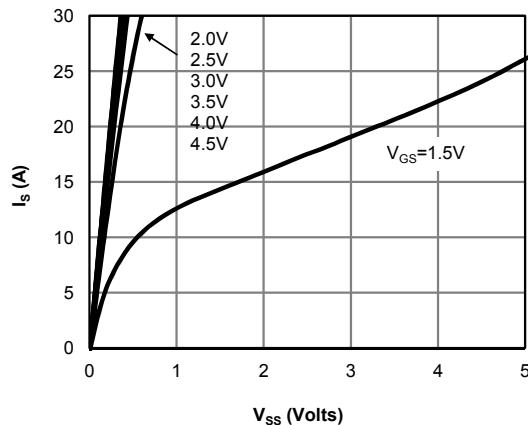
Note 1. I_S rated value is based on bare silicon. Mounted on 70mmx70mm FR-4 board.

Note 2. PW <10 μs pulses, duty cycle 1% max.

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
STATIC PARAMETERS							
BV_{SSS}	Source-Source Breakdown Voltage	$I_S=250\mu\text{A}, V_{GS}=0\text{V}$	Test Circuit 6	12		V	
I_{SSS}	Zero Gate Voltage Source Current	$V_{SS}=12\text{V}, V_{GS}=0\text{V}$	Test Circuit 1		1	μA	
			$T_J=55^\circ\text{C}$		5		
I_{GSS}	Gate leakage current	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$	Test Circuit 2		± 10	μA	
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{SS}=V_{GS}, I_S=250\mu\text{A}$	Test Circuit 3	0.4	0.75	1.1	V
$R_{\text{SS(ON)}}$	Static Source to Source On-Resistance	$V_{GS}=4.5\text{V}, I_S=4\text{A}$	Test Circuit 4	4.1	5.8	7.5	$\text{m}\Omega$
		$T_J=125^\circ\text{C}$		5.5	8.0	10.3	
		$V_{GS}=3.8\text{V}, I_S=4\text{A}$	Test Circuit 4	4.3	6.2	8.0	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=4\text{A}$	Test Circuit 4	4.8	6.9	9.0	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{SS}=5\text{V}, I_S=4\text{A}$	Test Circuit 4	5.6	8.0	11	$\text{m}\Omega$
			Test Circuit 3		35		
V_{FSS}	Forward Source to Source Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$	Test Circuit 5		0.6	1	V
DYNAMIC PARAMETERS							
R_g	Gate resistance	$f=1\text{MHz}$			1.6	$\text{k}\Omega$	
SWITCHING PARAMETERS							
Q_g	Total Gate Charge	$V_{G1S1}=4.5\text{V}, V_{SS}=6\text{V}, I_S=4\text{A}$			15	nC	
$t_{D(on)}$	Turn-On DelayTime				1.0	μs	
t_r	Turn-On Rise Time	$V_{G1S1}=4.5\text{V}, V_{SS}=6\text{V}, R_L=1.5\Omega,$ $R_{\text{GEN}}=3\Omega$	Test Circuit8		2.0	μs	
$t_{D(off)}$	Turn-Off DelayTime				4.9	μs	
t_f	Turn-Off Fall Time				5.2	μs	

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


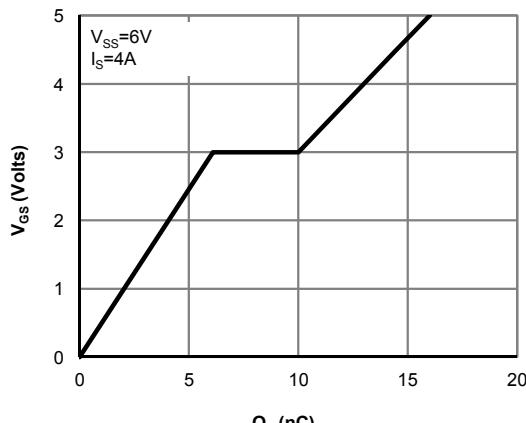
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 7: Gate-Charge Characteristics

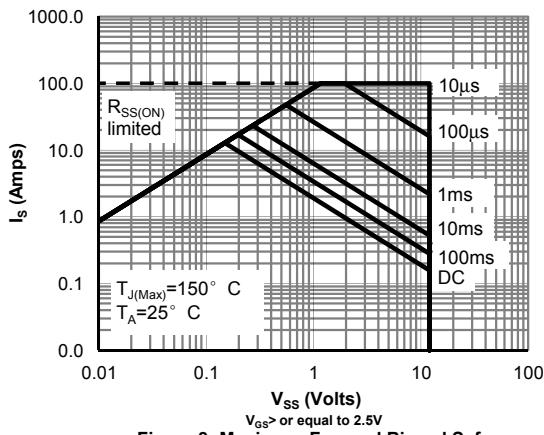


Figure 8: Maximum Forward Biased Safe Operating Area (Note1)

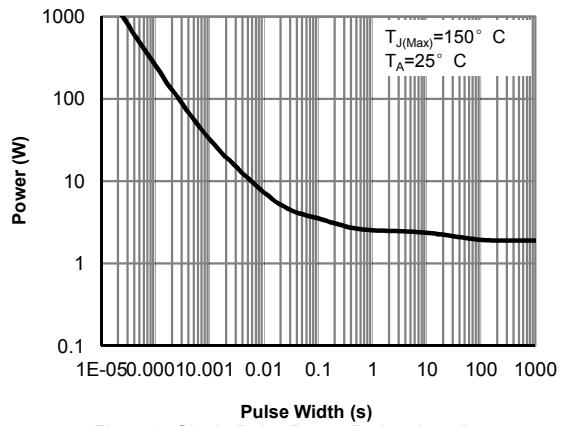


Figure 9: Single Pulse Power Rating Junction-to-Ambient (Note1)

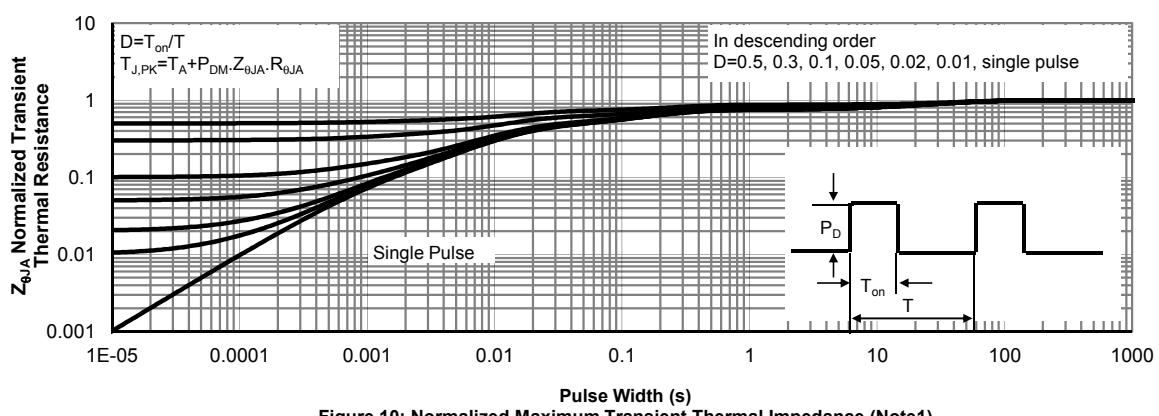
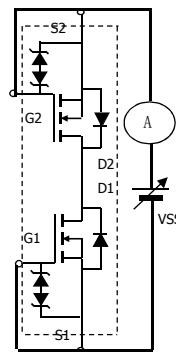
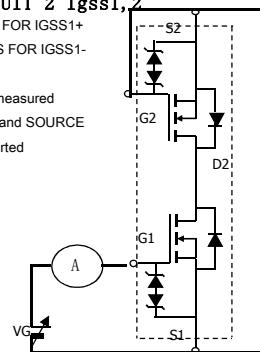


Figure 10: Normalized Maximum Transient Thermal Impedance (Note1)

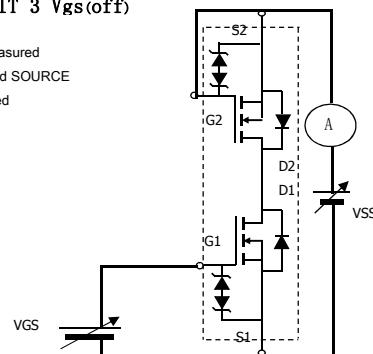
TEST CIRCUIT 1 Isss
 POSITIVE VSS FOR ISSS+
 NEGATIVE VSS FOR ISSS-



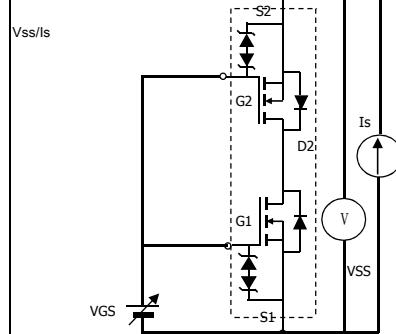
TEST CIRCUIT 2 Igss1,2
 POSITIVE VGS FOR IGSS1+
 NEGATIVE VGS FOR IGSS1-
 When FET1 is measured
 between GATE and SOURCE
 of FET2 are shorted



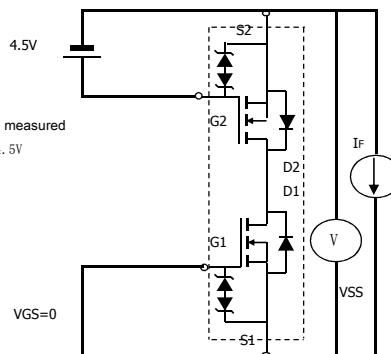
TEST CIRCUIT 3 Vgs(off)
 When FET1 is measured
 between GATE and SOURCE
 of FET2 are shorted



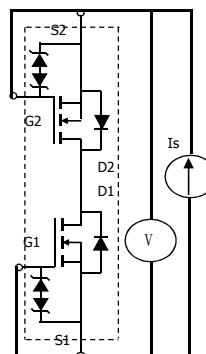
TEST CIRCUIT 4 Rss(on)



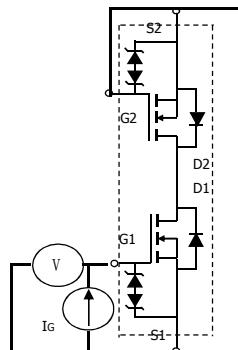
TEST CIRCUIT 5 VF(ss)1,2
 4.5V
 When FET1 measured
 FET2 VGS=4.5V
 VGS=0



TEST CIRCUIT 6 BVdss
 POSITIVE VSS FOR ISSS+
 NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 7 BVgs01,2
 POSITIVE VSS FOR ISSS+
 NEGATIVE VSS FOR ISSS-
 When FET1 is measured
 between GATE and SOURCE
 of FET2 are shorted



TEST CIRCUIT 8
 Switching time

