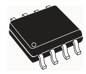
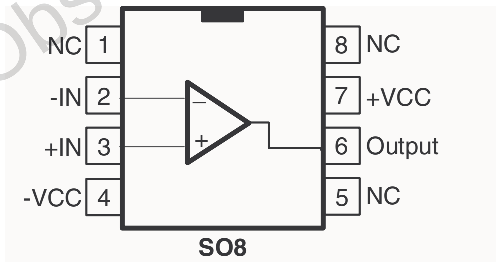
1.1 GHz Low-Noise Operational Amplifier

- **Bandwidth: 1.1GHz (Gain=+2)**
- **Quiescent current: 16.6 mA**
- **Slew rate: 1800V/μs**
- **Input noise: 1.3nV/√Hz**
- **Distortion: SFDR = -78dBc (10MHz, 2Vp-p)**
- **Output stage optimized for driving 100Ω loads**
- **Tested on 5V power supply**

Pin Connections (top view)



D
SO-8
(Plastic Micropackage)



Description

The TSH330 is a current feedback operational amplifier using a very high-speed complementary technology to provide a large bandwidth of 1.1GHz in gain of 2 while drawing only 16.6mA of quiescent current. In addition, the TSH330 offers 0.1dB gain flatness up to 160MHz with a gain of 2. With a slew rate of 1800V/µs and an output stage optimized for driving a standard 100Ω load, this device is highly suitable for applications where speed and low-distortion are the main requirements.

The TSH330 is a single operator available in the SO8 plastic package, saving board space as well as providing excellent thermal and dynamic performances.

Applications

- **Communication & video test equipment**
- **Medical instrumentation**
- **ADC drivers**

Order Codes

Part Number	Temperature Range	Package	Conditioning	Marking
TSH330ID	-40°C to +85°C	SO8	Tube	TSH330I
TSH330IDT		SO8	Tape&Reel	TSH330I

1 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage [1]	6	V
V_{id}	Differential Input Voltage[2]	+/-0.5	V
V_{in}	Input Voltage Range[3]	+/-2.5	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	SO8 Thermal Resistance Junction to Ambient	60	°C/W
R_{thjc}	SO8 Thermal Resistance Junction to Case	28	°C/W
P_{max}	SO8 Maximum Power Dissipation[4] (@Ta=25°C) for Tj=150°C	830	mW
ESD	HBM: Human Body Model [5] (pins 1, 4, 5, 6, 7 and 8)	2	kV
	HBM: Human Body Model (pins 2 and 3)	0.6	kV
	MM: Machine Model [6] (pins 1, 4, 5, 6, 7 and 8)	200	V
	MM: Machine Model (pins 2 and 3)	80	V
	CDM: Charged Device Model (pins 1, 4, 5, 6, 7 and 8)	1.5	kV
	CDM: Charged Device Model (pins 2 and 3)	1	kV
	Latch-up Immunity	200	mA

1) All voltages values are measured with respect to the ground pin.
2) Differential voltage are non-inverting input terminal with respect to the inverting input terminal.
3) The magnitude of input and output voltage must never exceed V_{CC} +0.3V.
4) Short-circuits can cause excessive heating. Destructive dissipation can result from short circuit on amplifiers.
5) Human body model, 100pF discharged through a 1.5kΩ resistor into pMin of device.
6) This is a minimum Value. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage [1]	4.5 to 5.5	V
V_{icm}	Common Mode Input Voltage	-Vcc+1.5V, +Vcc-1.5V	V

1) Tested in full production at 5V (±2.5V) supply voltage.

2 Electrical Characteristics

Table 3. Electrical characteristics for V_{CC}= ±2.5Volts, T_{amb}=+25°C (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	**Input Offset Voltage** Offset Voltage between both inputs	T_{amb}	-3.1	0.18	+3.1	mV
		$T_{min.} < T_{amb} < T_{max.}$		0.8		
ΔV_{io}	**V_{io} drift vs. Temperature**	$T_{min.} < T_{amb} < T_{max.}$		1.6		µV/°C
I_{ib+}	**Non Inverting Input Bias Current** DC current necessary to bias the input +	T_{amb}		26	55	µA
		$T_{min.} < T_{amb} < T_{max.}$		21		
I_{ib-}	**Inverting Input Bias Current** DC current necessary to bias the input -	T_{amb}		7	22	µA
		$T_{min.} < T_{amb} < T_{max.}$		13		
CMR	**Common Mode Rejection Ratio** 20 log $(\Delta V_{ic}/\Delta V_{io})$	$\Delta V_{ic} = \pm 1V$	50	54		dB
		$T_{min.} < T_{amb} < T_{max.}$		54		
SVR	**Supply Voltage Rejection Ratio** 20 log $(\Delta V_{cc}/\Delta V_{out})$	ΔV_{cc}= 3.5V to 5V	63	74		dB
		$T_{min.} < T_{amb} < T_{max.}$		67		
PSR	**Power Supply Rejection Ratio** 20 log $(\Delta V_{cc}/\Delta V_{out})$	ΔV_{cc}=200mVp-p@1kHz		56		dB
		$T_{min.} < T_{amb} < T_{max.}$		52		
ICC	**Supply Current** DC consumption with no input signal	No load		16.6	20.2	mA
		$T_{min.} < T_{amb} < T_{max.}$		16.6		mA
Dynamic performance and output characteristics						
R_{OL}	**Transimpedance** Output Voltage/Input Current Gain in open loop of a CFA. For a VFA, the analog of this feature is the Open Loop Gain (A_{VD})	ΔV_{out}= ±1V, R_L = 100Ω	104	153		kΩ
		$T_{min.} < T_{amb} < T_{max.}$		152		kΩ
Bw	**-3dB Bandwidth** Frequency where the gain is 3dB below the DC gain A_V Note: Gain Bandwidth Product criterion is not applicable for Current-Feedback-Amplifiers	Vout=20mVp-p, RL = 100Ω A_V = +1 A_V = +2 A_V = -4 A_V = -4, $T_{min.} < T_{amb} < T_{max.}$	550	1500 1100 630 600		MHz
	Gain Flatness @ 0.1dB Band of frequency where the gain variation does not exceed 0.1dB	Small Signal V_{out}=20mVp-p A_V = +2, RL = 100Ω		160		
SR	**Slew Rate** Maximum output speed of sweep in large signal	V_{out} = 2Vp-p, A_V = +2, R_L = 100Ω		1800		V/µs
V_{OH}	**High Level Output Voltage**	R_L = 100Ω	1.5	1.64		V
		$T_{min.} < T_{amb} < T_{max.}$		1.54		
V_{OL}	**Low Level Output Voltage**	R_L = 100Ω		-1.55	-1.5	V
		$T_{min.} < T_{amb} < T_{max.}$		-1.5		

Table 3. Electrical characteristics for V_{CC}= ±2.5Volts, T_{amb}=+25°C (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{out}	**Isink** Short-circuit Output current coming in the op-amp. See fig-17 for more details	Output to GND	360	453		mA
		$T_{min.} < T_{amb} < T_{max.}$		427		
	Isource Output current coming out from the op-amp. See fig-18 for more details	Output to GND	-340	-400		
		$T_{min.} < T_{amb} < T_{max.}$		-350		
Noise and distortion						
eN	**Equivalent Input Noise Voltage** see application note on page 13	F = 100kHz		1.3		nV/√Hz
iN	**Equivalent Input Noise Current (+)** see application note on page 13	F = 100kHz		22		pA/√Hz
	Equivalent Input Noise Current (-) see application note on page 13	F = 100kHz		16		pA/√Hz
SFDR	**Spurious Free Dynamic Range** The highest harmonic of the output spectrum when injecting a filtered sine wave	A_V = +2, Vout = 2Vp-p, R_L = 100Ω F = 10MHz F = 20MHz F = 100MHz F = 150MHz		 -78 -73 -48 -37		dBc

Table 4. Closed-loop gain and feedback components

V_{CC} (V)	Gain	R_{fb} (Ω)	-3dB Bw (MHz)	0.1dB Bw (MHz)
±2.5	+10	200	280	50
	-10	200	270	45
	+2	300	1000	160
	-2	270	530	180
	+1	300	1500	38
	-1	260	600	280

Figure 1. Frequency response, positive gain

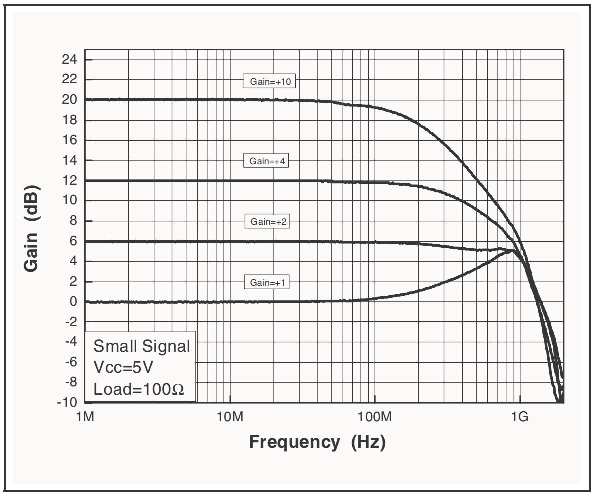


Figure 2. Gain flatness, gain=+4

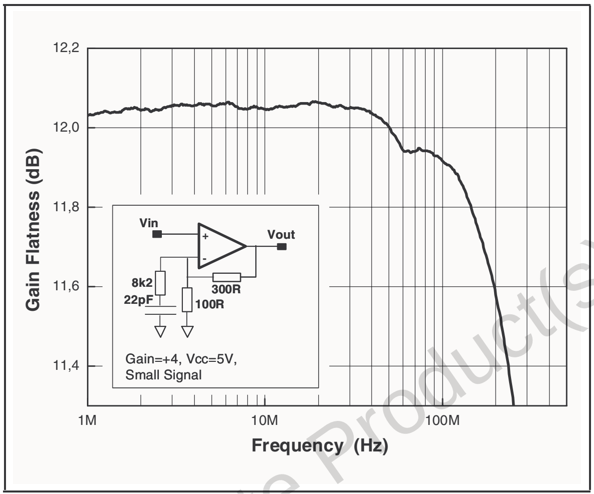


Figure 3. Compensation, gain=+2

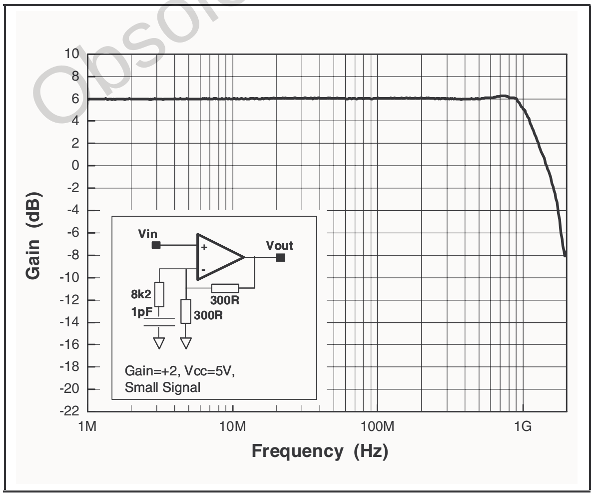


Figure 4. Frequency response, negative gain

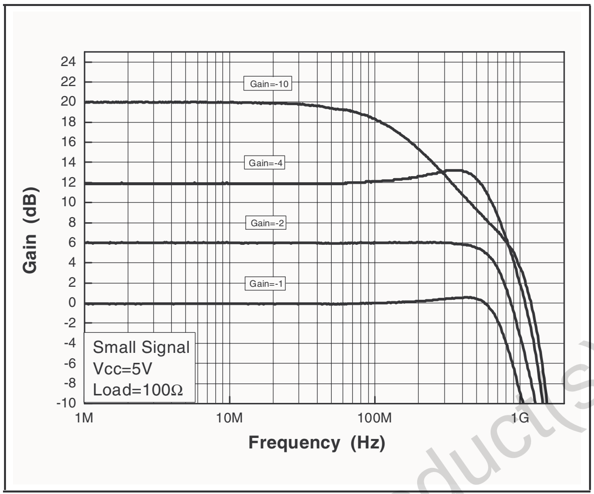


Figure 5. Gain flatness, gain=+2

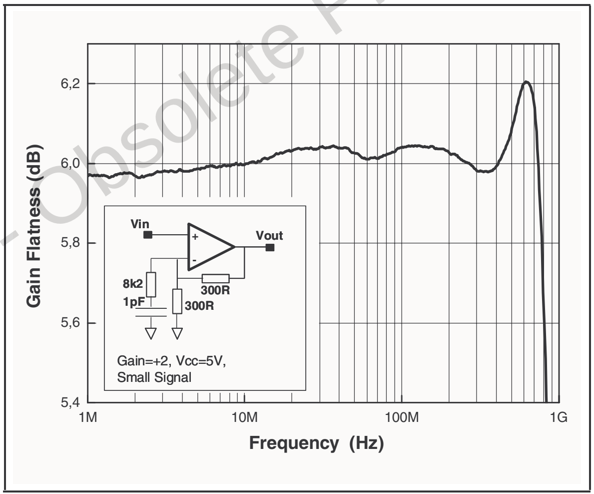


Figure 6. Compensation, gain=+4

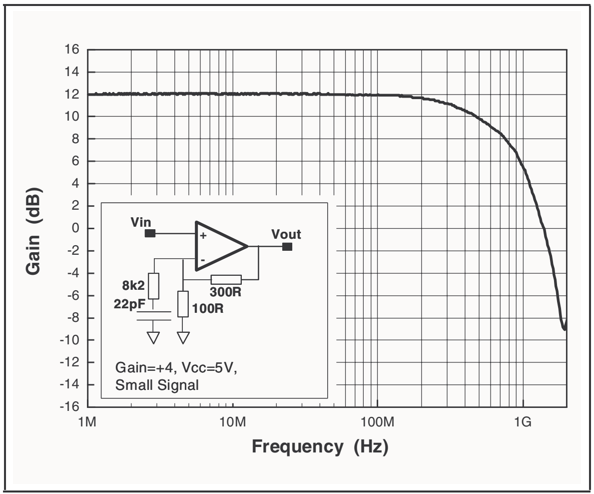


Figure 7. Compensation, gain=+10

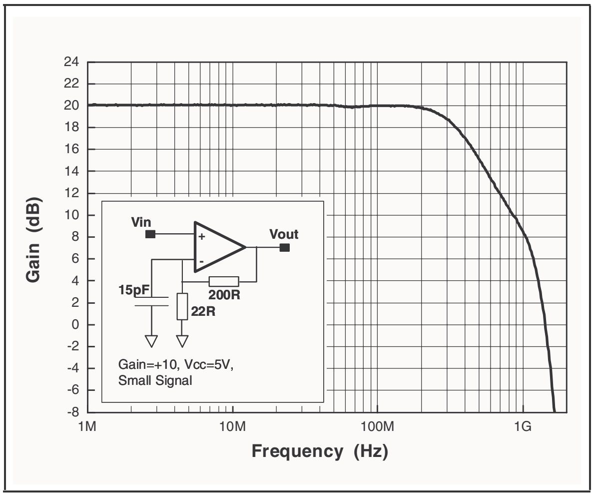


Figure 10. Quiescent current vs. Vcc

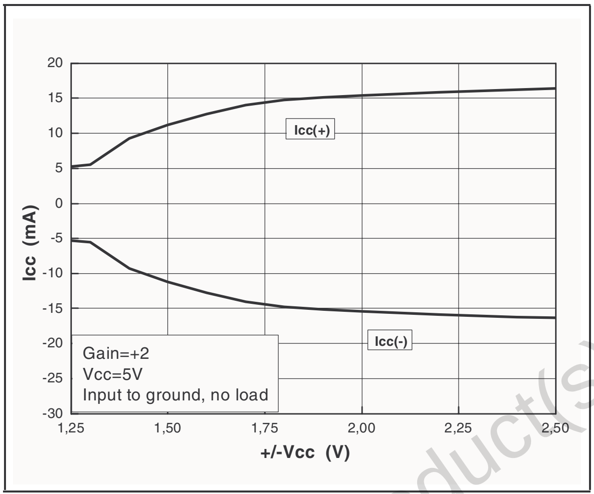


Figure 8. Input current noise vs. frequency

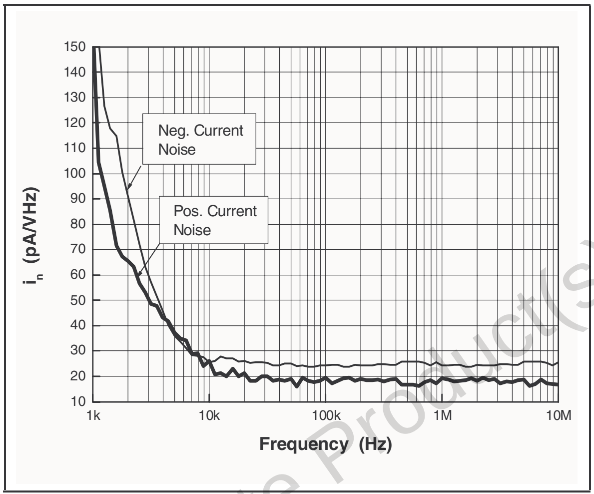


Figure 11. Input voltage noise vs. frequency

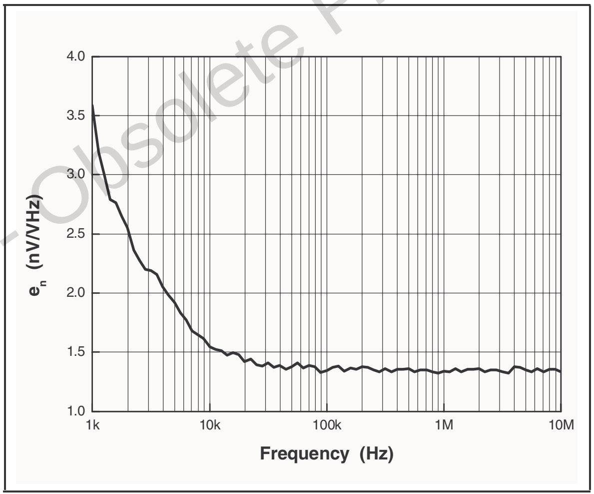


Figure 9. Output amplitude vs. load

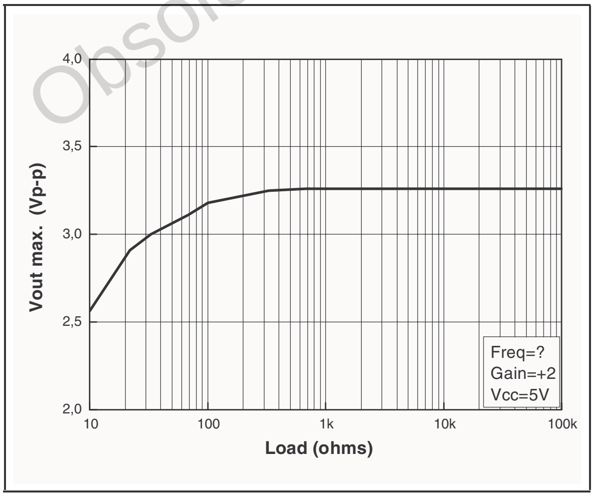


Figure 12. Noise figure

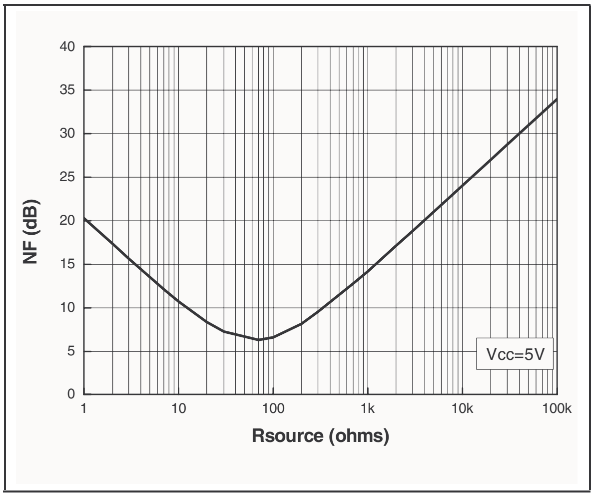


Figure 13. Output amplitude vs. frequency

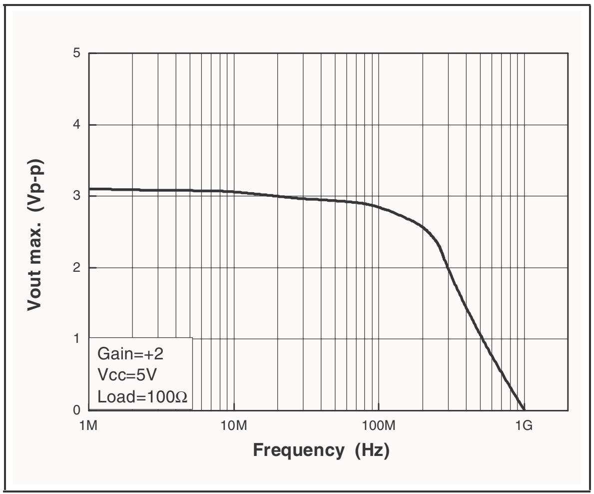


Figure 16. Distortion vs. amplitude

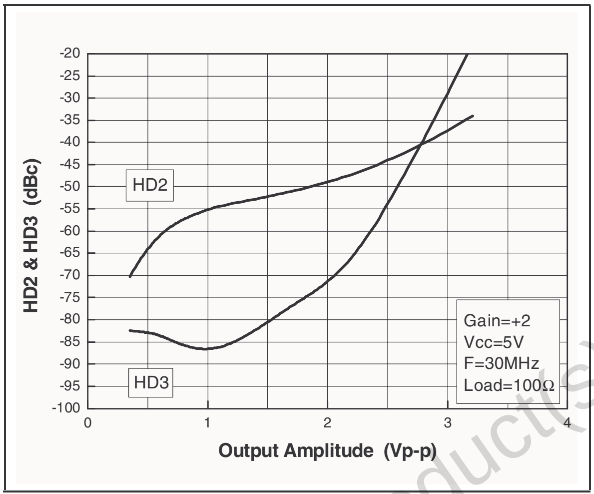


Figure 14. Distortion vs. amplitude

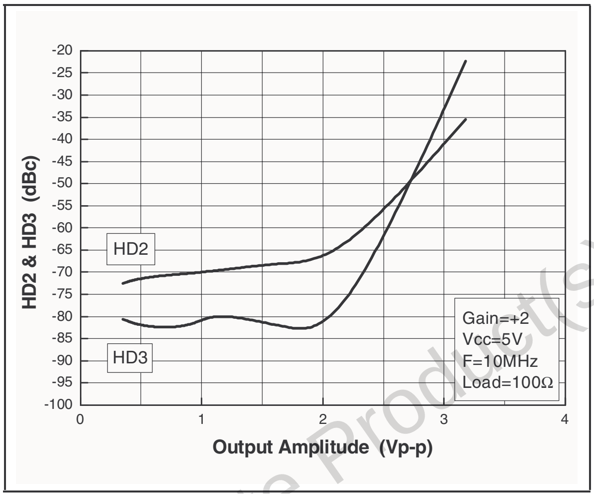


Figure 17. Isink

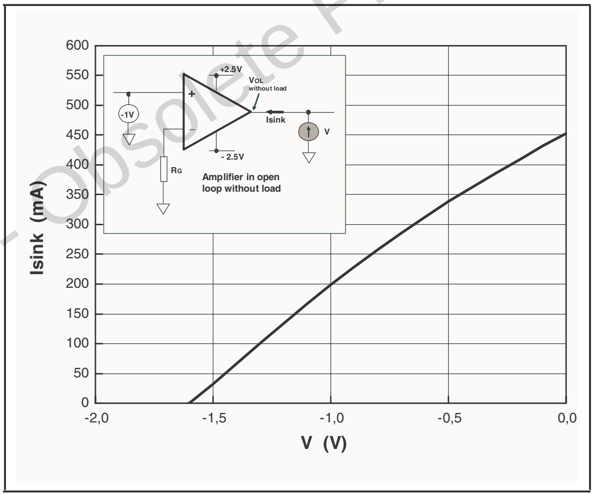


Figure 15. Distortion vs. amplitude

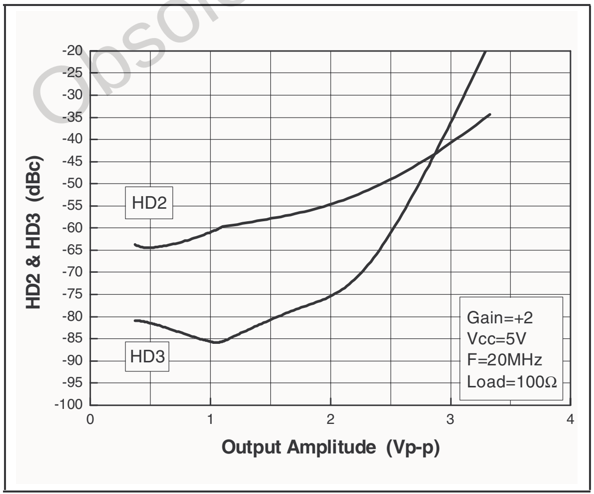


Figure 18. Isource

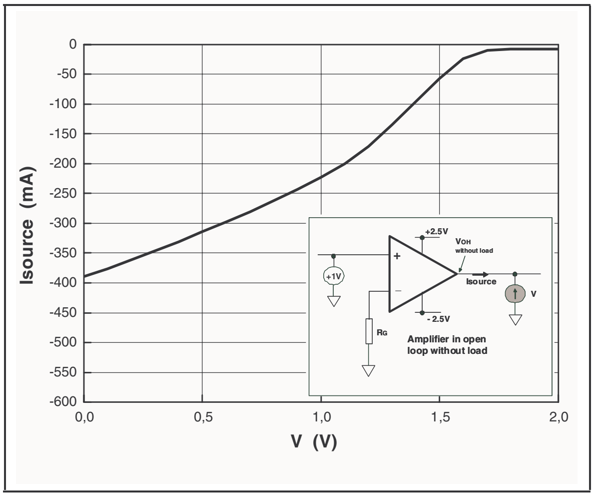


Figure 19. Slew rate

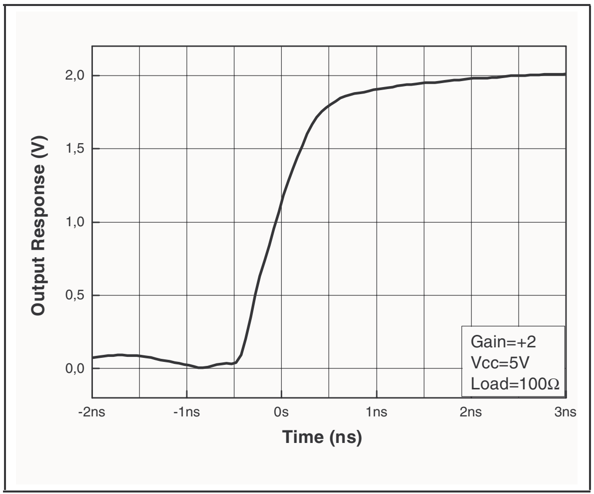


Figure 22. CMR vs. temperature

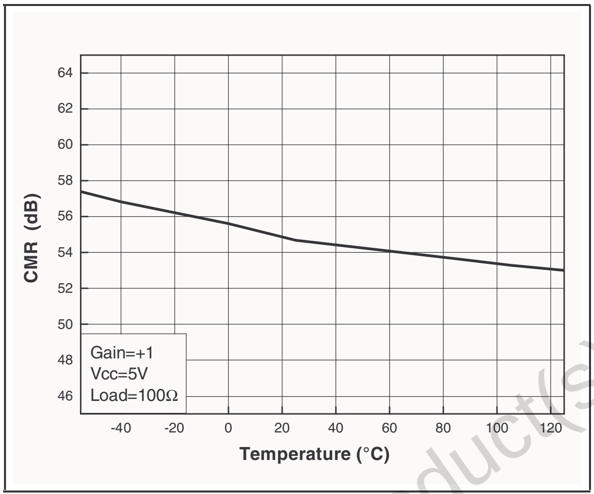


Figure 20. Reverse isolation vs. frequency

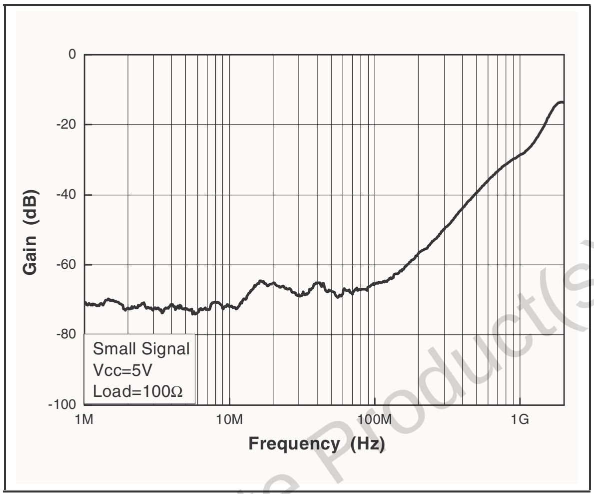


Figure 23. SVR vs. temperature

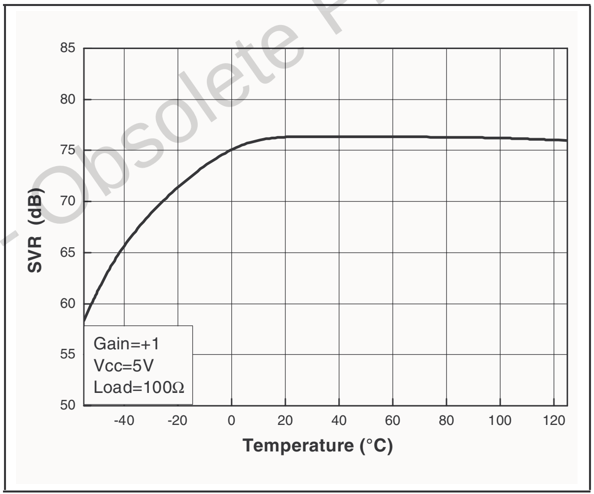


Figure 21. Bandwidth vs. temperature

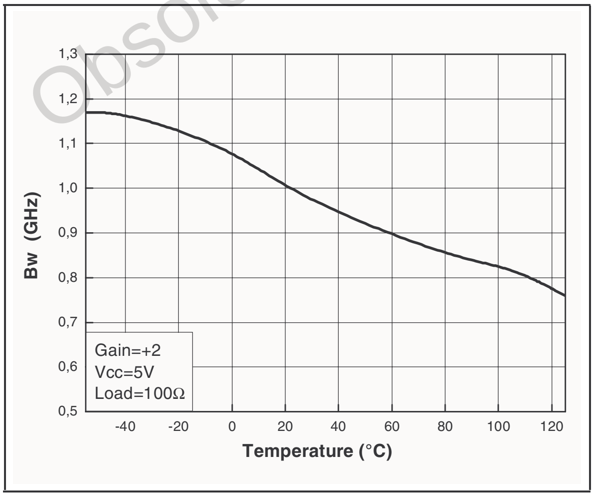


Figure 24. ROL vs. temperature

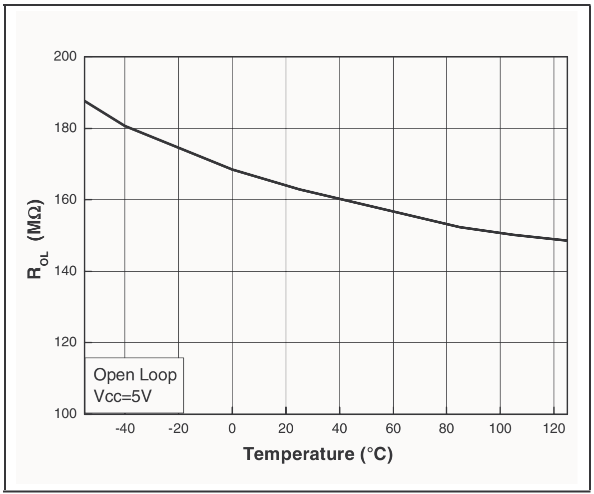


Figure 25. I-bias vs. temperature

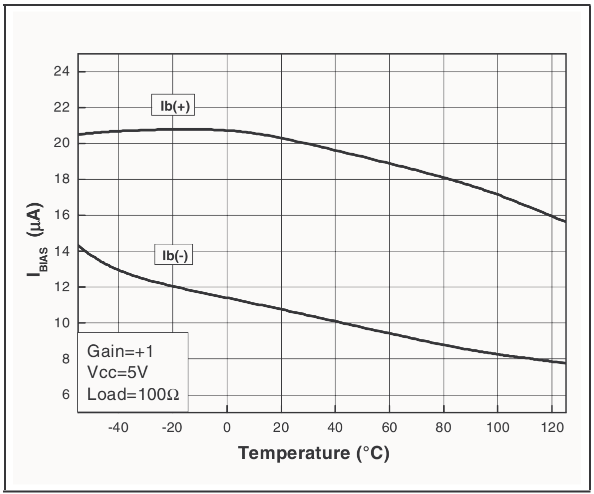


Figure 28. Icc vs. temperature

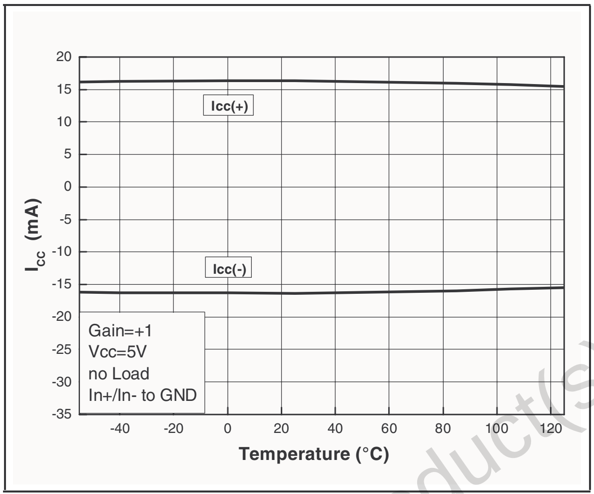


Figure 26. Vio vs. temperature

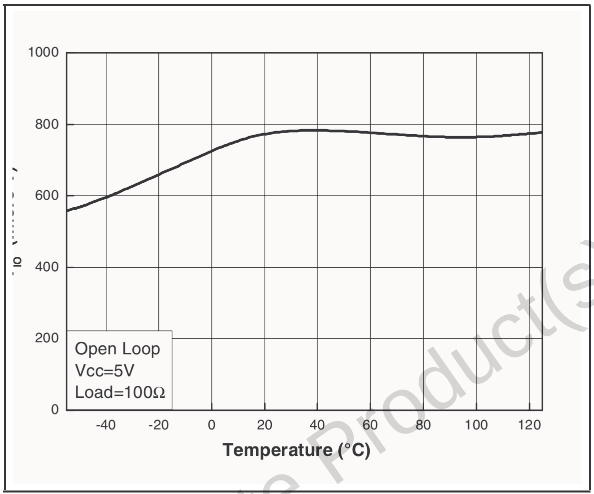


Figure 29. Iout vs. temperature

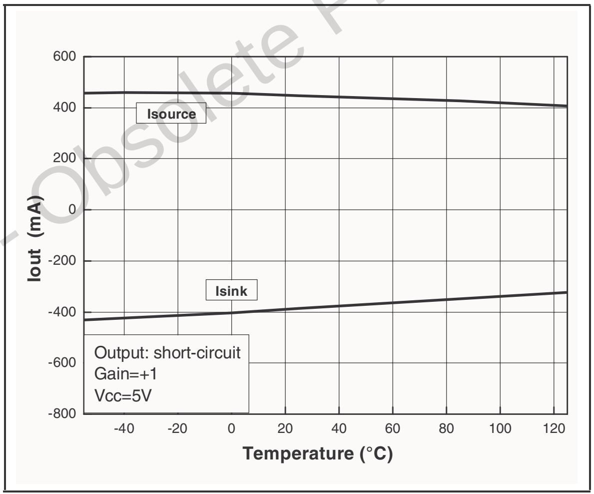
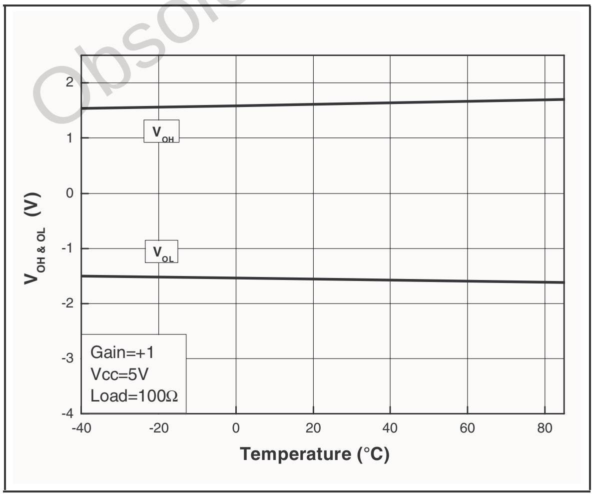


Figure 27. VOH & VOL vs. temperature



3 Evaluation Boards

An evaluation board kit optimized for high-speed operational amplifiers is available (order code: KITHSEVAL/STDL). The kit includes the following evaluation boards, as well as a CD-ROM containing datasheets, articles, application notes and a user manual:

- SOT23_SINGLE_HF BOARD: Board for the evaluation of a single high-speed op-amp in SOT23-5 package.
- SO8_SINGLE_HF: Board for the evaluation of a single high-speed op-amp in SO8 package.
- SO8_DUAL_HF: Board for the evaluation of a dual high-speed op-amp in SO8 package.
- SO8_S_MULTI: Board for the evaluation of a single high-speed op-amp in SO8 package in inverting and non-inverting configuration, dual and single supply.
- SO14_TRIPLE: Board for the evaluation of a triple high-speed op-amp in SO14 package with video application considerations.

Board material:

- 2 layers
- FR4 ($\varepsilon_r=4.6$)
- epoxy 1.6mm
- copper thickness: 35µm

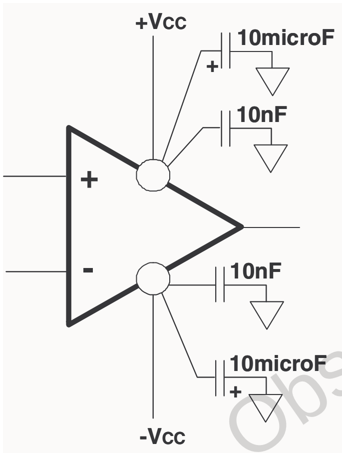
Figure 30. Evaluation kit for high-speed op-amps

4 Power Supply Considerations

Correct power supply bypassing is very important for optimizing performance in high-frequency ranges. Bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor greater than 1µF is necessary to minimize the distortion. For better quality bypassing, a capacitor of 10nF can be added using the same implementation conditions. Bypass capacitors must be incorporated for both the negative and the positive supply.

For example, on the SO8_SINGLE_HF board, these capacitors are C6, C7, C8, C9.

Figure 31. Circuit for power supply bypassing



Single power supply

In the event that a single supply system is used, new biasing is necessary to assume a positive output dynamic range between 0V and $+V_{CC}$ supply rails. Considering the values of V_{OH} and V_{OL}, the amplifier will provide an output dynamic from +0.9V to +4.1V on 100Ω load.

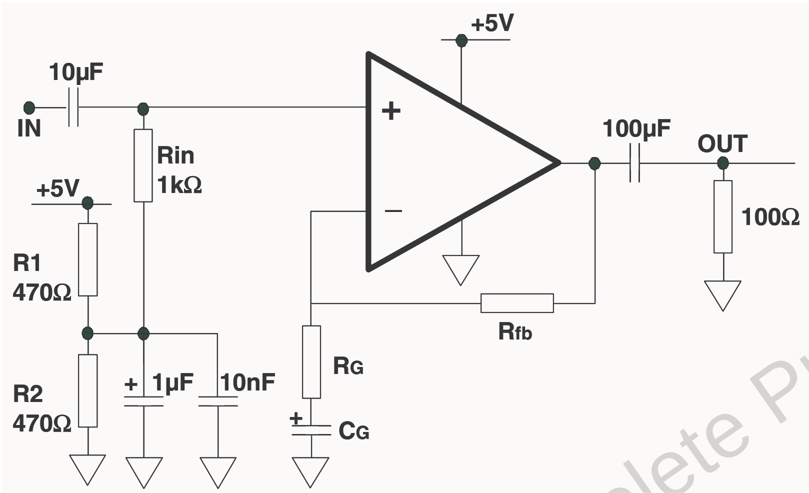
The amplifier must be biased with a mid-supply (nominally $+V_{CC}/2$), in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply, such as a virtual ground using an operational amplifier or a two-resistance divider (which is the cheapest solution). A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current (55µA max.) as the 1% of the current through the resistance divider to keep a stable mid-supply, two resistances of 470Ω can be used.

The input provides a high pass filter with a break frequency below 10Hz which is necessary to remove the original 0 volt DC component of the input signal, and to fix it at $+V_{CC}/2$.

Figure 32 illustrates a 5V single power supply configuration for the SO8_SINGLE evaluation board (see *Evaluation Boards* on page 10).

A capacitor C_G is added in the gain network to ensure a unity gain in low-frequency to keep the right DC component at the output. C_G contributes to a high-pass filter with $R_{fb}//R_G$ and its value is calculated with a consideration of the cut off frequency of this low-pass filter.

Figure 32. Circuit for +5V single supply

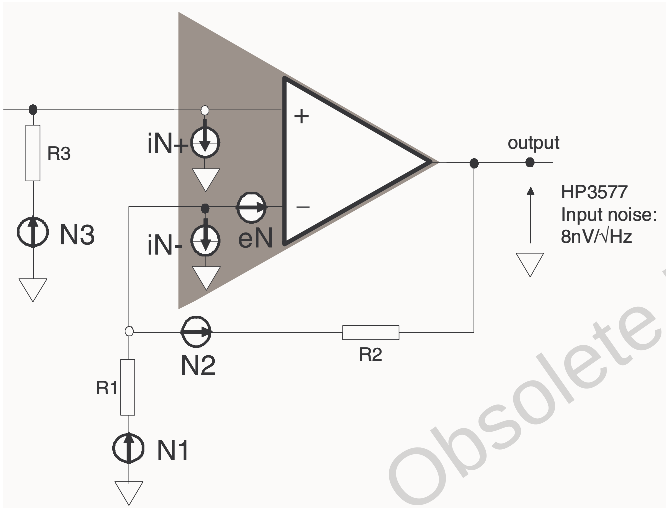


5 Noise Measurements

The noise model is shown in *Figure 33*, where:

- eN: input voltage noise of the amplifier
- iNn: negative input current noise of the amplifier
- iNp: positive input current noise of the amplifier

Figure 33. Noise model



The thermal noise of a resistance R is:

$$\sqrt{4kTR\Delta F}$$

where ΔF is the specified bandwidth.

On a 1Hz bandwidth the thermal noise is reduced to

$$\sqrt{4kTR}$$

where k is the Boltzmann's constant, equal to 1,374.10-23J/°K. T is the temperature (°K).

The output noise eNo is calculated using the Superposition Theorem. However eNo is not the simple sum of all noise sources, but rather the square root of the sum of the square of each noise source, as shown in *Equation 1*:

$$eNo = \sqrt{V1^2 + V2^2 + V3^2 + V4^2 + V5^2 + V6^2} \qquad \text{Equation 1}$$

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + \frac{R2^2}{R1} \times 4kTR1 + 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3 \qquad \text{Equation 2}$$

The input noise of the instrumentation must be extracted from the measured noise value. The real output noise value of the driver is:

$$eNo = \sqrt{(\text{Measured})^2 - (\text{instrumentation})^2} \qquad \textit{Equation 3}$$

The input noise is called the Equivalent Input Noise as it is not directly measured but is evaluated from the measurement of the output divided by the closed loop gain (eNo/g).

After simplification of the fourth and the fifth term of *Equation 2* we obtain:

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + g \times 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3 \qquad \textit{Equation 4}$$

Measurement of the Input Voltage Noise *eN*

If we assume a short-circuit on the non-inverting input (R3=0), from *Equation 4* we can derive:

$$eNo = \sqrt{eN^2 \times g^2 + iNn^2 \times R2^2 + g \times 4kTR2} \qquad \textit{Equation 5}$$

In order to easily extract the value of eN, the resistance R2 will be chosen to be as low as possible. In the other hand, the gain must be large enough:

R3=0, gain: g=100

Measurement of the Negative Input Current Noise *iNn*

To measure the negative input current noise iNn, we set R3=0 and use *Equation 5*. This time the gain must be lower in order to decrease the thermal noise contribution:

R3=0, gain: g=10

Measurement of the Positive Input Current Noise *iNp*

To extract iNp from *Equation 3*, a resistance R3 is connected to the non-inverting input. The value of R3 must be chosen in order to keep its thermal noise contribution as low as possible against the iNp contribution:

R3=100W, gain: g=10

6 Intermodulation Distortion Product

The non-ideal output of the amplifier can be described by the following series:

$$Vout = C_0 + C_1 V_{in} + C_2 V^2{}_{in} + \ldots C_n V^n{}_{in}$$

due to non-linearity in the input-output amplitude transfer, where the input is V_{in}=Asinωt, C_0 is the DC component, $C_1(V_{in})$ is the fundamental and C_n is the amplitude of the harmonics of the output signal V_{out}.

A one-frequency (one-tone) input signal contributes to harmonic distortion. A two-tone input signal contributes to harmonic distortion and to the intermodulation product.

The study of the intermodulation and distortion for a two-tone input signal is the first step in characterizing the driving capability of multi-tone input signals.

In this case:

$$V_{in} = A\sin\omega_1 t + A\sin\omega_2 t$$

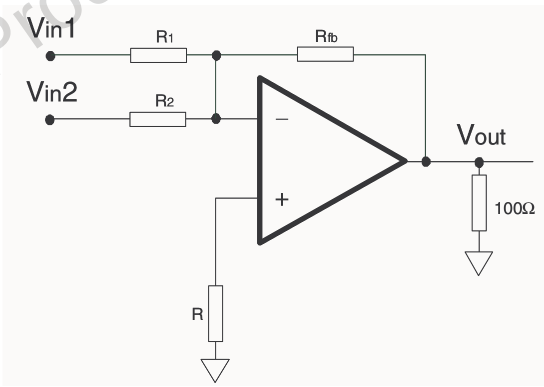
then:

$$V_{out} = C_0 + C_1(A\sin\omega_1 t + A\sin\omega_2 t) + C_2(A\sin\omega_1 t + A\sin\omega_2 t)^2 \ldots + C_n(A\sin\omega_1 t + A\sin\omega_2 t)^n$$

From this expression, we can extract the distortion terms, and the intermodulation terms form a single sine wave: second-order intermodulation terms IM2 by the frequencies (ω_1-ω_2) and (ω_1+ω_2) with an amplitude of C2A^2 and third-order intermodulation terms IM3 by the frequencies (2ω_1-ω_2), (2ω_1+ω_2), (–ω_1+2ω_2) and (ω_1+2ω_2) with an amplitude of (3/4)C3A^3.

The measurement of the intermodulation product of the driver is achieved by using the driver as a mixer by a summing amplifier configuration (see *Figure 34*). In this way, the non-linearity problem of an external mixing device is avoided.

Figure 34. Inverting summing amplifier (using evaluation board SO8_S_MULTI)



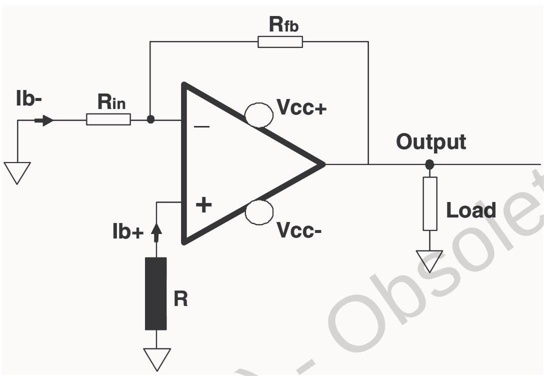
7 The Bias of an Inverting Amplifier

A resistance is necessary to achieve a good input biasing, such as resistance R shown in *Figure 35*.

The magnitude of this resistance is calculated by assuming the negative and positive input bias current. The aim is to compensate for the offset bias current, which could affect the input offset voltage and the output DC component. Assuming Ib-, Ib+, R_{in}, R_{fb} and a zero volt output, the resistance R will be:

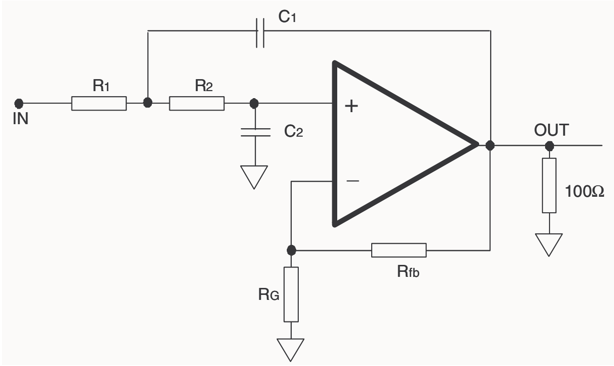
$$R = \frac{R_{in} \times R_{fb}}{R_{in} + R_{fb}}$$

Figure 35. Compensation of the input bias current



8 Active Filtering

Figure 36. Low-pass active filtering, Sallen-Key



From the resistors R_{fb} and R_G we can directly calculate the gain of the filter in a classical non-inverting amplification configuration:

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

We assume the following expression as the response of the system:

$$T_{j\omega} = \frac{Vout_{j\omega}}{Vin_{j\omega}} = \frac{g}{1 + 2\zeta\frac{j\omega}{\omega_c} + \frac{(j\omega)^2}{\omega_c^2}}$$

The cut-off frequency is not gain-dependent and so becomes:

$$\omega_c = \frac{1}{\sqrt{R1R2C1C2}}$$

The damping factor is calculated by the following expression:

$$\zeta = \frac{1}{2}\omega_c(C_1R_1 + C_1R_2 + C_2R_1 - C_1R_1g)$$

The higher the gain, the more sensitive the damping factor is. When the gain is higher than 1, it is preferable to use some very stable resistor and capacitor values. In the case of R1=R2=R:

$$\zeta = \frac{2C_2 - C_1\frac{R_{fb}}{R_g}}{2\sqrt{C_1C_2}}$$

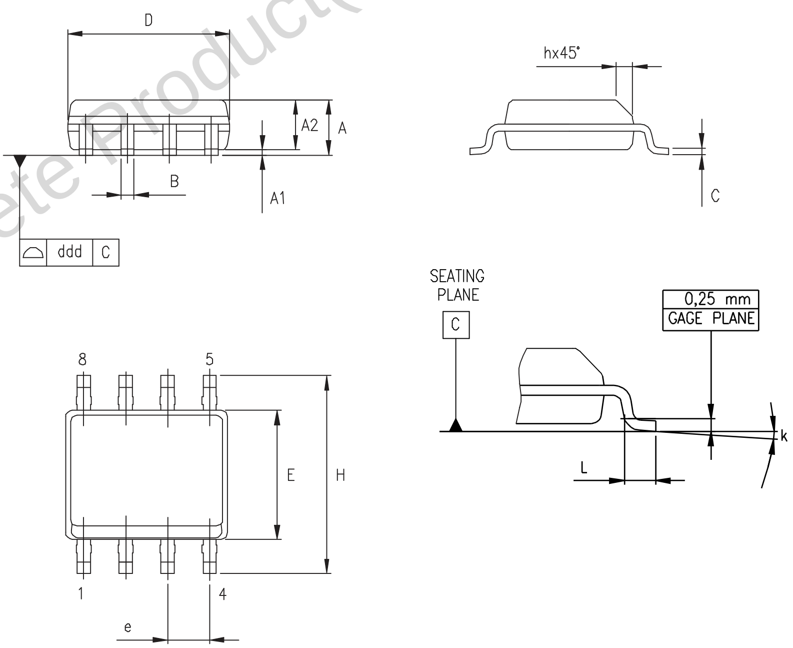
Due to a limited selection of values of capacitors in comparison with resistors, we can fix C1=C2=C, so that:

$$\zeta = \frac{2R_2 - R_1\frac{R_{fb}}{R_g}}{2\sqrt{R_1R_2}}$$

9 Package Mechanical Data

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



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10 Revision History

Date	Revision	Description of Changes
Oct. 2004	1	First release corresponding to Preliminary Data version of datasheet.
Dec. 2004	2	Release of mature product datasheet.
June 2005	3	*Table 1* on page 2 - Rthjc: Thermal Resistance Junction to Ambient replaced by Thermal Resistance Junction to Case