EV-ADuM7704-8FMCZ User Guide
UG-1871

Evaluating the ADuM7704 16-Bit, Isolated, Sigma-Delta Modulator

FEATURES

Fully featured evaluation board for the ADuM7704
On-board power supplies
Standalone capability
SDP-H1 controller board compatible
PC-based software for control and data analysis

EVALUATION KIT CONTENTS

EV-ADuM7704-8FMCZ
ACE software download instructions

EQUIPMENT NEEDED

EVAL-SDP-CH1Z (SDP-H1) controller board
USB cable (provided in SDP-H1 kit)
12 V wall wart signal source (provided in SDP-H1 kit)
PC running Windows Vista SP2 (32-bit or 64-bit), Windows 7 SP1 (32-bit or 64-bit), Windows 8.1 (32-bit or 64-bit), or Windows 10 (32-bit or 64-bit) with a USB 2.0 port

DOCUMENTS NEEDED

ADuM7704 data sheet

SOFTWARE NEEDED

ACE software
ADuM7704 ACE plugin (provided in ACE software)

GENERAL DESCRIPTION

The EV-ADuM7704-8FMCZ is a fully featured evaluation board that allows the user to evaluate all features of the ADuM7704 isolated analog-to-digital converter (ADC). The high speed system demonstration platform (SDP) EVAL-SDP-CH1Z (SDP-H1) controller board controls the EV-ADuM7704-8FMCZ via the J9 connector and through the USB port of a PC using the Analysis, Control, Evaluation (ACE) software. The ACE software is available to download on the ACE software page.

On-board components include an isolated, 5 kV, *iso*Power® dc-to-dc converter (the ADuM6000), a 50 mA, 60 V, high efficiency buck regulator (the ADP2360ACPZ-5.0), and a 5 V, low noise, low dropout (LDO) regulator (the ADP7104ARDZ-5.0).

This user guide explains how to use the EV-ADuM7704-8FMCZ to evaluate the ADuM7704. The ADuM7704 is a high performance, second-order, Σ-Δ modulator that converts an analog input signal into a high speed, single-bit data stream with on-chip digital isolation based on Analog Devices, Inc., *i*Coupler® technology. The device is powered by a 4.5 V to 20 V power supply (V_{DD1}) and accepts a pseudo differential input signal of up to ±50 mV (±64 mV at full scale). The pseudo differential input shunts voltage monitoring in high voltage applications where galvanic isolation is required.

The analog input is continuously sampled by a high performance analog modulator and converts to a ones density digital output stream with a data rate of up to 21 MHz. The original information can be reconstructed with the appropriate digital filter to achieve an 82 dB signal-to-noise ratio (SNR) at 78.1 kSPS with a 20 MHz MCLKIN frequency (f_{MCLKIN}) for the ADuM7704. The serial input and output is powered by a supply of either 5 V or 3.3 V (V_{DD2}).

The serial interface is digitally isolated. The on-chip isolation provides performance characteristics superior to alternatives, such as optocoupler devices, due to high speed CMOS technology combined with monolithic transformer technology. The ADuM7704 comes in both 16-lead and 8-lead, wide-body SOIC packages, and the device has an operating temperature range of −40°C to +125°C (16-lead SOIC_W) and −40°C to +105°C (8-lead SOIC_IC).

For full details on the ADuM7704, see the ADuM7704 data sheet, which must be consulted in conjunction with this user guide when using the evaluation board. Full details on the SDP-H1 are available on the SDP-H1 product page.

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REVISION HISTORY

9/2020—Revision 0: Initial Version

EVALUATION BOARD CONNECTION DIAGRAM

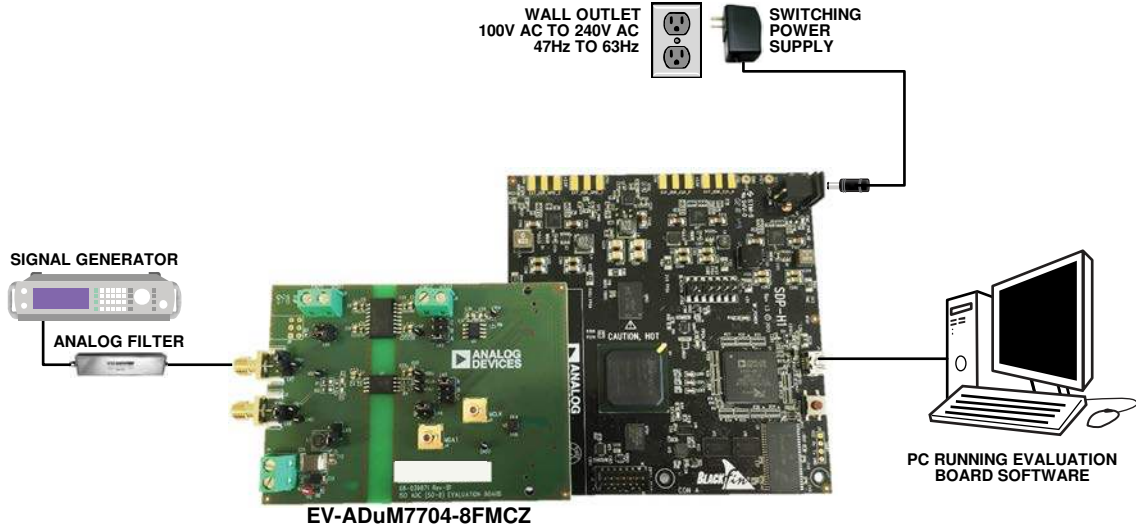*Figure 1.*

EVALUATION BOARD HARDWARE

POWER SUPPLIES

Ensure that all link positions are set according to the required operating mode before applying power and signals to the EV-ADuM7704-8FMCZ. See Table 2 for the list of link options.

The EV-ADuM7704-8FMCZ is powered via the SDP-H1. The SDP-H1 generates 12 V and 3.3 V supply rails. The 12 V supply is connected to the on-board ADP7104ARDZ-5.0, which powers the ADuM6000. The ADuM6000 generates an isolated 5 V supply to power the V_{DD1} rail of the ADuM7704. The 3.3 V supply rail generated by the SDP-H1 powers the V_{DD2} rail of the ADuM7704.

To power V_{DD1} externally, connect an external power supply in the 23 V to 25 V range to the high voltage (HIGH_V) J7 connector, or connect an external power supply in the 4.5 V to 5.5 V range to the J5 connector.

To power V_{DD2} externally, connect an external power supply in the 3 V to 5.5 V range to the J6 connector.

There are two main ground planes on the PCB, GND_1 and GND_2, on the ADuM7704. The GND_1 and GND_2 planes are isolated with a creepage and clearance of 8 mm.

When an external voltage is supplied to the J6 input connector, and the EV-ADuM7704-8FMCZ is connected to the SDP-H1, ensure that the voltage does not exceed 3.3 V. Exceeding 3.3 V causes permanent damage to the SDP-H1.

INPUT SIGNALS

Do not exceed an analog input of ±50 mV (±64 mV at full scale) to the ADuM7704. Connect an input signal of up to 500 mV p-p to the EV-ADuM7704-8FMCZ via the J1 analog input connector.

The EV-ADuM7704-8FMCZ has analog and digital ground planes that are physically isolated from each other. Power to the analog supply rail is supplied through the on-board ADuM6000. V_{DD1} can be supplied from the J5 external connector or from the HIGH_V J7 external connector. The on-board ADP2360ACPZ-5.0 steps the 24 V supply connected to the J7 connector down to 5 V. See Table 1 and Table 2 for more information about supplying V_{DD1} externally.

Table 1. External Power Supplies (Optional)

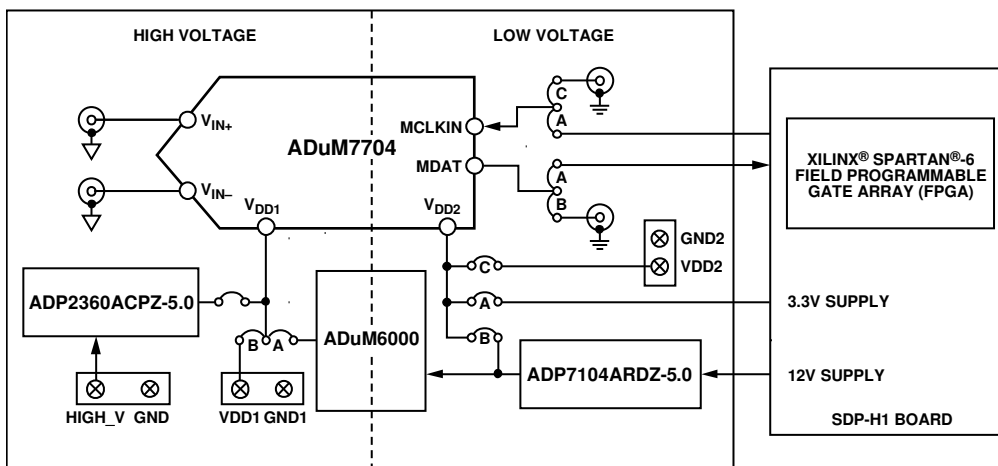| Power Supply	Connector	Voltage Range	Purpose
V_{DD1}	J5	4.5 V to 5.5 V	Analog supply rail
V_{DD2}	J6	3 V to 5.5 V	Digital supply rail without the SDP-H1 connected
		3.15 V to 3.45 V	Digital supply rail with the SDP-H1 connected
HIGH_V	J7	23 V to 25 V	Analog supply rail (high voltage alternative to J5)

Figure 2. EV-ADuM7704-8FMCZ Block Diagram

LINK CONFIGURATION OPTIONS

Multiple link options must be set properly to select the appropriate operating setup before using the EV-ADuM7704-8FMCZ. The functions of these link options are outlined in Table 2.

Setup Conditions

Ensure that all link positions are set as required by the operating mode before applying power and signals to the EV-ADuM7704-8FMCZ. The EV-ADuM7704-8FMCZ operates in standalone mode or in SDP-H1 controlled mode when used with the SDP-H1.

Table 2 shows the default positions the links are set to when the EV-ADuM7704-8FMCZ is packaged. When the EV-ADuM7704-8FMCZ is shipped, the evaluation board is set up to operate in SDP-H1 controlled mode with power supplied from the SDP-H1. The on-board ADuM6000 powers V_{DD1}.

Table 2. Link Options

Category	Link	Default Position	Function
Power Supplies	LK1	A	LK1 selects the ADuM7704 V_{DD1} supply source. Remove LK5 if using Position A or Position B.
			In Position A, the on-board ADuM6000 supplies V_{DD1}.
			In Position B, the J5 connector supplies V_{DD1} externally.
	LK5	Removed	Insert LK5 to power V_{DD1} with the on-board ADP2360ACPZ-5.0 via the J7 connector. Remove LK5 if V_{DD1} is powered via LK1.
	LK2	A	LK2 selects the ADuM7704 V_{DD2} supply source.
			In Position A, the SDP-H1 supplies V_{DD2}.
			In Position B, the on-board ADP7104ARDZ-5.0 supplies V_{DD2}.
			In Position C, the J6 connector supplies V_{DD2} externally.
Analog Input	LK7	Removed	Insert LK7 to short V_{IN+} to ground. Remove LK7 if a signal is applied to V_{IN+}.
	LK8	Inserted	Insert LK8 to short V_{IN-} to ground. Remove LK8 if a signal is applied to V_{IN-}.
Serial Interface	LK3	A	LK3 selects the MCLK source for the serial interface.
			In Position A, the SDP-H1 sources MCLK.
			In Position B, do not use.
			In Position C, the J3 Subminiature Version B (SMB) jack sources MCLK (standalone mode).
	LK4	A	LK4 routes the MDAT pin signal output for the serial interface.
			In Position A, MDAT is sent to the SDP-H1.
			In Position B, MDAT is sent to the J4 SMB jack (standalone mode).

SOCKETS AND CONNECTORS

Table 3 describes the connectors and sockets on the EV-ADuM7704-8FMCZ.

Table 3. On-Board Connectors

Connector	Function
J1	Analog input V_{IN+}
J2	Analog input V_{IN-}
J3	MCLK input (standalone mode)
J4	MDAT output (standalone mode)
J5	V_{DD1} external source
J6	V_{DD2} external source
J7	V_{DD1} external source (high voltage)

The default interface to the EV-ADuM7704-8FMCZ is achieved via the 160-way connector. The connector attaches the EV-ADuM7704-8FMCZ to the SDP-H1. When the EV-ADuM7704-8FMCZ is used in standalone mode, communication is achieved via the J3 SMB jack and the J4 SMB jack. See Table 2 for more information on configuring the EV-ADuM7704-8FMCZ for standalone mode.

TEST POINTS

There are several test points on the EV-ADuM7704-8FMCZ. These test points provide access to the EV-ADuM7704-8FMCZ signals for probing, evaluation, and debugging.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURES

Download the ACE software from the ACE software page. Install the ACE software before using the EV-ADuM7704-8FMCZ.

The ACE installation process in the Installing the ACE Software section includes the ACE software installation and the SDP-H1 driver installation.

Install the ACE software and SDP-H1 drivers before connecting the EV-ADuM7704-8FMCZ and the SDP-H1 to the USB port of the PC to ensure that the evaluation system is properly recognized when it is connected to the PC.

Installing the ACE Software

To install the ACE software, take the following steps:

1. Download the ACE software to a Windows®-based PC.
2. Double click the **ACEInstall.exe** file to begin the installation. By default, the ACE software is saved to the following location: **C:\Program Files (x86)\Analog Devices\ACE.**
3. A dialog box opens asking for permission to allow the program to make changes to the PC. Click **Yes** to start the installation process.
4. In the **ACE Setup** window, click **Next >** to continue the installation (see Figure 3).
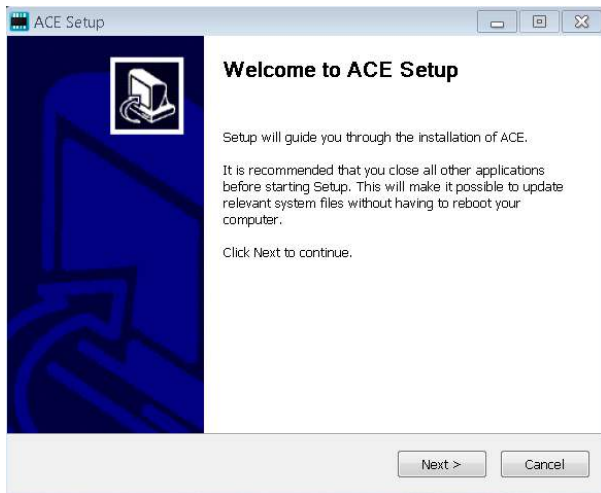
Figure 3. ACE Software Installation Confirmation

5. Read the software license agreement and click **I Agree** (see Figure 4).

Figure 4. License Agreement

6. Click **Browse…** to choose the installation location and then click **Next >** (see Figure 5).
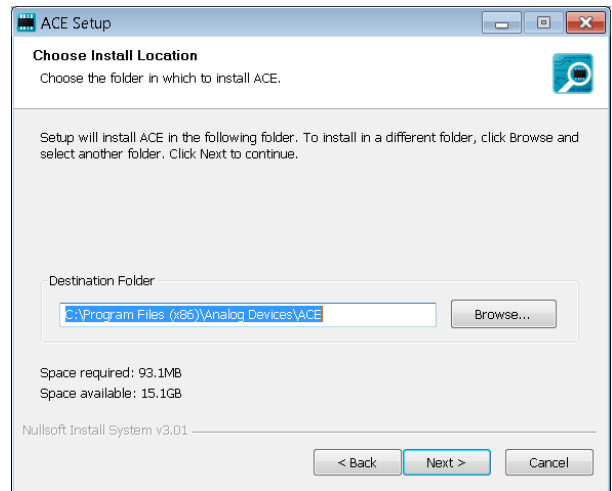
Figure 5. Choose Installation Location

7. The ACE software components to install are preselected (see Figure 6). Click **Install**.
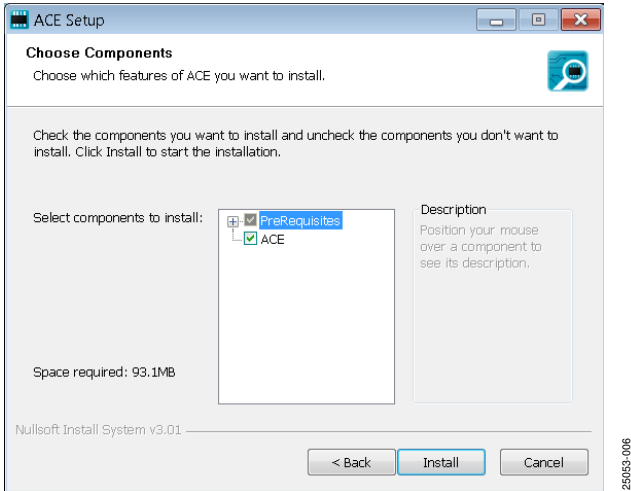
*Figure 6. **Choose Components** Window*

8. The **Windows Security** window opens (see Figure 7). Click **Install**. Figure 8 shows the installation in progress. No action is required.

*Figure 7. **Windows Security** Window*
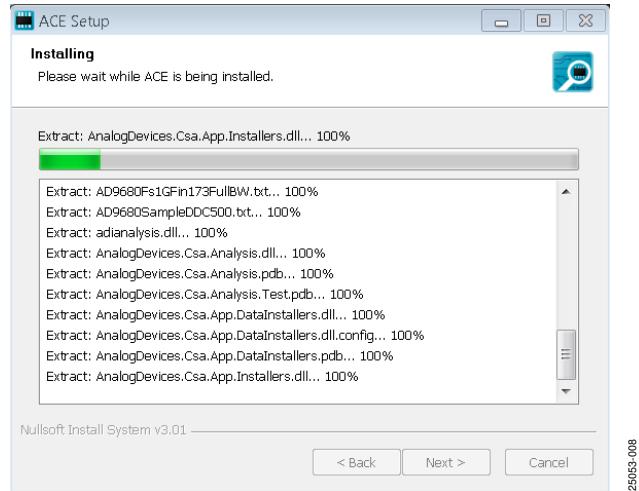
Figure 8. Installation in Progress

9. When the installation is complete, click **Next >** (see Figure 9), and then click **Finish** to complete the installation process.
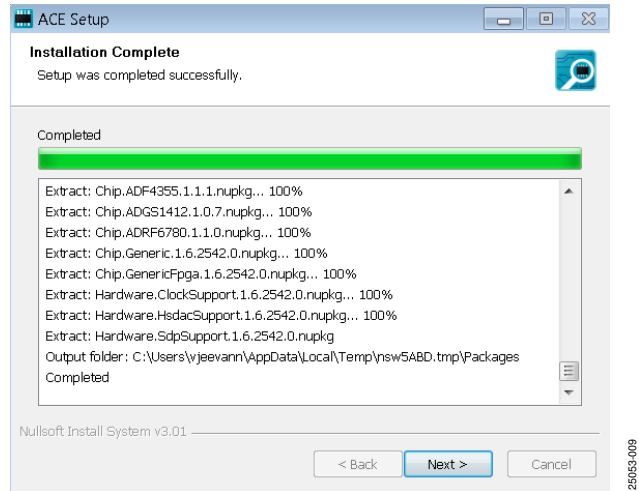
Figure 9. Installation Complete

EVALUATION BOARD SETUP PROCEDURES

The EV-ADuM7704-8FMCZ connects to the SDP-H1. The SDP-H1 is the communication link between the PC and the EV-ADuM7704-8FMCZ. A diagram of the connections between the EV-ADuM7704-8FMCZ and the SDP-H1 is shown in Figure 11.

Connecting the EV-ADuM7704-8FMCZ and the SDP-H1 to the PC

After the ACE software is installed, take the following steps to set up the EV-ADuM7704-8FMCZ and the SDP-H1:

1. Ensure that all configuration links are in the proper positions, as described in Table 2.
2. Connect the EV-ADuM7704-8FMCZ to the 160-way connector on the SDP-H1.
3. To power up the SDP-H1, insert the 12 V, dc barrel jack (included in the SDP-H1 kit) into the barrel connector labeled +12V_VIN on the SDP-H1. Note that the EV-ADuM7704-8FMCZ does not require an external power supply adapter.
4. Connect the SDP-H1 to the PC via the USB cable included in the SDP-H1 kit.

Verifying the Board Connection

After connecting the SDP-H1 to the PC, allow the **Found New Hardware Wizard** to run. If prompted by the operating system, choose to automatically search for the drivers for the SDP-H1.

1. Navigate to the **Device Manager** window on the PC (see Figure 10).

2. A dialog box opens asking for permission to allow the program to make changes to the computer. Click **Yes**.
3. The **Computer Management** window opens. In the list labeled **System Tools**, click **Device Manager**. If the SDP-H1 driver is installed, and both the SDP-H1 board and the EV-ADuM7704-8FMCZ are properly connected to the PC, **Analog Devices SDP-H1** is shown in the **ADI Development Tools** list in the **Device Manager** window, as shown in Figure 10.
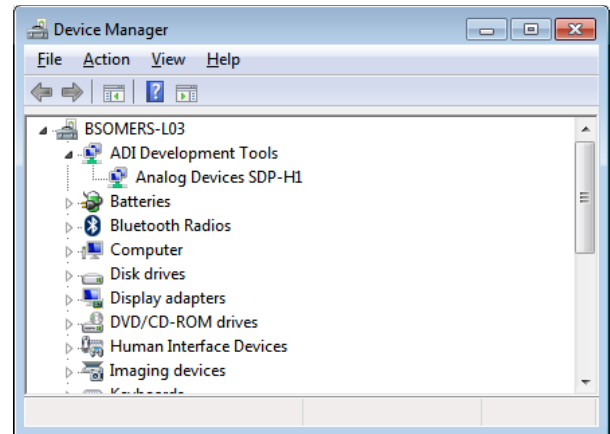
*Figure 10. **Device Manager** Window*

Disconnecting the EV-ADuM7704-8FMCZ

Disconnect power from the SDP-H1, or press the reset tact switch located alongside the mini USB port on the SDP-H1 before disconnecting the EV-ADuM7704-8FMCZ from the SDP-H1.
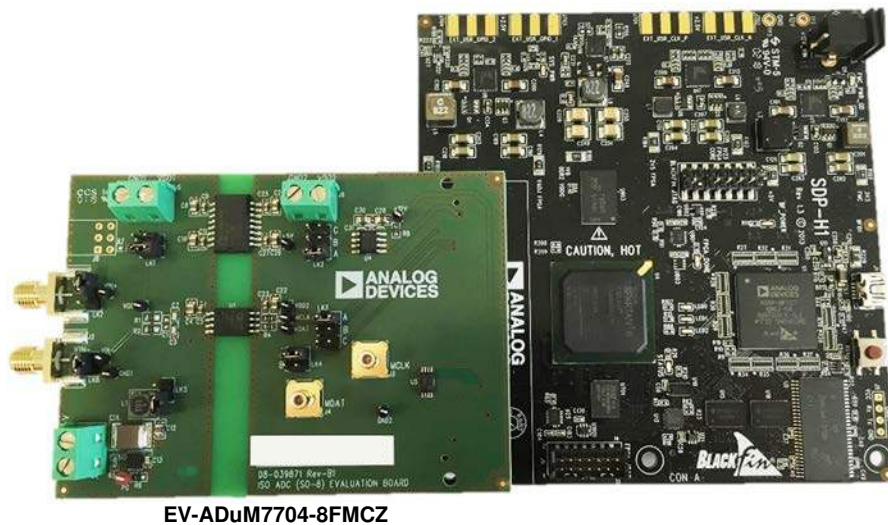
EV-ADuM7704-8FMCZ

Figure 11. EV-ADuM7704-8FMCZ (Left) and SDP-H1 (Right) Connection

ACE SOFTWARE OPERATION

LAUNCHING THE SOFTWARE

When the EV-ADuM7704-8FMCZ and the SDP-H1 are properly connected to the PC, launch the ACE software by taking the following steps:

1. In the **Start** menu of the PC, click **All Programs** > **Analog Devices** > **ACE** > **ACE.exe** to open the ACE software main window shown in Figure 12.
2. Connect an input signal via the V_{IN+} J1 connector. Note that if the EV-ADuM7704-8FMCZ is not connected to the USB port via the SDP-H1 when the ACE software launches, the **ADuM7704 Eval Board** icon does not appear in the **Attached Hardware** section in ACE (see Figure 12). To make the **ADuM7704 Eval Board** icon appear, connect the EV-ADuM7704-8FMCZ and the SDP-H1 to the USB port of the PC, wait a few seconds, and then follow the instructions in the dialog box that opens.
3. Double click the **ADuM7704 Eval Board** icon (see Figure 12) to open the chip view window shown in Figure 13.
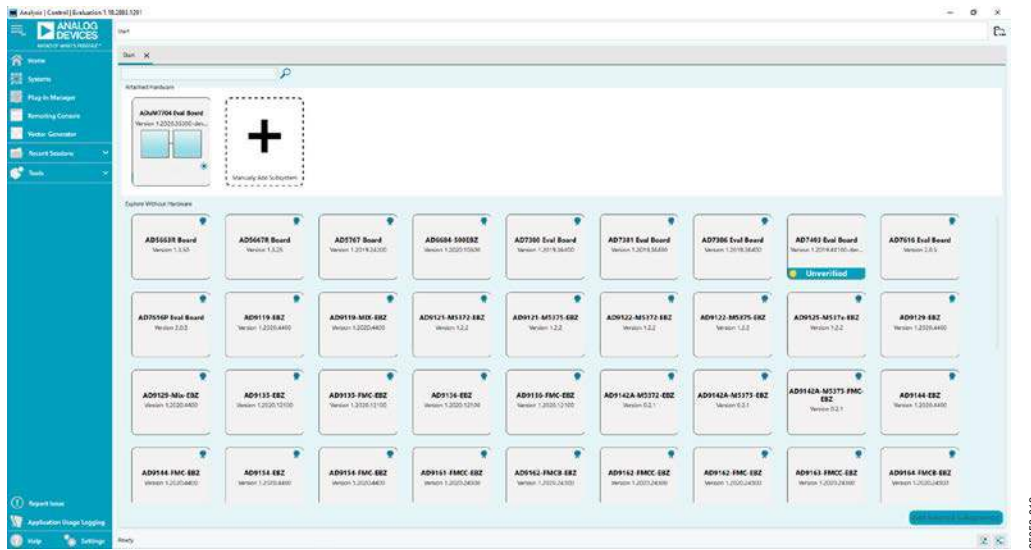
Figure 12. ACE Software Main Window

CHIP VIEW WINDOW FEATURES

Click **Proceed to Analysis** in the chip view window of the ACE software (see Figure 13) to open the analysis view window shown in Figure 14. The analysis view window contains the **Waveform** tab, **Histogram** tab, and **FFT** tab on the left side of the window.
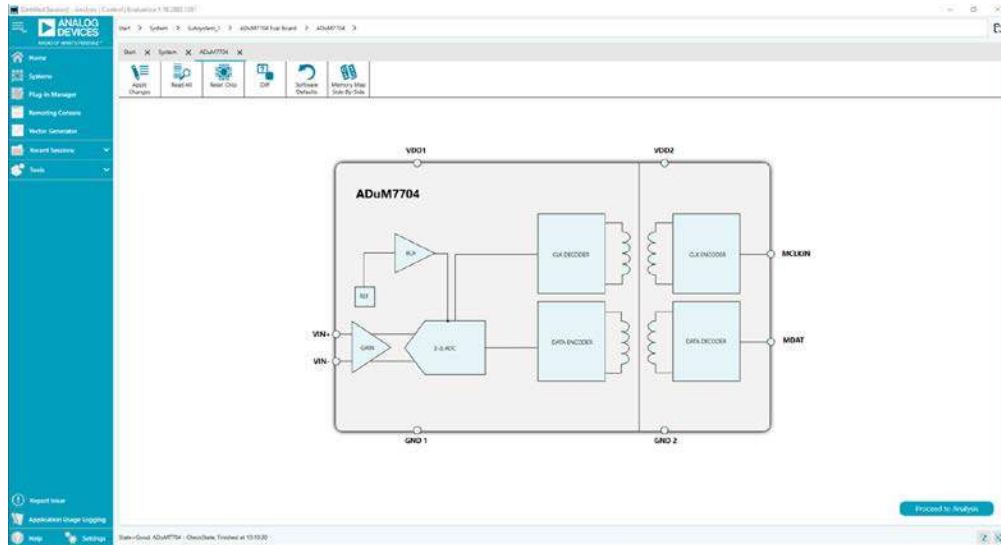
Figure 13. Chip View Window
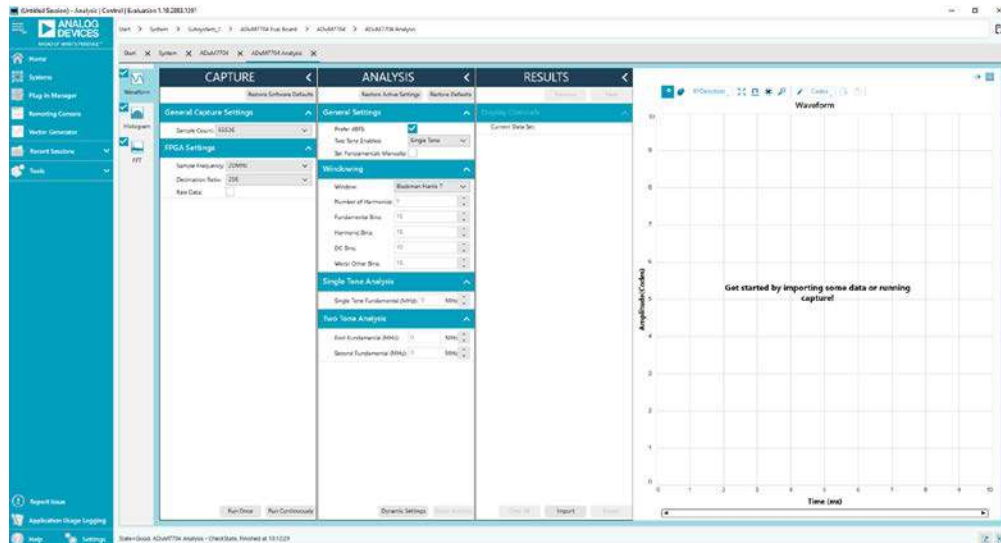
Figure 14. Analysis View Window

WAVEFORM TAB

The **Waveform** tab in the analysis view window displays data in the form of time vs. discrete data values with the results (see Figure 15).

CAPTURE

The **CAPTURE** pane contains the capture settings. These settings reflect onto the registers automatically before data capture.

The **Sample Count** field in the **General Capture Settings** section allows the user to select the number of samples per channel per capture (see Figure 15).

The **FPGA Settings** section contains the FPGA settings that specify the **Sample Frequency** (MCLKIN frequency) used for the serial interface, as well as the **Decimation Ratio** used by the field programmable gate array (FPGA) to filter the data (see Figure 15).

Click **Run Once** at the bottom of the **CAPTURE** pane to start a data capture of the samples at the sample rate specified in the **Sample Count** field (see Figure 15). These samples are stored on the SDP-H1 and are only transferred to the PC when the sample frame is complete.

Click **Run Continuously** to start a data capture that gathers samples continuously with one batch of data at a time (see Figure 15).

RESULTS

The **Display Channels** section allows the user to select which channels to capture (see Figure 15). Data for a specific channel is only shown if that channel is selected before the capture.

The **Waveform** section displays the amplitude and sample frequency for the selected channel.

Click **Export** to export captured data (see Figure 15). The waveform, histogram, and FFT data is stored in .xml files along with the values of parameters at capture.

The **Waveform** graph shows each successive sample of the ADC output (see Figure 15). Zoom in on and pan over the **Waveform** graph using the embedded waveform tools above the graph. Select the channels to display in the **Display Channels** section.

Click the display units dropdown menu labeled **Codes** above the **Waveform** graph (see Figure 15) to select whether the **Waveform** graph displays in units of **Codes**, **Hex**, or **Volts**. The axis controls are dynamic.

Note that the corresponding axis width of the **Waveform** graph automatically adjusts to show the entire range of the ADC results after each batch of samples when either **xy scale dynamic** or **x scale dynamic** is selected. Select the dynamic using the **XYDirection** tool (see Figure 15).

HISTOGRAM TAB

The **Histogram** tab contains the **Histogram** graph and the **RESULTS** pane (see Figure 16).

Click the **RESULTS** pane to display the information related to the dc performance.

The **Histogram** graph displays the number of hits per code within the sampled data (see Figure 16). The **Histogram** graph also displays dc analysis and indicates the noise performance of the ADuM7704.

FFT TAB

The **FFT** tab displays fast Fourier transform (FFT) information for the last batch of samples gathered (see Figure 17).

The **General Settings** section on the **ANALYSIS** pane allows the user to set up the preferred configuration of the FFT analysis (see Figure 17). The fundamental is set manually.

The **Windowing** section on the **ANALYSIS** pane allows the user to select the windowing type used in the FFT analysis, the number of **Harmonic Bins**, and the number of **Fundamental Bins** that must be included (see Figure 17).

The **Single Tone Analysis** and **Two Tone Analysis** sections on the **ANALYSIS** pane allow the user to select the fundamental frequency included in the FFT analysis (see Figure 17). Use the **Two Tone Analysis** settings when analyzing two frequencies.

The **Signal** section on the **RESULTS** pane displays the **Sample Frequency**, **Sample Count**, **Fund Frequency**, and **Fund Power** (see Figure 17).

The **Noise** section on the **RESULTS** pane displays the **SNR** and other noise performance results (see Figure 17).

The **Distortion** section on the **RESULTS** pane displays the harmonic content of the sampled signal and the dc power when viewing the FFT analysis (see Figure 17).

EXITING THE SOFTWARE

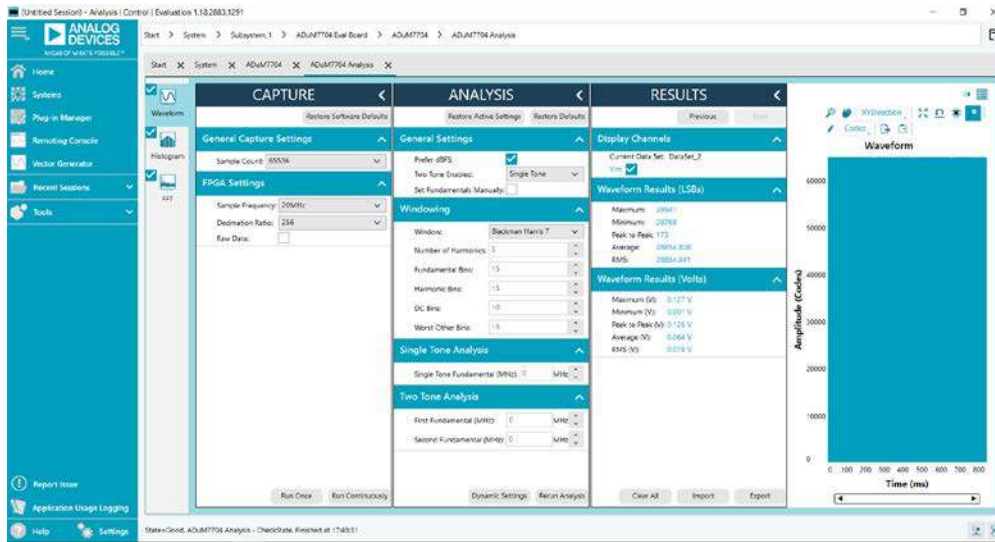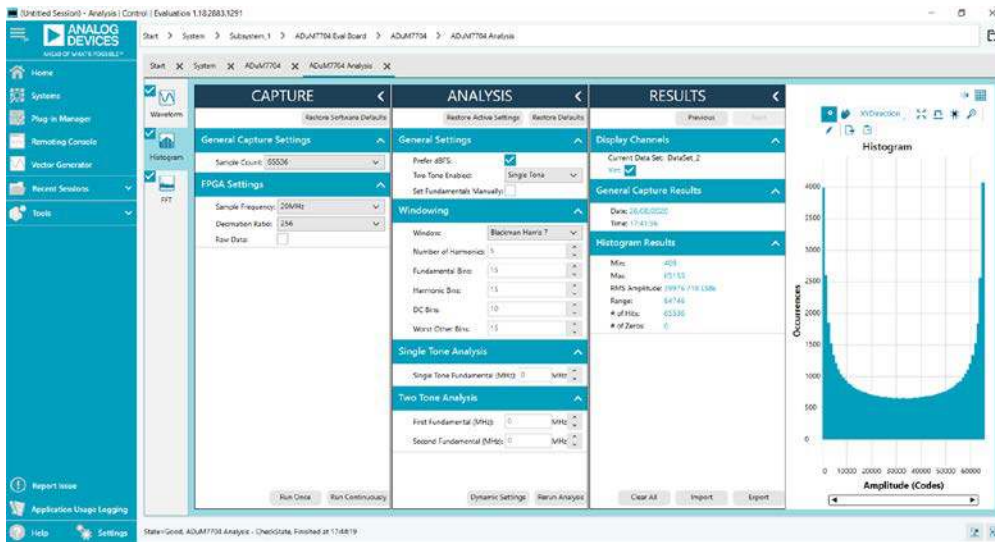To exit the ACE software, click **File** and then click **Exit**.

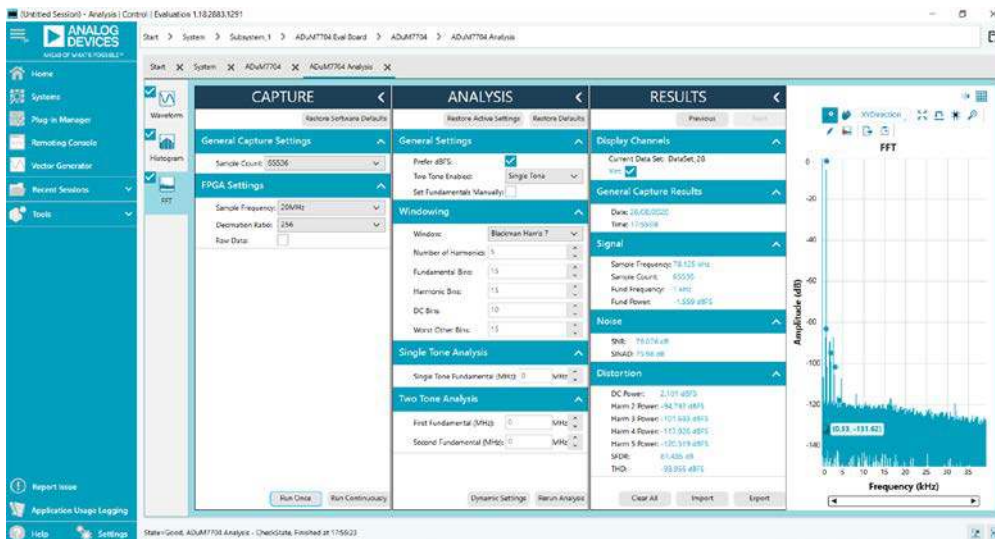Figure 15. **Waveform** Tab

Figure 16. **Histogram** Tab

Figure 17. **FFT** Tab

NOTES

ANALOG DEVICES

www.analog.com