

Automotive-grade N-channel 100 V, 6.8 mΩ typ., 80 A, STripFET™ F7 Power MOSFET in a DPAK package

Datasheet - production data

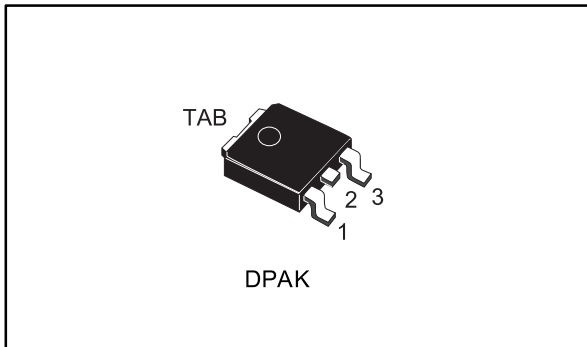
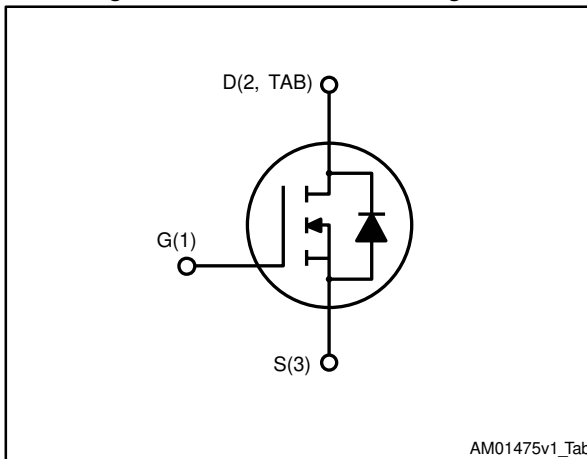


Figure 1: Internal schematic diagram



AM01475v1_Tab

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STD105N10F7AG	100 V	8 mΩ	80 A	120 W

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STD105N10F7AG	105N10F7	DPAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	62	A
$I_{DM}^{(1)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	120	W
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_J	Operation junction temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.25	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
E_{AS}	Single pulse avalanche energy $T_J = 25\text{ }^\circ\text{C}$, $L = 3.5\text{ mH}$, $I_{AS} = 15\text{ A}$, $V_{DD} = 50\text{ V}$, $V_{GS} = 10\text{ V}$	400	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250\ \mu\text{A}$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 100\ \text{V}$			1	μA
		$V_{DS} = 100\ \text{V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}$, $I_D = 40\ \text{A}$		6.8	8	m Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0\ \text{V}$	-	4369	-	pF
C_{oss}	Output capacitance		-	823	-	pF
C_{rss}	Reverse transfer capacitance		-	36	-	pF
Q_g	Total gate charge	$V_{DD} = 50\ \text{V}$, $I_D = 80\ \text{A}$, $V_{GS} = 10\ \text{V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	61	-	nC
Q_{gs}	Gate-source charge		-	26	-	nC
Q_{gd}	Gate-drain charge		-	13	-	nC

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ \text{V}$, $I_D = 40\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\ \text{V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	27	-	ns
t_r	Rise time		-	40	-	ns
$t_{d(off)}$	Turn-off delay time		-	46	-	ns
t_f	Fall time		-	15	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 80 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 80 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	77		ns
Q_{rr}	Reverse recovery charge		-	146		nC
I_{RRM}	Reverse recovery current		-	4		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

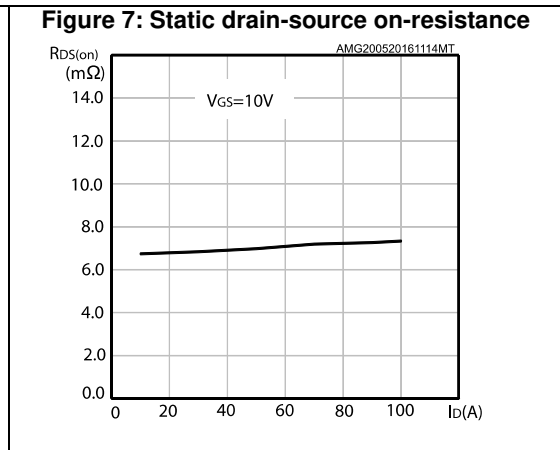
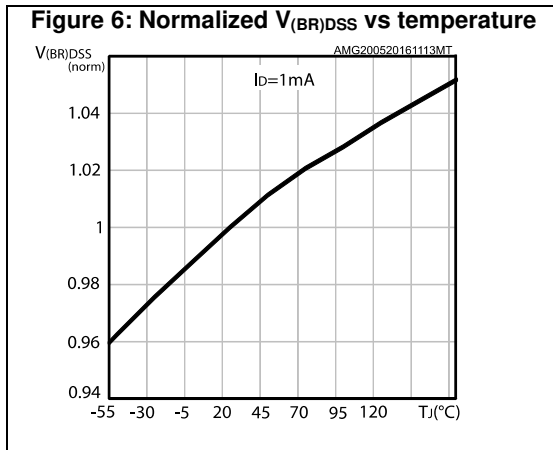
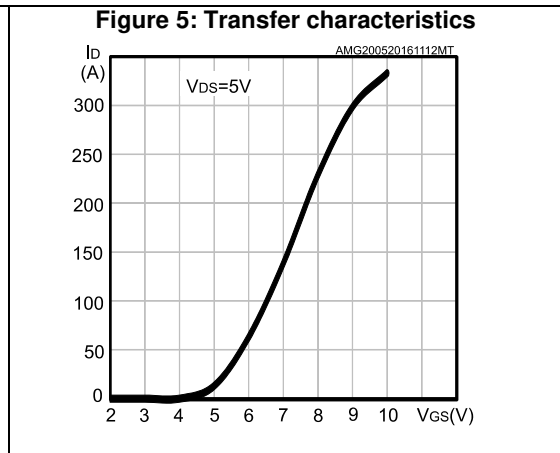
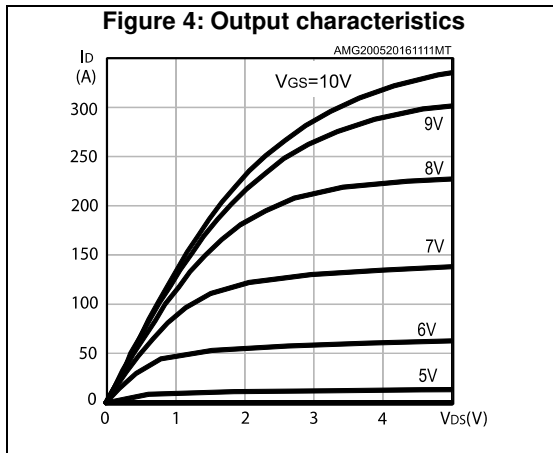
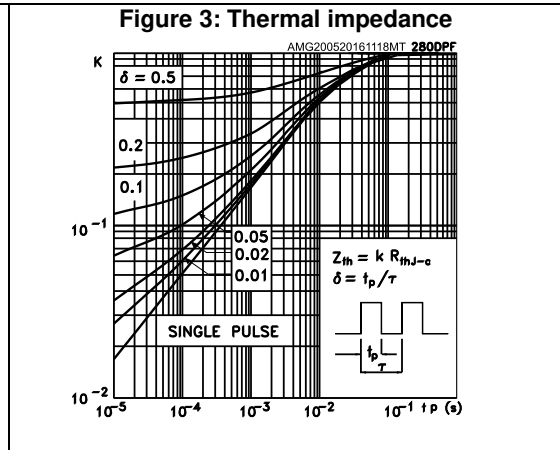
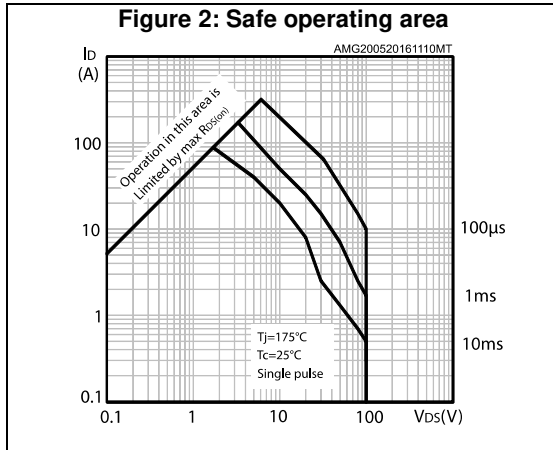


Figure 8: Gate charge vs gate-source voltage

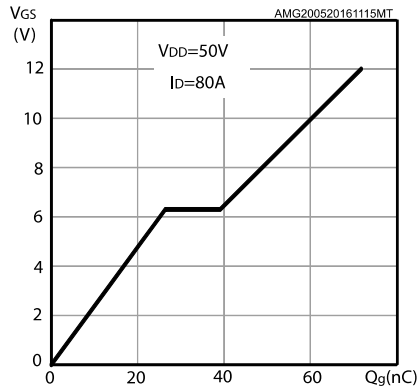


Figure 9: Capacitance variations

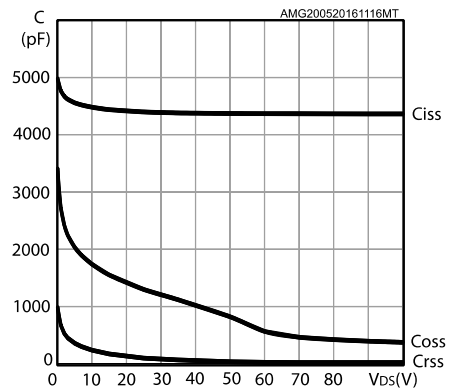


Figure 10: Normalized gate threshold voltage vs temperature

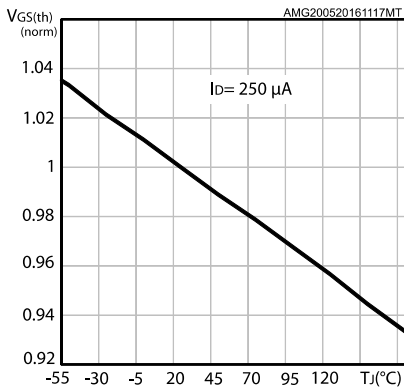


Figure 11: Normalized on-resistance vs temperature

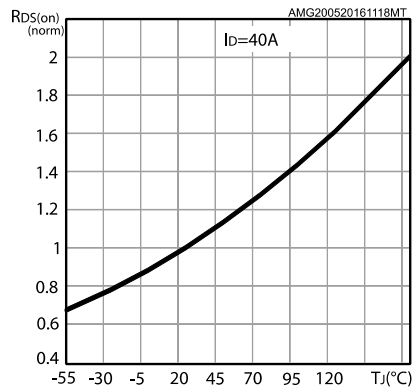
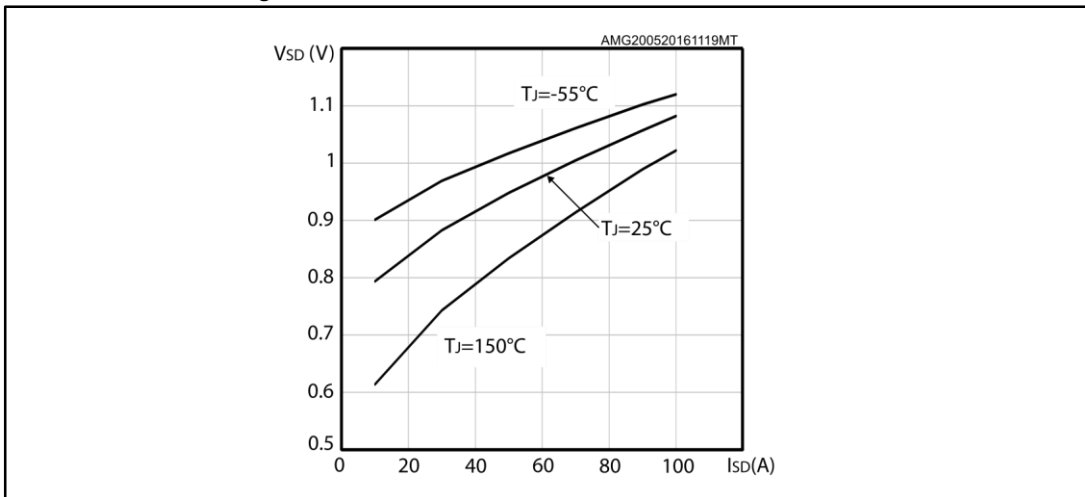


Figure 12: Source-drain diode forward characteristics



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 19: DPAK (TO-252) type A2 package outline

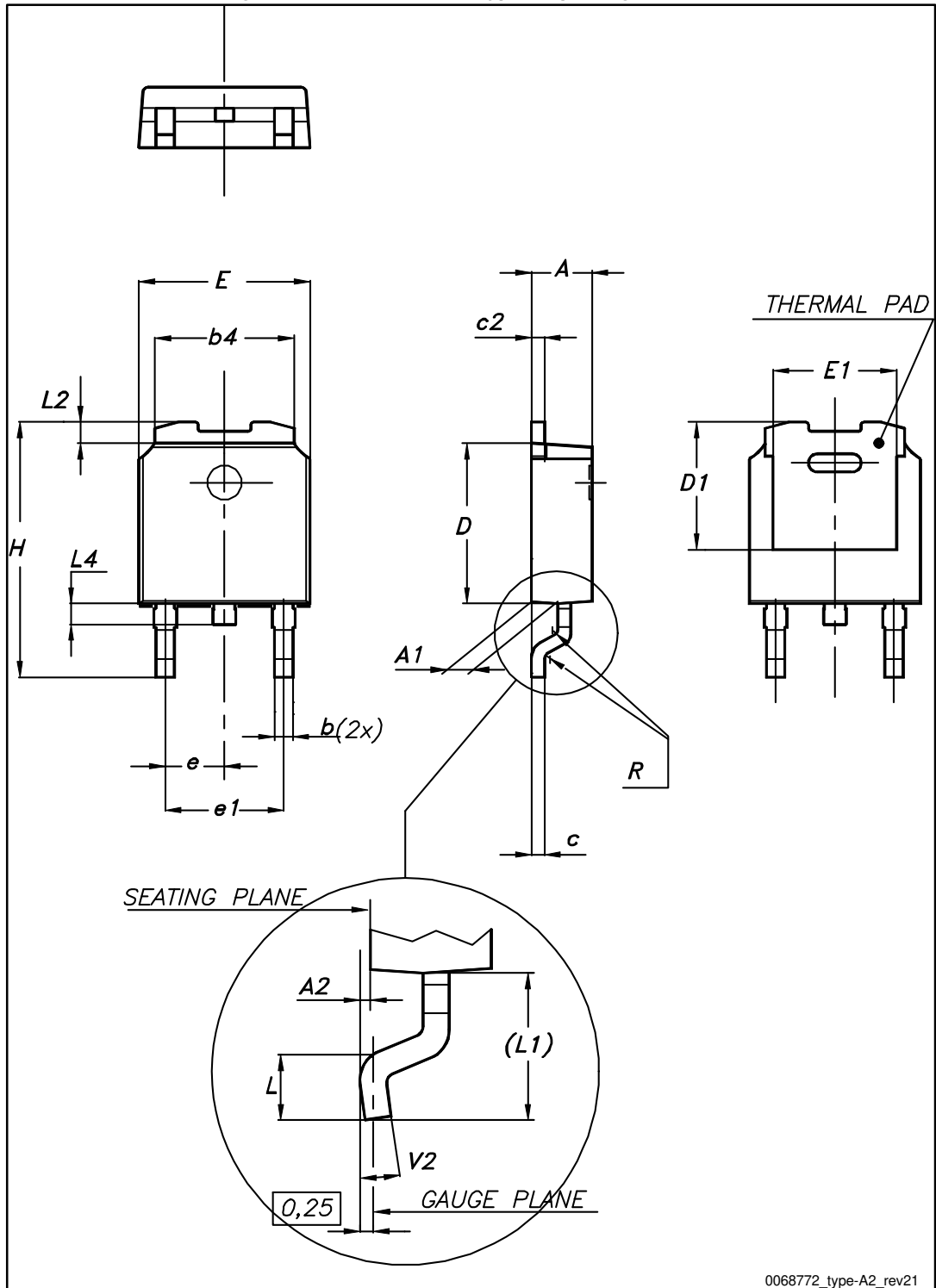
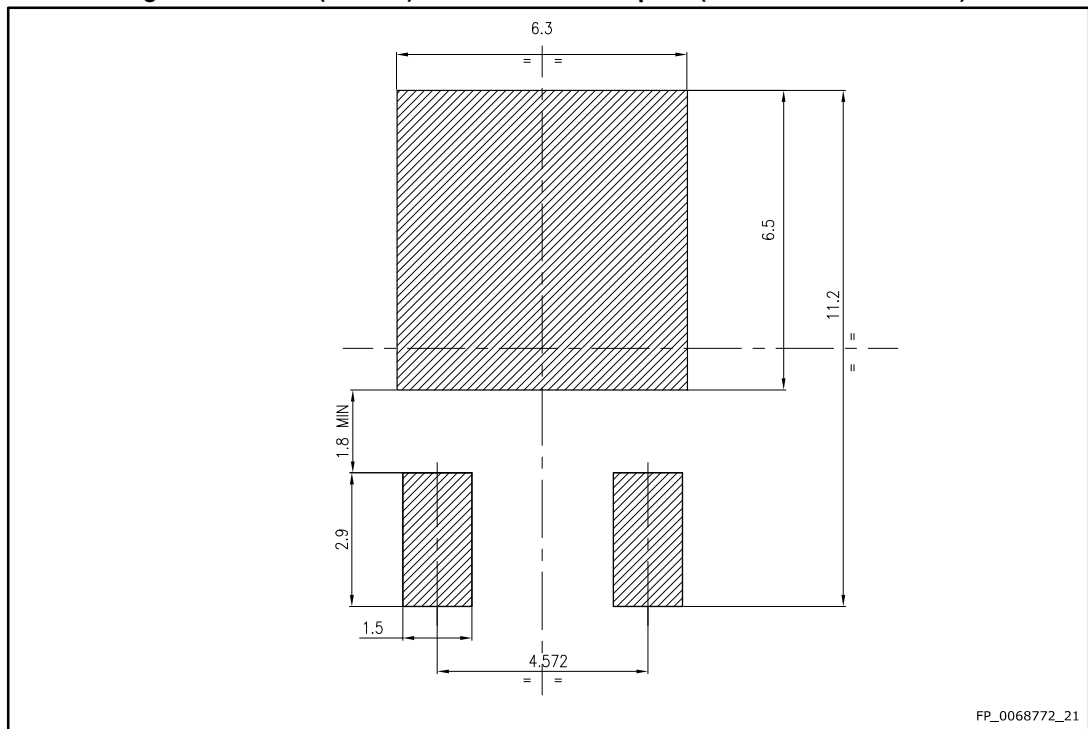


Table 9: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20: DPAK (TO-252) recommended footprint (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
23-Oct-2014	1	First release.
30-Oct-2014	2	Document status promoted from preliminary to production data.
20-May-2016	3	Updated Section 4.1: "DPAK (TO-252) type A2 package information". Minor text changes.
03-Jun-2016	4	Updated title and features in cover page. Updated Table 5: "On/Off states" . Minor text changes.

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