

FC4B22270L1

Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

■ Features

- Low source-source ON resistance: $R_{ss(on)}$ typ. = 18 m Ω ($V_{GS} = 3.8$ V)
- CSP(Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL : Level 1)

■ Marking Symbol: 2J

■ Packaging

Embossed type (Thermo-compression sealing) : 1 000 pcs / reel (standard)

■ Absolute Maximum Ratings $T_a = 25$ °C

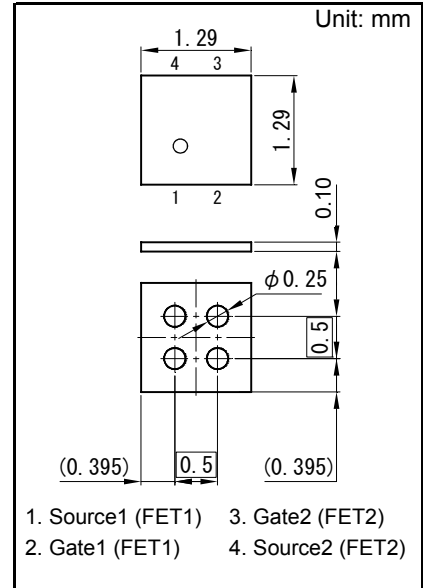
Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	20	V
Gate-source Voltage	VGS	± 12	V
Source Current (DC)	I_S^{*1}	4	A
	I_S^{*2}	8	
Source Current (Pulsed)	I_{Sp}^{*2}	40	A
Total Power Dissipation	PD^{*1}	0.37	W
	PD^{*2}	1.5	
Channel Temperature	Tch	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Thermal Resistance (ch-a)	R_{th}^{*1}	338	°C/W
	R_{th}^{*2}	83	

Note *1 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm)

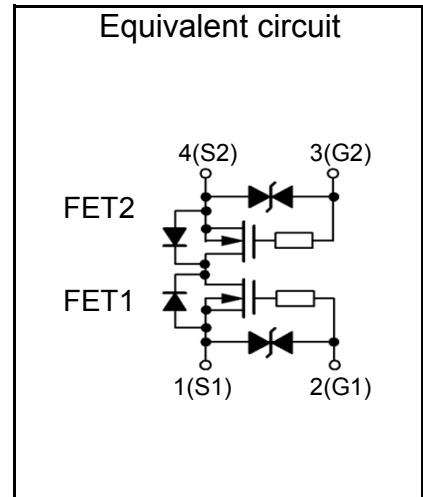
using the minimum recommended pad size (36 μ m Copper).

*2 Mounted on Ceramic substrate (70 mm × 70 mm × t1.0 mm).

*3 $t = 10$ μ s, Duty Cycle ≤ 1 %



Panasonic	ULGA004-W-1313-RA
JEITA	—
Code	—



■ Electrical Characteristics Ta = 25 °C ± 3 °C

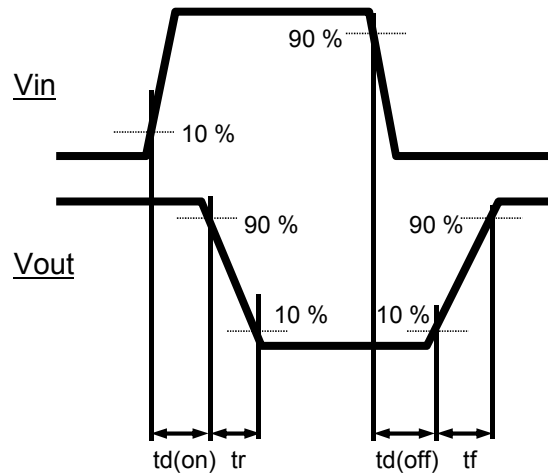
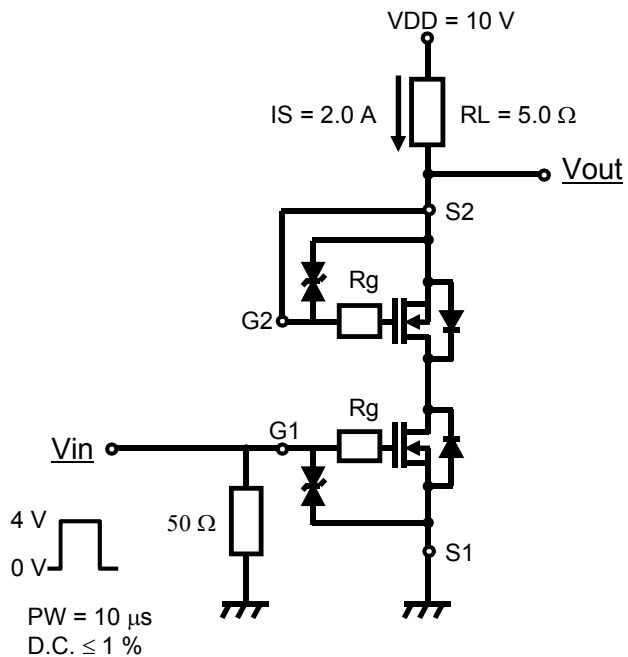
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	20			V
Zero Gate Voltage Source Current	ISSS	VSS = 20 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	IS = 0.31 mA, VSS = 10 V	0.35	0.90	1.4	V
Source-source On-state Resistance	RSS(on)1	IS = 2.0 A, VGS = 4.5 V	12	17	22	mΩ
	RSS(on)2	IS = 2.0 A, VGS = 3.8 V	12.5	18	23	
	RSS(on)3	IS = 2.0 A, VGS = 3.1 V	13.5	19	26.5	
	RSS(on)4	IS = 2.0 A, VGS = 2.5 V	14	22	37	
Body Diode Forward Voltage	VF(s-s)	IF = 2.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance ^{*1}	Ciss	VSS = 10 V, VGS = 0 V, f = 1 KHz		910		pF
Output Capacitance ^{*1}	Coss			105		
Reverse Transfer Capacitance ^{*1}	Crss			80		
Turn-on delay Time ^{*1,*2}	td(on)	VDD = 10 V, VGS = 0 to 4.0 V		0.25		μs
Rise Time ^{*1,*2}	tr	IS = 2.0 A		0.55		
Turn-off delay Time ^{*1,*2}	td(off)	VDD = 10 V, VGS = 4.0 to 0 V		1.65		μs
Fall Time ^{*1,*2}	tf	IS = 2.0 A		1.0		
Total Gate Charge ^{*1}	Qg	VDD = 10 V		9		nC
Gate-source Charge ^{*1}	Qgs	VGS = 0 to 4.0 V,		2.6		
Gate-drain Charge ^{*1}	Qgd	IS = 2.0 A		2.4		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing

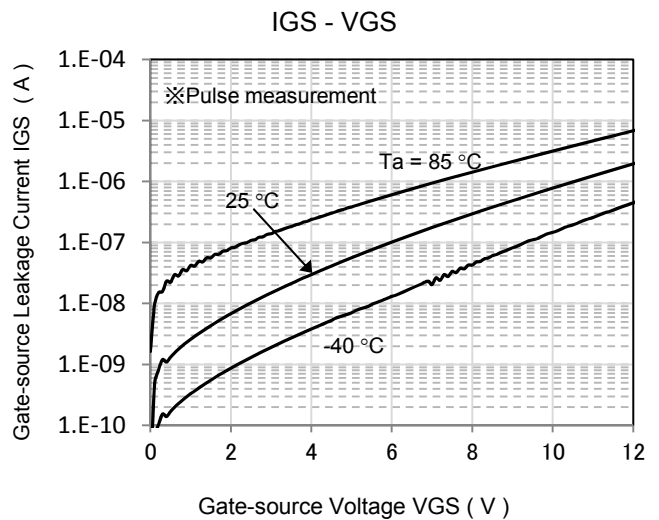
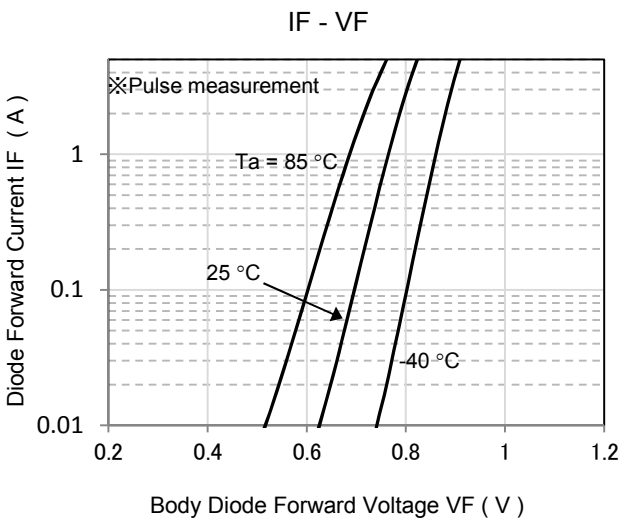
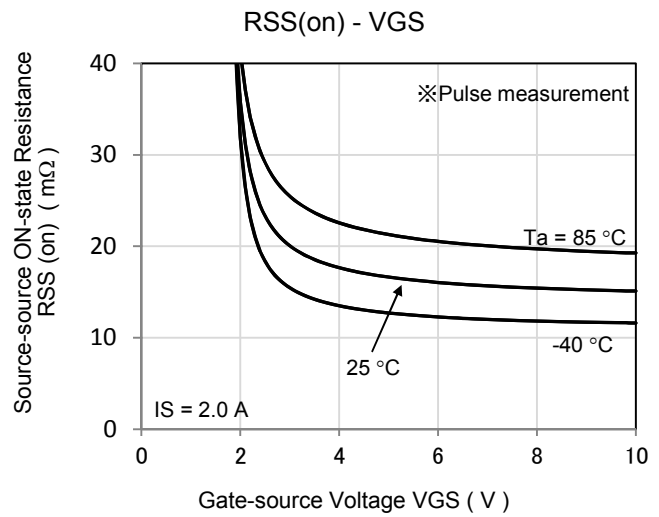
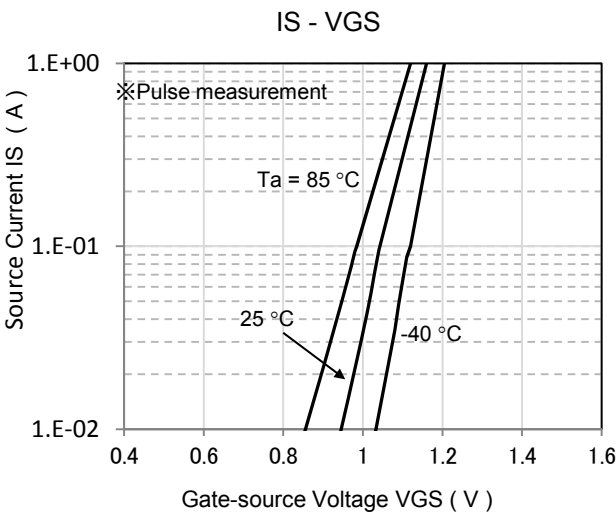
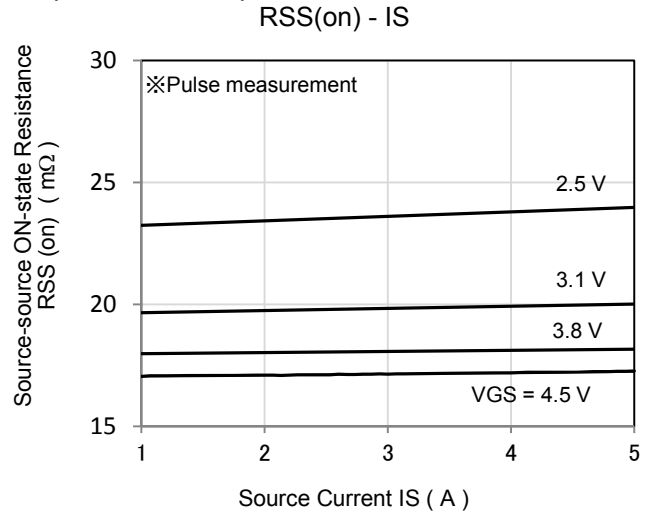
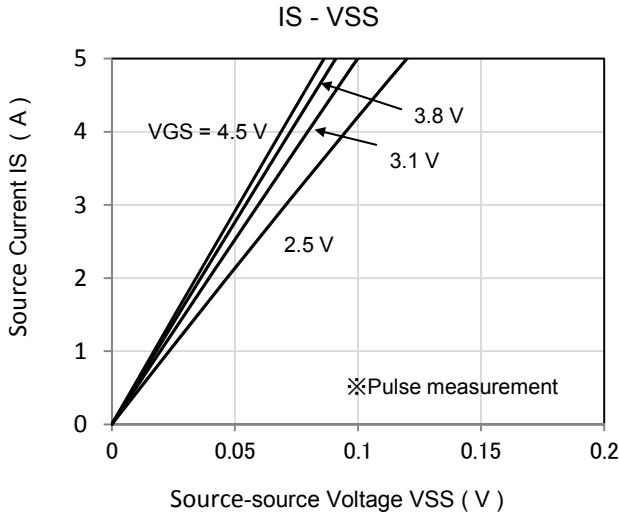
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

Note2: Measurement circuit



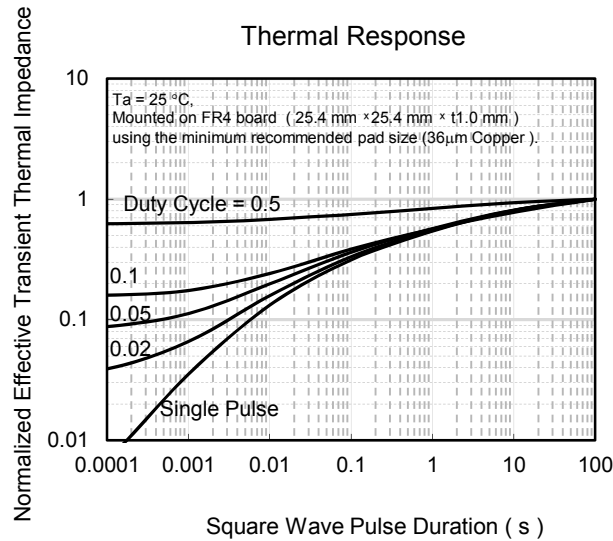
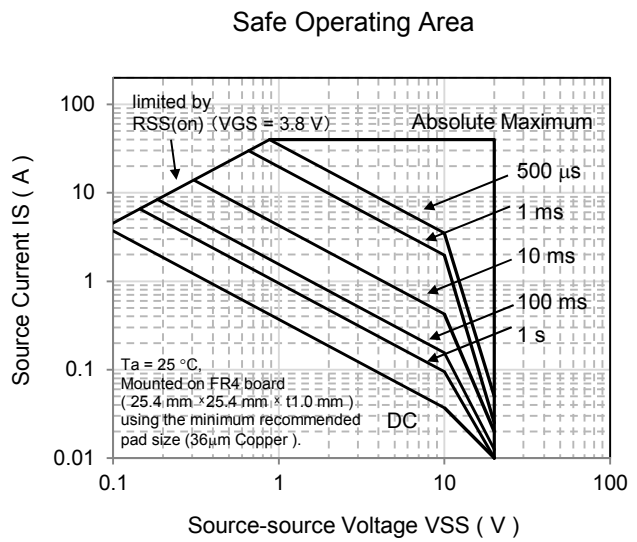
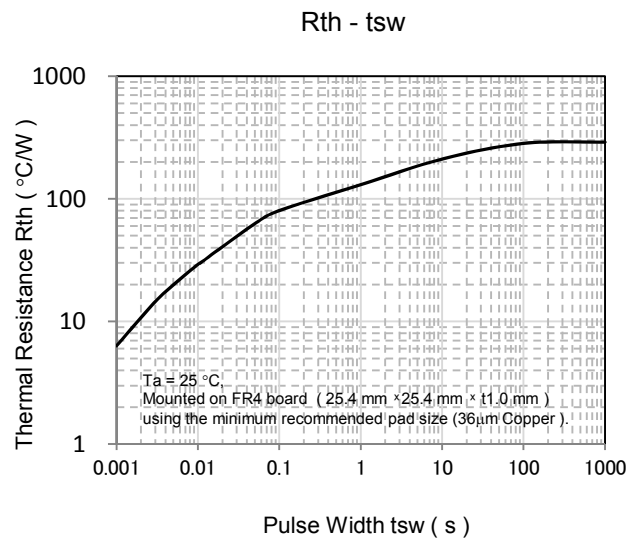
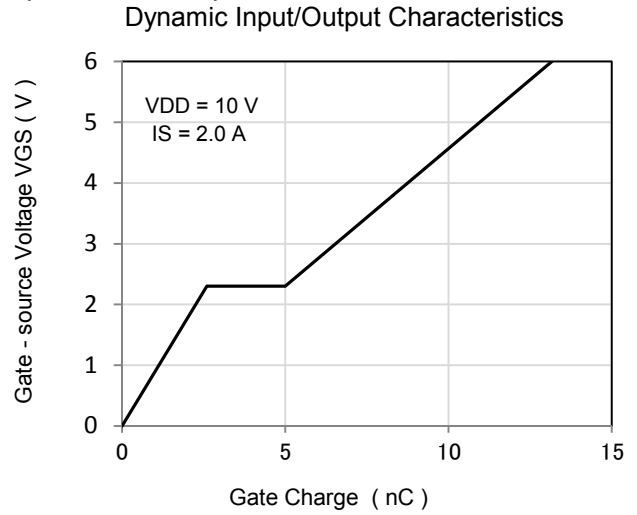
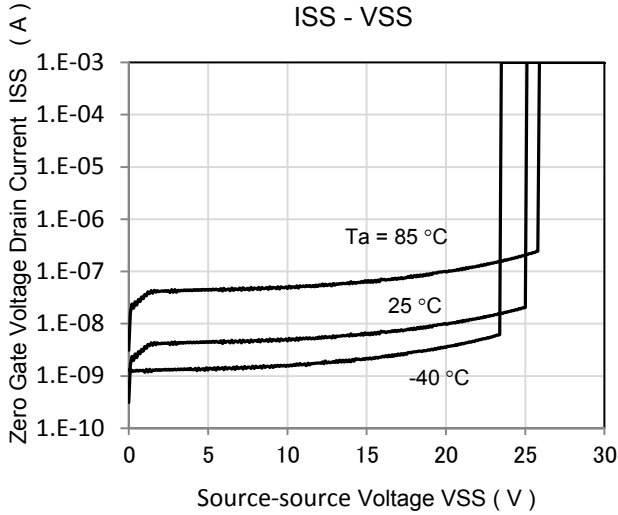


Technical Data (reference)



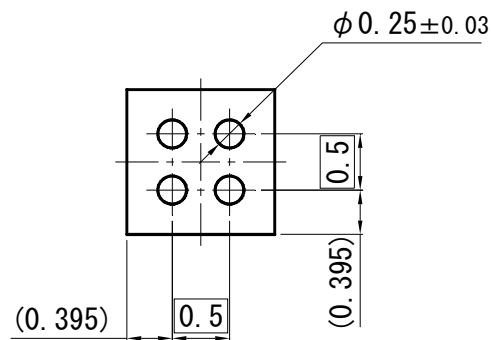
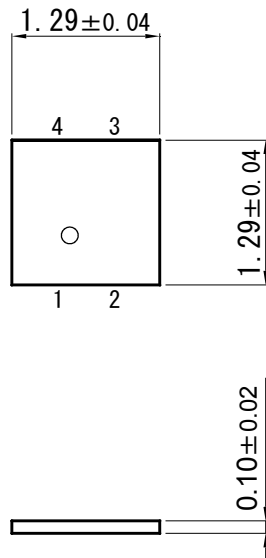


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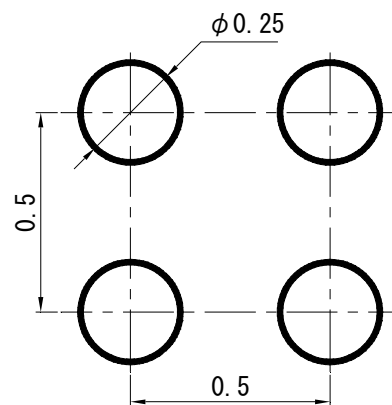
■ Outline (ULGA004-W-1313-RA)

Unit: mm



■ Land Pattern (Reference)

Unit: mm



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