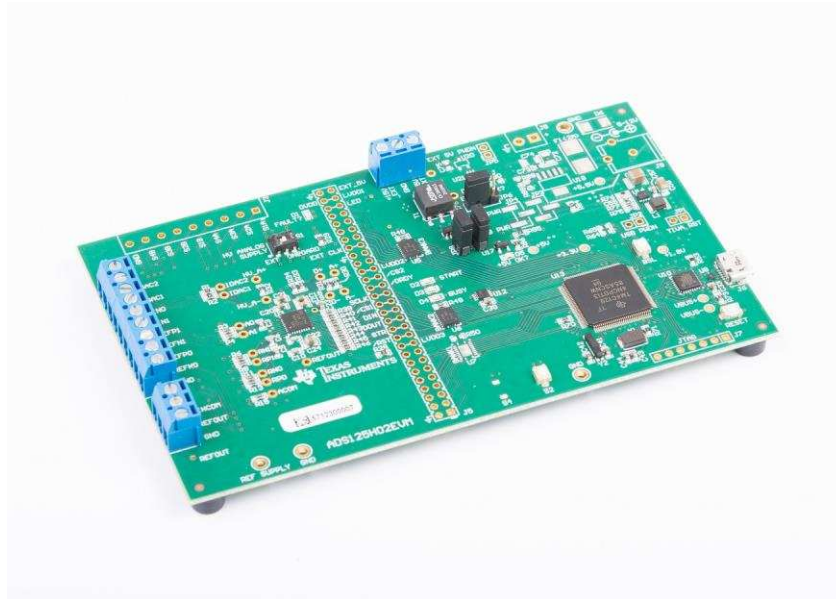


ADS125H02 Evaluation Module



ADS125H02 Evaluation Module

The ADS125H02 is a 2-channel, 24-bit, 40-kSPS, delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) with an integrated ± 18 -V programmable gain amplifier (PGA) with a 1-G Ω input impedance. The device also includes a voltage reference and features to enhance data reliability such as cyclic redundancy check (CRC) and signal monitors.

The ADS125H02EVM is an evaluation module kit providing hardware and software support for evaluation of the ADS125H0x, delta-sigma analog-to-digital converter (ADC). The kit uses the Texas Instruments [TM4C1294NCPDT](#) processor to communicate with the ADC via SPI and provide communication with a PC over the USB interface. The software application is downloaded from the Texas Instruments website and runs on the Windows operating system allowing for register manipulation and data collection from the ADC. The ADS125H02EVM kit includes the ADS125H02 device along with a USB micro cable.

This document includes a detailed description of the hardware (HW), software, bill of materials, and schematic for the EVM.

Throughout this document, the term *EVM* is synonymous with the ADS125H02EVM, demonstration kit, and evaluation module. The term *GUI* is synonymous with *Delta-Sigma ADC Evaluation Software*, core application, and EVM software. The use of *Tiva™* is synonymous with the TM4C1294NCPDT microcontroller.

Table 1. Related Documentation

Device	Literature Number
ADS125H02	SBAS790
Delta-Sigma ADC Evaluation Software User Manual	SBAU260

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1 EVM Overview

1.1 Description

This user's guide describes the operation and use of the ADS125H02 evaluation module. The EVM platform is intended for evaluating the ADS125H02 performance and functionality.

1.2 Requirements

1.2.1 Software Requirements

PC with Microsoft® Windows® 7 or higher operating system.

1.2.2 Hardware Requirements

PC with available USB 2.0 or greater connection.

1.2.2.1 Power Supply

The ADS125H02EVM is USB powered and has an onboard ± 15 -V supply that is boosted from the USB power. An external ± 15 -V supply may also be used for operation of the EVM. A header for an external ± 15 -V supply is provided at J4 through the left position of switch S1.

1.3 Software Reference

For the core software documentation, see the [Delta-Sigma ADC Evaluation Software User Manual](#) or navigate to the *File -> About* option from within the GUI, then click on the *Software user guide* icon.

1.4 Supported Functionality

1.4.1 Hardware Functionality

The EVM features the following hardware capabilities:

- Onboard 5-V AVDD supply operation
- Onboard 3.3-V DVDD supply
- Onboard or external high voltage power supply, either bipolar supplies or unipolar supply
- Digital header for external processor or controller configuration
- Analog header and configurable input circuitry for direct sensor connections
- Place holder for optional REF62xx external reference source
- Onboard (not installed) high-voltage multiplexer for analog inputs
- Fault LED for STATUS or CRC error notification

1.4.2 Software Functionality

The EVM features the following software functions:

- Device conversion control
- Device software reset
- Device power down
- Register read and write
- Conversion result readback
- Offset and system input calibration
- Readback of STATUS and CRC data bytes (for error detection)
- CRC of SPI communication between the ADC and the host (for error prevention or detection of data transmission)

2 Quick Start

This section provides a guide to quickly begin using the EVM.

2.1 Default Jumper and Switch Configuration

The EVM is configured with the settings listed in [Table 2](#) and shown in [Figure 1](#).

Table 2. Default Settings

Jumper	Position	Function
JP1	(Not Installed)	Use onboard processor
JP2	(Not Installed)	USB-derived supplies ON
JP3	(Not Installed)	DVDD from USB power (1-2 connection via R84)
JP4	(Not Installed)	AVDD from USB power (1-2 connection via R85)
JP5	(Not Installed)	External +5-V power down
JP6	Installed	+5-V supply selection, jumper installed left
JP7	(Not Installed)	Onboard HV supply disable, jumper not installed
JP8	Installed	HV transformer driver clock input, jumper installed to select internal clock
Switch	Position	Function
S1	Left	Bipolar high-voltage analog supply selection (± 15 V)

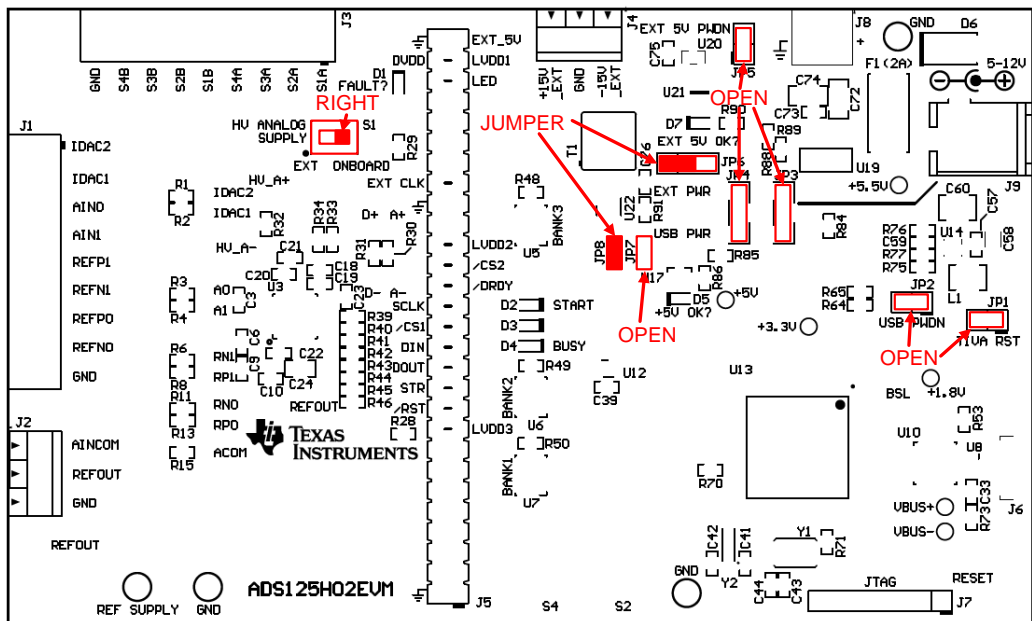


Figure 1. Default Configurations for ADS125H02 EVM

2.2 Powering the EVM

The EVM is powered through the USB interface with the PC. This power includes a +5-V and an HV supply generated onboard the EVM from the USB. Additionally, the HV supplies the ADS125H02 (± 18 V to ± 5 V), which can be powered from an external source from header connections on J4 through switch S1. Follow the installation and connection procedure in [Section 2.3](#) before connecting the EVM to the PC. [Section 2.2.1](#) and [Section 2.2.2](#) provide additional details about the analog and digital power supply configurations of the ADC. [Section 2.2.3](#) provides additional details about the high voltage supply.

2.2.1 Analog Supply Configuration of the ADC

The ADS125H02 low-voltage analog supply requires a 5-V source for the AVDD. The EVM provides onboard 5-V supply for the AVDD low-voltage analog supply.

Use R30 to measure the AVDD supply current, either by measuring the voltage drop across this resistor or by removing the resistor and connecting a dc current meter between the $A+$ and $A-$ test points.

2.2.2 Digital Supply Configuration of the ADC

The ADS125H02 digital supply requires a 2.7-V to 5.25-V source connected between DVDD and DGND. The EVM provides a 3.3-V onboard digital supply for the digital supply of the ADC.

R31 can be use to measure the DVDD supply current, either by measuring the voltage drop across this resistor or by removing the resistor and connecting a dc current meter between the $D+$ and $D-$ test points.

2.2.3 High-Voltage Analog Supply Configuration of the ADC

The ADS125H02 high-voltage supply requires a high-voltage power supply ranging from ± 18 V to ± 5 V for bipolar operation, or ranging from +36 V to +10 V for unipolar operation (when HV_AVSS = GND). An onboard HV supply generator supplies ± 15 V from the USB connection.

The EVM also provides terminal block J4 to connect an external ± 15 V for the high-voltage analog supply of the ADC when setting S1 to the left position. When switching S1, TI recommends disconnecting the USB cable from the EVM, toggling the switch, and then reconnecting the USB cable.

R32 can be use to measure the high-voltage supply current, either by measuring the voltage drop across this resistor or by removing the resistor and connecting a dc current meter between the HV_A+ and HV_A- test points.

2.3 Software Installation and Hardware Connection Procedure

Use the following steps at startup:

1. Download all required software from www.ti.com/tool/ads125H02evm.
2. Install the GUI software on the PC.
3. Install the ADS125H02 device package software on the PC.
4. Ensure all jumpers and switches are configured in the default configuration per [Table 2](#) and [Figure 1](#).
5. Connect the EVM to the PC using a USB cable to power the board.
6. Attach the high-voltage supply to J4 and ensure that S1 is set to the left. Alternately, use the onboard high-voltage supply (not installed) and set S1 to the right.
7. If prompted, install any required drivers.
8. Start the GUI application on your PC. The GUI automatically detects the connected EVM.

NOTE: After powering the EVM, the green D2 and +5V LEDs light up.

3 Hardware Reference

3.1 Jumper and Switch Configuration Reference

Table 3 provides all jumper and switch configuration settings for the EVM.

Table 3. Jumper and Switch Options

Jumper	Position	Description
JP1	Operation of EVM with external digital signals	
	Installed (ON)	Hold the Tiva processor (U13) in reset and disable level shifters to allow external digital signals
	Uninstalled (OFF)	Normal operation with onboard Tiva processor (default)
JP2	Power down USB power supplies	
	Installed (ON)	USB-derived power supplies disabled and powered down
	Uninstalled (OFF)	USB-derived power supplies enabled and ON (default)
JP3	Digital supply source	
	1–2 shorted	Digital supply (U18) powered from USB power (default using R94 as the short)
	2–3 shorted	Digital supply (U18) powered from external supply source
	Open	No digital system power provided
JP4	5-V supply source	
	Installed (ON)	5-V supply powered from USB (default using R85 as the short)
	Uninstalled (OFF)	No analog supply powering AVDD
JP5	EXT_5V supply power down	
	Installed (ON)	External supply regulator (U18-not installed) disabled
	Uninstalled (OFF)	External supply regulator (U18-not installed) enabled (default)
JP6	Onboard 5-V source for the HV analog supply source	
	Right	5-V supply sourced from EXT_5V
	Left	5-V supply sourced from USB power (default)
JP7	Disable for the onboard HV analog supply	
	Installed (ON)	Holds enable low to disable onboard HV analog supply
	Uninstalled (OFF)	Onboard HV analog supply enabled (default)
JP8	External clock for transformer driver for the onboard HV analog supply	
	Installed (ON)	Transformer driver (U22) uses onboard oscillator for onboard HV analog supply (default)
	Uninstalled (OFF)	Connection to transformer driver (U22) external clock
Switch	Position	Description
S1 ⁽¹⁾	High-voltage analog supply selection switch	
	Right (pin connections: 5–6, 2–3)	High-voltage supply sourced from onboard ±15-V supply (not installed)
	Left (pin connections: 5–4, 2–1)	High-voltage supply sourced from external supplies through J4 (default)
S2	Reset FAULT button	
	Closed (depressed)	Clears FAULT indicator and writes 0x00 to the STATUS register of the ADC
	Open (normally)	Normal operation
S3	BSL button for <i>Device Firmware Update</i> (DFU) mode	
	Closed (depressed)	Total Tiva FLASH erasure (on reset Tiva enumerates as a DFU device)
	Open (normally)	Normal operation
S4	Spare button (not installed)	
	Closed (depressed)	
	Open (normally)	

⁽¹⁾ Switch is DPDT. Pin 1 is identified with a dot on the PCB silkscreen.

Table 3. Jumper and Switch Options (continued)

Jumper	Position	Description
S5	Tiva reset (U13 RST) button	
	Closed (depressed on RESET)	Tiva held in RESET, level shifters (U5, U6, and U7) tri-stated
	Open (normally)	Normal operation

3.2 Header, Connector, and Test Point Reference

This section provides the connection information and details for the connectors and test points utilized on the EVM.

3.2.1 Analog Input Terminal Blocks

Connect the analog input to the EVM at the terminal blocks located on the left side of the board (as shown in Figure 2) to evaluate the performance of the ADS125H02. The functions for these terminal blocks are listed in Table 4. At no time apply a voltage to the inputs of the ADS125H02 that exceeds the absolute maximum ratings for the device.

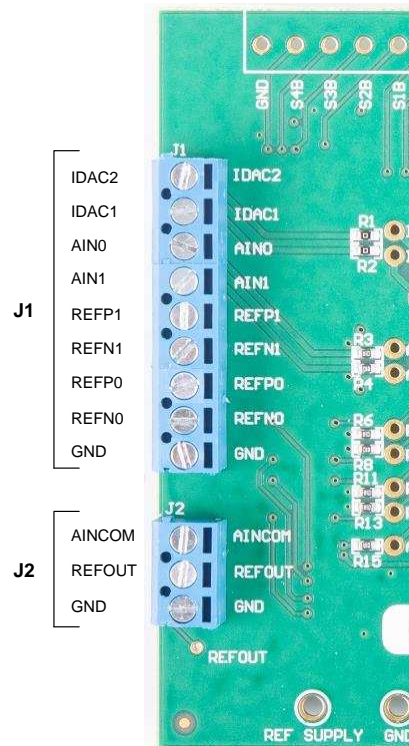


Figure 2. Input Terminal Blocks

Table 4. Analog Input Terminal Blocks, J1–J3

Pin	Function	Test Point	ADS125H02 Input Pin
J1			
1	IDAC current output	IDAC2	IDAC2
2	IDAC current output	IDAC1	IDAC1
3	Analog input ⁽¹⁾	A0	AIN0
4	Analog input ⁽¹⁾	A1	AIN1
5	External reference input 1 / GPIO 1	RP1	REFP1/GPIO0
6	External reference input 1 / GPIO 0	RN1	REFN1/GPIO1
7	External reference input 0	RP0	REFP0
8	External reference input 0	RN0	REFN0
9	GND	–	GND
J2			
1	Analog input ⁽¹⁾	ACOM	AINCOM
2	Reference output	–	REFOUT
3	GND	–	GND
J3 (not installed)			
1	Multiplexer analog input	S1A	–
2	Multiplexer analog input	S2A	–
3	Multiplexer analog input	S3A	–
4	Multiplexer analog input	S4A	–
5	Multiplexer analog input	S1B	–
6	Multiplexer analog input	S2B	–
7	Multiplexer analog input	S3B	–
8	Multiplexer analog input	S4B	–
9	GND	–	GND

⁽¹⁾ Analog inputs are pinned out to terminal blocks through RC filters. See [Figure 19](#) for additional connection details.

3.2.2 High-Voltage Supply Terminal

The EVM has an optional external high-voltage supply connection (nominally $\pm 15\text{ V}$) that is connected to the J4 terminal block located on the top center side of the board, as shown in [Figure 3](#). This connection provides a high voltage bipolar supply to the EVM for evaluation purposes. The functions for these terminal blocks are listed in [Table 5](#). Never apply a supply voltage that exceeds the absolute maximum ratings for the power supply of the ADS125H02.

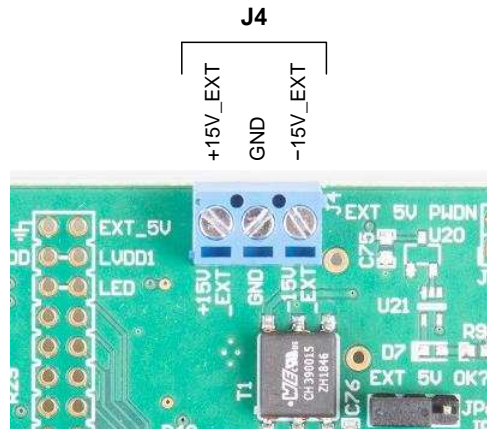


Figure 3. High-Voltage Supply Terminal Block

Table 5. High-Voltage Supply Terminal Block, J4

Pin	Function	Test Point	ADS125H02 Input Pin
J4			
1	-15-V supply input	-15V_EXT	HV_AVSS
2	GND	GND	GND
3	+15-V supply input	+15V_EXT	HV_AVDD

3.2.3 External Clock

By default, a clock is supplied by the internal oscillator of the ADC when the CLKIN pin is low. However, the EVM also provides the capability to connect an external clock directly to the ADC using the J5 connector; see [Figure 21](#). When connecting to J5, a direct connection can be made between pins 42 (CLKIN) and 40 (GND). A typical clock source of 7.3728 MHz (10.24 MHz only for 40000 SPS operation) tracks with all timing described in the [ADS125H02 data sheet](#).

NOTE: The CLKIN pin connects to the Tiva microcontroller. The microcontroller holds the CLKIN pin low in order to enable the internal oscillator of the ADC. Before applying an external clock, be sure to disable the GPIO output on this pin by sending the *HOLDLOCK 0* command, as described in [Table 8](#).

3.2.4 Digital Interface Header

Table 6 lists the functions and pin numbers for all signals used on the digital interface.

Table 6. Digital Interface, J5

Function	ADC Side		Processor Side	
	Signal Name	Pin Number ⁽¹⁾	Pin Number ⁽²⁾	Signal Name , Tiva Connection ⁽³⁾
External voltage input	GND	56	55	EXT_5V
Bank3 level-shifter voltage	DVDD	54	53	LVDD1
GPIO for the ADC	FAULT_LED	52	51	PD7
	EXT_CLK	42	41	PD3 (Unused)
Bank2 level-shifter voltage	DVDD	36	35	LVDD2
SPI0	ADC_nCS2	34	33	PA0
	ADC_nDRDY	32	31	PA1
	ADC_SCLK	30	29	PA2 (SSI0CLK)
	ADC_nCS1	28	27	PA3
	ADC_MOSI (DIN)	26	25	PA4 (SSI0XDAT0)
	ADC_MISO (DOUT)	24	23	PA5 (SSI0XDAT1)
ADC GPIOs	ADC_START	22	21	PA6
	ADC_nRESET	20	19	PA7
Bank1 level-shifter voltage	DVDD	18	17	LVDD3 (Unused)

⁽¹⁾ Even-numbered pins not included in this list are connected to GND.

⁽²⁾ Odd-numbered pins not included are connected to the Tiva microcontroller (via level shifters) but the functionality is not used for this EVM. For connection details, see Figure 21.

⁽³⁾ Signals connected to the Tiva microcontroller are named according to their respective processor pin connections. For connection details, see Figure 21.

3.2.5 Test Points

The test points listed in Table 7 may be used to probe onboard voltage supplies and signals.

Table 7. Test Points

Function	Signal Name	Restrictions
ADC side		
Excitation current source (IDAC2)	IDAC2	Probe only
Excitation current source (IDAC1)	IDAC1	Probe only
Analog input (AIN0)	A0	Probe only
Analog input (AIN1)	A1	Probe only
Reference input (REFN1 / GPIO1)	RN1	Probe only
Reference input (REFP1 / GPIO0)	RP1	Probe only
Reference input (REFN0)	RN0	Probe only
Reference input (REFP0)	RP0	Probe only
Analog input (AINCOM)	ACOM	Probe only
Internal reference (REFOUT)	REFOUT	Probe only
External Reference Supply Source	REF SUPPLY	Probe only
Analog supply (AVDD supply side of sense resistor)	A+	Probe only
Analog supply (AVDD device side of sense resistor)	A-	Probe only
Digital supply (DVDD supply side of sense resistor)	D+	Probe only
Digital supply (DVDD device side of sense resistor)	D-	Probe only
HV analog supply (HV_AVDD supply side of sense resistor)	HV_A+	Probe only
HV analog supply (HV_AVDD device side of sense resistor)	HV_A-	Probe only

Table 7. Test Points (continued)

Function	Signal Name	Restrictions
2-V subregulator output (BYPASS)	BYPASS	Probe only
Internal reference (REFOUT)	REFOUT	Probe only
5-V supply	+5V	Probe only
3.3-V supply	+3.3V	Probe only
Ground	GND	Probe only
Processor Side		
USB-sourced supply	USB_VBUS (VBUS+)	Probe only
USB-sourced supply	USB_VBUSP (VBUS-)	Probe only
5.5-V output (U14)	USB_BOOST (+5.5V)	Probe only
1.8-V output (U16)	+1.8V	Probe only
5.0-V output (U15)	+5V	Probe only
Ground	GND	Probe only
3.3-V output (U18)	+3.3V	Probe only
Step-up transformer output (not populated)	HVBoost	Probe only
Inverting transformer output (not populated)	HVInvert	Probe only

4 Software Details

4.1 Installing the Software

4.1.1 Delta-Sigma ADC Evaluation Software

Download the *Delta-Sigma ADC Evaluation Software* installer, as shown in [Figure 4](#), from the [DELTASIGMAEVAL-GUI](#) page and save to a local folder. Run the installer and follow the on-screen prompts. Future software versions may show slightly different screens.

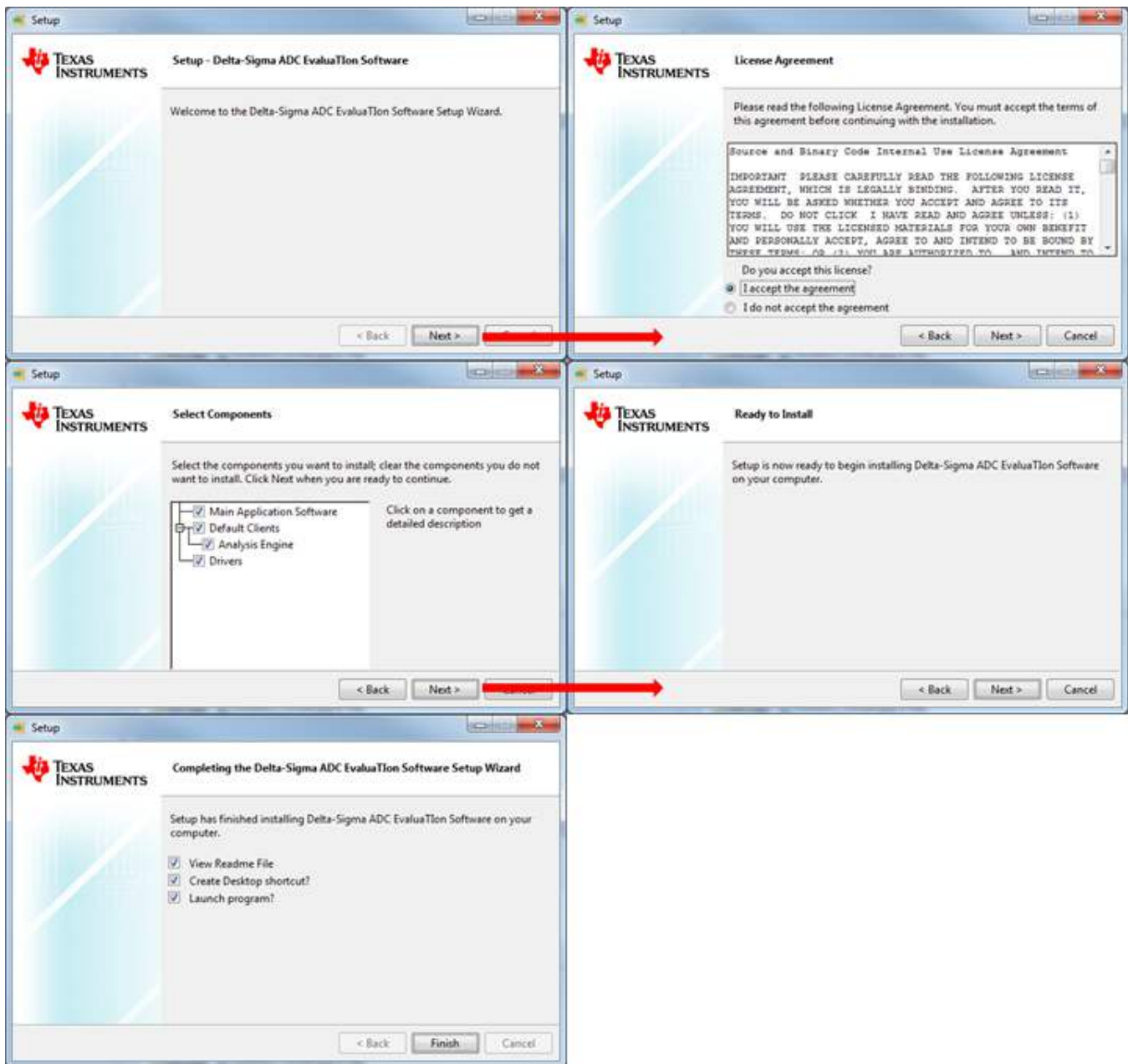


Figure 4. Delta-Sigma Evaluation Engine Installation Instructions

4.1.2 ADS125H02 EVM Device Package

Download the *ADS125H02 Device Package* installer, as shown in [Figure 5](#), from the [ADS125H02EVM tool page](#) for the ADS125H02EVM and save the file to a local folder. Run the appropriate device package installer and follow the on-screen prompts. Future software versions may show slightly different screens.

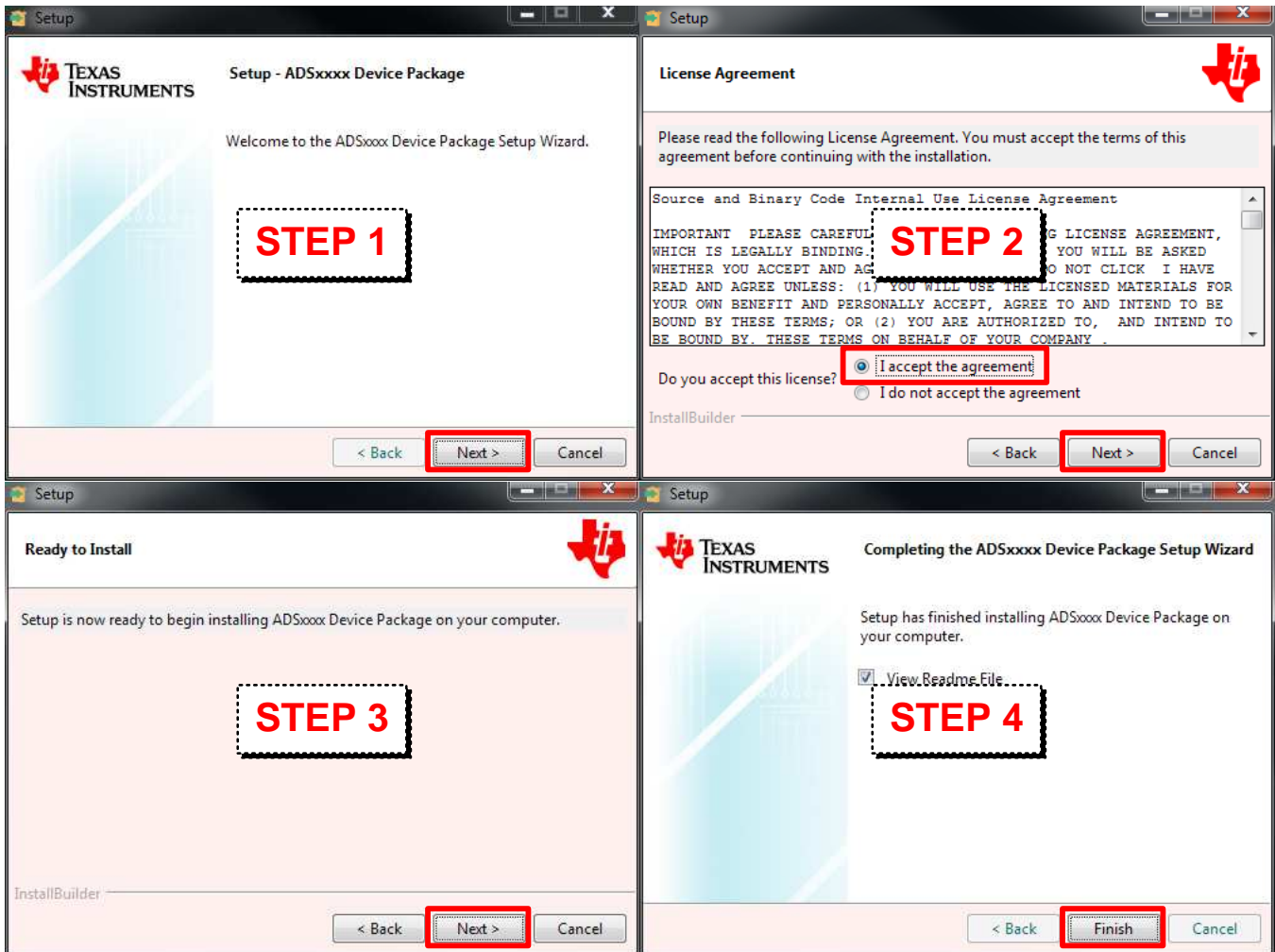


Figure 5. Device Package Installation Instructions

4.2 Connecting to the EVM Hardware

After the *Delta-Sigma ADC Evaluation Software* and the *ADS125H02 Device Package* is installed, connect the hardware with the provided USB micro cable and connect the high-voltage supplies to J4 (if the onboard high-voltage supply is not installed). Start the *Delta-Sigma ADC Evaluation Software*. The GUI automatically detects the connected hardware and displays the device register map under the *Device* tab as [Figure 6](#) and [Figure 7](#) show.

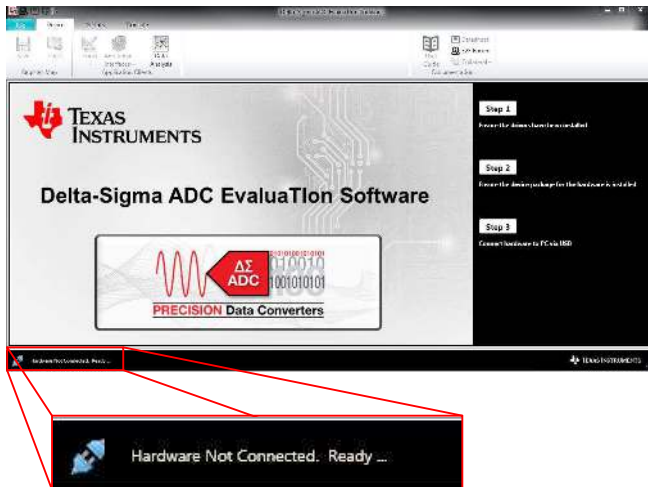


Figure 6. GUI View Before Connecting

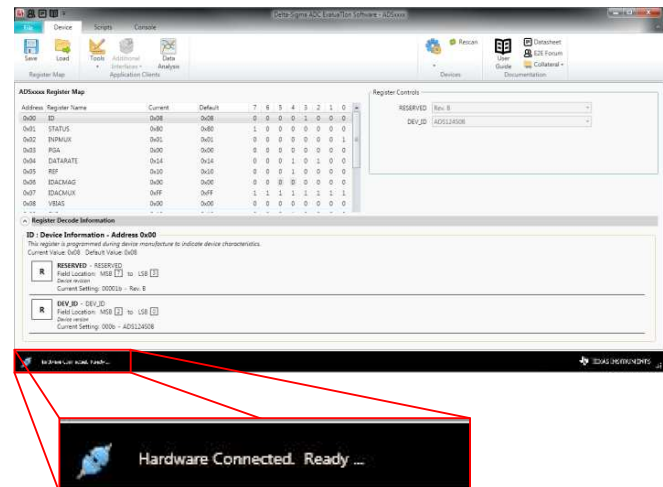


Figure 7. GUI View After Connecting EVM

4.3 Using the Software With the EVM

The *Delta-Sigma ADC Evaluation Software User Manual* provides an overview of the GUI, an explanation of how to modify device register settings, how to collect and analyze data, and control device operations with scripts. For a list of commands that are supported on the ADS125H02 EVM, see [Section 4.3.4](#).

4.3.1 Powering Up the EVM

When the EVM is powered up, the software start up must allow the GUI to identify the device and post the register map. However, if the EVM fails to recognize the device, the register map is not read out by the device. The device table appears as an empty register map, as shown in Figure 8. Verify that the device is unrecognized by checking the Console tab to see that the USB is connected to an unrecognized device, as shown in Figure 9 and Figure 9.



Figure 8. Empty Register Map for an Unrecognized Device

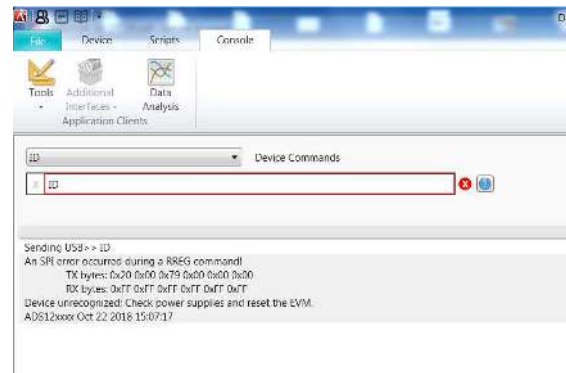


Figure 9. Console Tab View of an Unrecognized Device

Verify that the ADS125H02EVM is properly connected to the USB port. Then check the connection to the high-voltage supplies at J4, and the position of switch S2. If the EVM is fully powered up, press the RESET button at the lower left corner of the EVM, next to the USB cable connection.

4.3.2 ADS125H02EVM Configuration

When the ADS125H02EVM is correctly powered up, the software recognizes the device. The register map must be configurable in the GUI as shown in Figure 10.

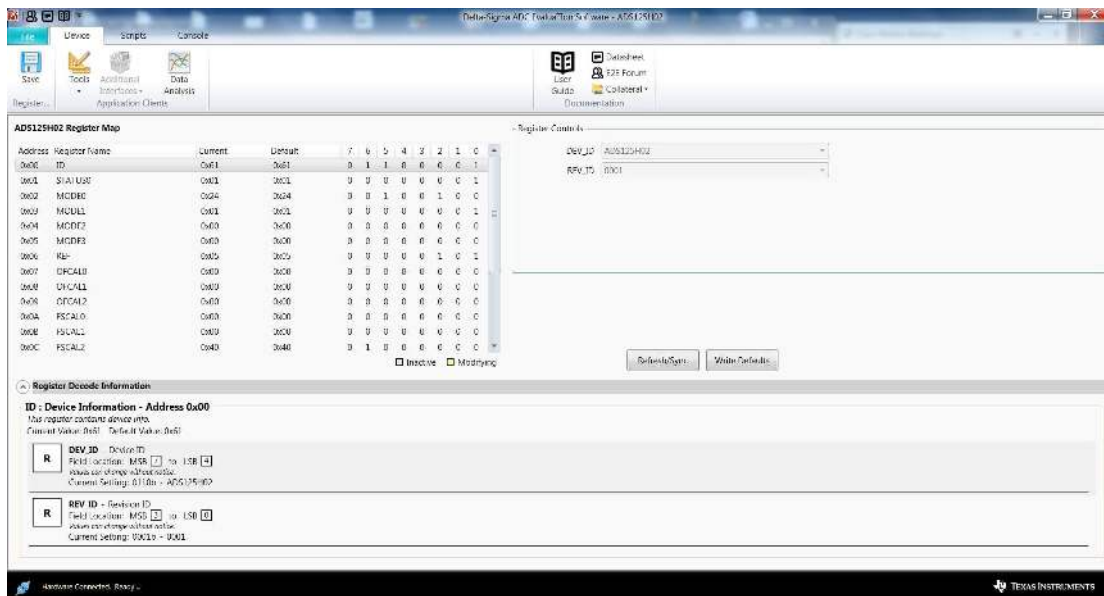


Figure 10. Register Map for the ADS125H02

The ADS125H02 can be configured through the register map as well as through commands through the Console tab as described in Section 4.3.4.

4.3.3 ADS125H02 Data Analysis Window

The *Delta-Sigma ADC Evaluation Software* collects data from the EVM with the *Data Analysis* window. Clicking on the *Data Analysis* icon opens up the analysis engine of the software. This window is shown in [Figure 11](#).

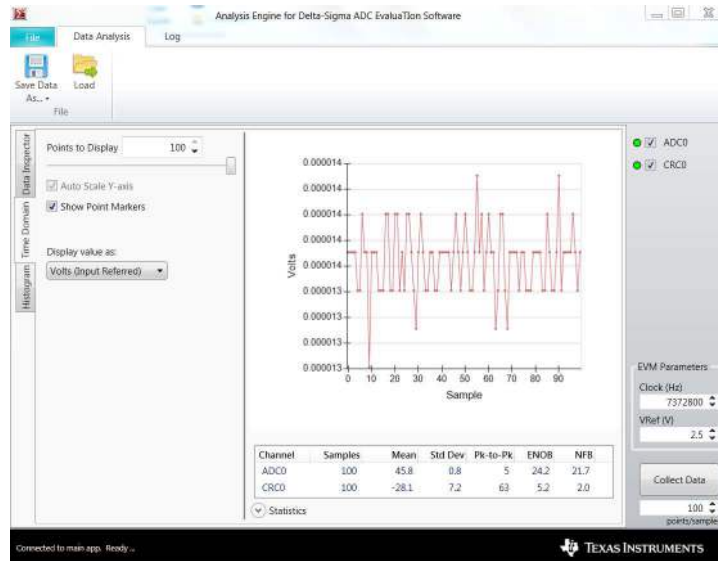


Figure 11. Data Analysis Window

Here are several helpful hints to collecting data with the *Data Analysis* window:

- It is convenient to set the *points/sample* size in the lower left corner of the *Data Analysis* window to a lower value. The default sample size is 2048, while the default data rate for the ADS125H02 is 20 SPS. Collecting that amount of data takes over 100 seconds.
- When the *Data Analysis* window plots voltage, ensure that the reference voltage is set to the correct value. The default setting for the reference is set to AVDD to AVSS and the reference is set to 5 V, instead of the 2.5-V reference default setting in the window.
- The voltage values for PGA gains below 1 V/V (0.125, 0.1875, 0.25, and 0.5) cannot be processed in the *Data Analysis* window. The actual output voltage shown in the plot is smaller by a factor of the gain. If the display plots the output ADC code, the code is correct.

The *Data Analysis* window collects and plots the ADC data. To start, click on the *Collect Data* button at the lower right. For more information about the *Data Analysis* window or the EVM software, consult the [Delta-Sigma ADC Evaluation Software User Manual](#).

4.3.4 ADS125H02 EVM Commands

The EVM commands are given in [Table 8](#). These commands are available for use within the *Scripts* and *Console* tabs of the Delta-Sigma ADC Evaluation software. Many of these commands are SPI commands that are defined in the device data sheet. All other command functions are provided by the EVM firmware.

In general, most device commands that communicate with the ADC via SPI require the $\overline{\text{PWDN}}$ pin to be set high, prior to issuing the command. When the $\overline{\text{PWDN}}$ pin is low, the device is in hardware power-down mode and all device functions are disabled (only the internal LDO remains powered). Returning the $\overline{\text{PWDN}}$ pin resumes normal ADC operations and preserves the registers settings.

The ADC may also be placed into a software power-down mode by setting the PWDN bit high, in the MODE3 register. In this mode the internal LDO, internal reference, and serial interface remain enabled. SPI commands can be sent while the device is in software power-down mode; however, these actions may or may not take effect in this mode.

Some of the commands listed in [Table 8](#) may wake the ADC prior to taking effect, particularly for EVM commands that are used by the GUI. See the *Wakes Device?* column in [Table 8](#) to determine the intended behavior of the EVM firmware.

Table 8. ADS125H02 EVM Software Commands

Command	Command Arguments	Description	Wakes Device?
ID		Returns EVM ID string: "<DEVICE> <DATE> <TIME>", where "<DEVICE>" is "ADS125H02", and "<DATE> <TIME>" indicates when the EVM firmware was compiled.	N
COMMANDLIST		Returns a list of all commands supported by the EVM firmware.	N
COLLECT	<# Samples>	Collects a number of ADC samples equal to "<# Samples>", where "<# Samples>" is an unsigned integer. During this operation, all other commands are ignored and the BUSY LED blinks until all samples have been collected.	Y ⁽¹⁾
REGMAP		This command is used by the GUI to read the values of all registers.	Y ⁽¹⁾
NOP		Issues the NOP device command to the ADC (via SPI).	N
RESET		Issues the RESET device command to the ADC (via SPI).	N ⁽²⁾
START		Sets the START pin low and issues the START device command to the ADC (via SPI).	N
STOP		Sets the START pin low and issues the STOP device command to the ADC (via SPI).	N
RDATA		Starts a single conversion, waits for \overline{DRDY} to go low, and prints the conversion result to the console.	N
OFSCAL		Issues the offset calibration device command to the ADC (via SPI).	N
GANCAL		Issues the gain calibration device command to the ADC (via SPI).	N
RREG	<ADDRESS>	Issues a read register device command to the ADC (via SPI), where "<ADDRESS>" is the starting register address in hexadecimal (without the "0x" prefix or "h" postfix).	N
READSINGLE	<ADDRESS>	This command is used by the GUI. This command provides the same function as RREG, but wakes the device from power down and returns to previous power-down mode after completion.	Y ⁽¹⁾
HOLDLOCK	<"0" or "1">	This command disables the Tiva GPIO output connected to "EXT CLK" to allow for external clocks to be applied to J5. Refer to Section 3.2.3 .	N
WREG	<ADDRESS> <DATA>	Issues a write register device command to the ADC (via SPI), where "<ADDRESS>" is the starting register address in hex, and "<DATA>" is the value to write to the register in hex (without the "0x" prefix or "h" postfix).	N
WRITESINGLE	<ADDRESS> <DATA>	This command is used by the GUI. This command provides the same function as WREG, but wakes the device from power down and returns to previous power-down mode after completion.	Y ⁽¹⁾
LOCK		Sends the lock register device command to the ADC (via SPI). While in this mode, all write register commands are ignored until the device is unlocked.	N
UNLOCK		Sends the unlock register device command to the ADC (via SPI). This command unlocks the device register to allow write commands to take effect.	N
HOLDSTART	<"0" or "1">	This command controls the state of the START GPIO pin. An argument of "1" sets the START pin high, while a "0" argument sets the START pin low.	N
HWRESET		This command toggles the \overline{RESET} GPIO pin.	N ⁽²⁾
CLEAR		Clears the software fault flag, writes "0x00" to the STATS register (to clear the CRC_ERR and RESET bits), and turns off the FAULT LED. NOTE: Pressing S3 performs the same action as the CLEAR command.	N
STATUS		Reads the STATUS register (to check for any new fault conditions) and prints (to the console) a description of each fault type that has occurred since last clearing the software fault flag (with S3 or the CLEAR command).	N
CRC	<LENGTH> <DATA1> <DATA2> <DATA3> <DATA4>	Computes the CRC-n of the data bytes given in "<DATA1>" through "<DATA4>", where "<LENGTH>" is the number of bytes to be used in the CRC-n calculation. If the number of data bytes provided is greater than "<LENGTH>", the extra data bytes are ignored.	N
DONTCARE	<VALUE>	Sets the "Don't care" byte value that is used for all SPI commands that include a "Don't care" byte. Changing the value of this byte only has the effect of modifying the resulting CRC byte that is used with CRC-mode.	N
SPISEND	<LENGTH> <BYTE1> <BYTE2> ...	Sends a user-specified SPI command sequence to the ADC. \overline{CS} remains low until all bytes have been sent. After issuing this command the firmware reads the STATUS register to check for any CRC errors. This command allows for testing of the CRC command validation of the ADC, for example, because this command allows the user to provide invalid CRC bytes with the various SPI commands.	N

⁽¹⁾ Returns device to previous state after completion.

⁽²⁾ Resetting wakes the device from software-power down mode.

5 EVM Bill of Materials, PCB Layouts, and Schematics

The bill of materials and schematics are shown for the ADS125H02EVM.

5.1 Bill of Materials

NOTE: All components should be compliant with the *European Union Restriction on Use of Hazardous Substances* (RoHS) directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see www.ti.com.)

Table 9. EVM Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC045	Any
C1, C2, C4, C5, C7, C8	6	1000pF	CAP, CERM, 1000 pF, 50 V, ±10%, C0G/NP0, 0603	0603	06035A102KAT2A	AVX
C3, C6, C9, C10	4	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H103JA01D	MuRata
C11, C12	2	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	C1608X7R1H104K080AA	TDK
C16, C18, C21, C23, C51, C62, C65, C67, C69, C71	10	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	0603	UMK107AB7105KA-T	Taiyo Yuden
C17, C19, C26, C27, C28, C29, C30, C33, C34, C35, C36, C39, C40, C45, C46, C47, C48, C49, C52, C54, C55, C56, C57, C63, C68	25	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603	06033C104JAT2A	AVX
C20, C25, C76	3	0.1uF	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCJ188R72A104KA01D	MuRata
C22	1	4700pF	CAP, CERM, 4700 pF, 100 V, +/- 5%, C0G/NP0, 0603	0603	C0603C472J1GAC7867	Kemet
C24	1	10uF	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805	0603	GRM21BR71A106KE51L	MuRata
C41, C42	2	6.8pF	CAP, CERM, 6.8 pF, 50 V, +/- 4%, C0G/NP0, 0603	0603	06035A6R8CAT2A	AVX
C43, C44	2	12pF	CAP, CERM, 12 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C120J5GACTU	Kemet
C50, C53	2	2.2uF	CAP, CERM, 2.2 uF, 35 V, +/- 10%, X5R, 0603	0603	GRM188R6YA225KA12D	MuRata
C58	1	4.7uF	CAP, CERM, 4.7 uF, 50 V, +/- 10%, X7R, 1206	1206	GRM31CR71H475KA12L	MuRata
C59	1	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C101J5GACTU	Kemet
C60	1	22uF	CAP, CERM, 22 uF, 16 V, +/- 10%, X7R, 1210	1210	GRM32ER71C226KE18L	Murata
C61	1	10uF	CAP, CERM, 10 uF, 35 V, +/- 10%, X7R, 1206	1206	GMK316AB7106KL	Taiyo Yuden
C64	1	47uF	CAP, CERM, 47 uF, 10 V, +/- 20%, X5R, 1206	1206	C3216X5R1A476M160AB	TDK
C66, C70	2	1000pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603	0603	06031C102JAT2A	AVX
C77, C78, C80, C81	4	10uF	CAP, CERM, 10 uF, 50 V, +/- 10%, X5R, 1206	1206	GRM31CR61H106KA12L	Murata
D1	1	Orange	LED, Orange, SMD	LED_0603	LTST-C191KFKT	Lite-On
D2, D3, D5	3	Green	LED, Green, SMD	LED_0603	LTST-C191TGKT	Lite-On
D4	1	Red	LED, Red, SMD	LED_0603	LTST-C191KRKT	Lite-On

Table 9. EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
D8, D9	2		Diode, Schottky, 80 V, 0.5 A, SOD-123	SOD-123	MBR0580-TP	Micro Commercial Components
H1, H2, H3, H4	4		Bump, Cylindrical, 0.312 X 0.200, Black	Black Bump	SJ61A1	3M
J1	1		Terminal Block, 3.5mm, 9x1, R/A, TH		ED555/9DS	On-Shore Technology
J2, J4	2		Terminal Block, 3.5mm Pitch, 3x1, TH		ED555/3DS	On-Shore Technology
J6	1		Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT		473460001	Molex
JP6	1		Header, 100mil, 3x1, Gold, TH		PBC03SAAN	Sullins Connector Solutions
JP7, JP8	2		Header, 100mil, 2x1, Gold, TH		TSW-102-07-G-S	Samtec
L1	1	1uH	Inductor, Wirewound, Ferrite, 1 uH, 2.05 A, 0.054 ohm, SMD	1210	LQH32PH1R0NN0L	Murata
R1, R2, R5, R7, R10, R12, R28, R29, R78, R81	11	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo America
R3, R4, R6, R8, R11, R13, R15, R56, R58, R66	10	100	RES, 100, 1%, 0.1 W, 0603	0603	RC0603FR-07100RL	Yageo America
R30, R31, R32, R73	4	0.1	RES, 0.1, 1%, 0.1 W, 0603	0603	ERJ-L03KF10CV	Panasonic
R33, R39, R40, R41, R42, R43, R44, R45, R46	9	47	RES, 47, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060347R0JNEA	Vishay-Dale
R34, R35, R36, R37, R38, R48, R49, R74, R97	9	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo America
R47	1	1.69k	RES, 1.69 k, 1%, 0.1 W, 0603	0603	RC0603FR-071K69L	Yageo America
R51, R54, R55, R57, R67	5	10k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R52, R86	2	1k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R53	1	8.06k	RES, 8.06 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06038K06FKEA	Vishay-Dale
R61, R62, R63	3	2.94k	RES, 2.94 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K94L	Yageo America
R68	1	1.0Meg	RES, 1.0 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M00JNEA	Vishay-Dale
R70	1	4.87k	RES, 4.87 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034K87FKEA	Vishay-Dale
R71	1	2.00k	RES, 2.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06032K00FKEA	Vishay-Dale
R72	1	51	RES, 51, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060351R0JNEA	Vishay-Dale
R75	1	20.0k	RES, 20.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0720KL	Yageo America
R76	1	768k	RES, 768 k, 1%, 0.1 W, 0603	0603	RC0603FR-07768KL	Yageo America
R77	1	215k	RES, 215 k, 1%, 0.1 W, 0603	0603	RC0603FR-07215KL	Yageo America
R84, R85	2	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R91	1	10k	RES, 10 k, 5%, 0.1 W, 0603	0603	RC1608J103CS	Samsung Electro-Mechanics
R92	1	118k	RES, 118 k, 1%, 0.1 W, 0603	0603	RC0603FR-07118KL	Yageo America
R93	1	150k	RES, 150 k, 1%, 0.1 W, 0603	0603	RC0603FR-07150KL	Yageo America
R94, R95	2	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1002V	Panasonic
R96	1	499k	RES, 499 k, 1%, 0.1 W, 0603	0603	RC0603FR-07499KL	Yageo America

Table 9. EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
S1	1		SLIDE SWITCH DPDT .1A, SMT	SWITCH, 5.4x2.5x3.9mm	CAS-220TA	Copal Electronics
S2, S3, S5	3		Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	Switch, 4.4x2x2.9 mm	TL1015AF160QG	E-Switch
SH-1, SH-2	2	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
T1	1	475 uH	Transformer, 475 uH, SMT		760390015	Würth Elektronik
U3	1		+/- 15.5 V-Input, 3-Channel, 19.2-kSPS, 24-Bit, Delta-Sigma ADC With PGA and Voltage Reference, RHB0032E (VQFN-32)	VQFN-32	ADS125H02IRHBR	Texas Instruments
U4	1		Single Inverter Buffer/Driver With Open-Drain Output, DCK0005A	DCK0005A	SN74LVC1G06DCKT	Texas Instruments
U5, U6	2		8-Bit Bidirectional Voltage-Level Shifter For Open-Drain And Push-Pull Application, RGY0020A (VQFN-20)	RGY0020A	TXS0108ERGYR	Texas Instruments
U8	1		USB ESD Solution with Power Clamp, 4 Channels, -40 to +85 degC, 6-pin SON (DRY), Green (RoHS & no Sb/Br)	DRY0006A	TPD4S012DRYR	Texas Instruments
U9	1		High-Speed USB 2.0 (480 Mbps) 1:2 Multiplexer / Demultiplexer Switch with Single Enable, 6 ohm RON, 2.5 to 3.3V, -40 to 85 degC, 10-Pin UQFN (RSE), Green (RoHS & no Sb/Br)	RSE0010A	TS3USB221ERSE	Texas Instruments
U10	1		Highly Integrated Full Featured Hi-Speed USB 2.0 ULPI Transceiver, QFN-32	5x5 QFN-32	USB3320C-EZK	Microchip
U12	1		Triple Inverter Buffer/Driver with Open-Drain Output, DCU0008A, SMALL T&R	DCU0008A	SN74LVC3G06DCUT	Texas Instruments
U13	1		Tiva C Series Microcontroller, 1024 KB Flash, 256 KB SRAM, 12 Bit, 20 Channels, -40 to 85 degC, 128-Pin TQFP (PDT), Green (RoHS & no Sb/Br), Tape and Reel	PDT0128A	TM4C1294NCPDTI3R	Texas Instruments
U14	1		3.5MHz, 1.5A, 92% Efficient Boost Converter with Adjustable Input Current Limit, DSG0008A (WSON-8)	DSG0008A	TPS61252DSGR	Texas Instruments
U15	1		36-V, 1-A, 4.17-uVRMS, RF LDO Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4700RGWR	Texas Instruments
U16	1		Single Output High PSRR LDO, 150 mA, Fixed 1.8 V Output, 2.5 to 6.5 V Input, with Low IQ, 5-pin SC70 (DCK), -40 to 85 degC, Green (RoHS & no Sb/Br)	DCK0005A	TPS71718DCKR	Texas Instruments
U17	1		Voltage Supervisor with Active-Low, Open Drain Reset, 1 Supply Monitored, -40 to 125 degC, 3-pin SOT-23 (DBZ), Green (RoHS & no Sb/Br)	DBZ0003A	TLV803MDBZR	Texas Instruments
U18	1		Single Output LDO, 1A, Adj. (1.2 to 5.0V), Reverse Current Protection, DRV0006A (WSON-6)	DRV0006A	TPS73733DRVR	Texas Instruments
U22	1		Low-Noise 1 A, 420 kHz Transformer Driver, DBV0006A (SOT-23-6)	DBV0006A	SN6505BDBVR	Texas Instruments
U23	1		Wide-VIN (+/-33 V), 150-mA, Split-Rail Output, Positive and Negative LDO Voltage Regulator with Startup Tracking, DSC0010J (WSON-10)	DSC0010J	TPS7A3901DSCR	Texas Instruments
Y1	1		Crystal, 25 MHz, 18 pF, SMD	ABM3	ABM3-25.000MHZ-D2Y-T	Abracon Corporation
Y2	1		CRYSTAL, 32.768KHz, 7PF, SMD	1.5x1.4x6.7mm	SSPT7F-7PF20-R	Seiko Instruments
C11, C12, C76	0	0.1uF	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, 0603	0603	GRM188R72A104KA35D	MuRata
C13	0	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, 0603	0603	GRM188R71A225KE15D	MuRata

Table 9. EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C14	0	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	0603	UMK107AB7105KA-T	Taiyo Yuden
C15	0	22uF	CAP, CERM, 22 uF, 10 V, +/- 10%, X7R, 1206	1206	LMK316AB7226KL-TR	Taiyo Yuden
C31, C32, C37, C38, C73	0	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603	06033C104JAT2A	AVX
C72, C74	0	10uF	CAP, CERM, 10 uF, 35 V, +/- 10%, X7R, 1206	1206	GMK316AB7106KL	Taiyo Yuden
C75	0	0.01uF	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E103KA01D	MuRata
D6	0		Diode, TVS, Uni, 12 V, 19.9 Vc, SMB	SMB	SMBJ12A-13-F	Diodes Inc.
D7	0	Green	LED, Green, SMD	LED_0603	LTST-C191TGKT	Lite-On
F1	0		Fuse, 2 A, 125VAC/VDC, SMD	SMD, 2-Leads, Body 9.73x5.03mm	0154002.DRT	Littelfuse
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H5	0		CABLE USB-A TO MICRO USB-B 1M	Used in PnP output and some BOM reports	102-1092-BL-00100	CNC Tech
J3	0		Terminal Block, 3.5mm, 9x1, R/A, TH		ED555/9DS	On-Shore Technology
J5	0		Header, 2.54 mm, 28x2, Gold, TH		TSW-128-07-S-D	Samtec
J7	0		Header, 100mil, 7x1, Gold, TH		TSW-107-07-G-S	Samtec
J8	0		Terminal Block, 3.5mm Pitch, 2x1, TH		ED555/2DS	On-Shore Technology
J9	0		Connector, DC Jack 2.1X5.5 mm, TH		PJ-102A	CUI Inc
JP1, JP2, JP5	0		Header, 100mil, 2x1, Gold, TH		TSW-102-07-G-S	Samtec
JP3, JP4	0		Header, 100mil, 3x1, Gold, SMT		TSM-103-01-L-SV	Samtec
R9, R14, R60	0	100	RES, 100, 1%, 0.1 W, 0603	0603	RC0603FR-07100RL	Yageo America
R16, R17, R18, R22, R23, R24, R26, R27, R79, R80, R82, R83, R98, R99	0	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo America
R19, R20, R21	0	10k	RES, 10 k, 5%, 0.1 W, 0603	0603	RC1608J103CS	Samsung Electro-Mechanics
R25	0	0.005	RES, 0.005, 1%, 0.25 W, 1206	1206	WSL12065L000FEA	Vishay-Dale
R50, R97	0	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo America
R59, R64, R65, R87	0	10k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R88	0	9.31k	RES, 9.31 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06039K31FKEA	Vishay-Dale
R89	0	3.01k	RES, 3.01 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06033K01FKEA	Vishay-Dale
R90	0	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R100, R101	0	47	RES, 47, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEYJ470V	Panasonic
S4	0		Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	Switch, 4.4x2x2.9 mm	TL1015AF160QG	E-Switch
TP11, TP26, TP27, TP28	0		Terminal, Turret, TH, Double	Keystone1573-2	1573-2	Keystone
U1	0		MUX36xxx 36-V, Low-Capacitance, Low-Leakage-Current, Precision, Analog Multiplexers, PW0016A (TSSOP-16)	TSSOP-16	MUX36D04IPWR	Texas Instruments
U2	0		High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	VSSOP-8	REF6225IDGKR	Texas Instruments

Table 9. EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
U7	0		8-Bit Bidirectional Voltage-Level Shifter For Open-Drain And Push-Pull Application, RGY0020A (VQFN-20)	RGY0020A	TXS0108ERGYR	Texas Instruments
U11	0		256K I2C™ CMOS Serial EEPROM, TSSOP-8	TSSOP-8	24AA256-I/ST	Microchip
U19	0		Single Output Fast Transient Response LDO, 1.5 A, Adjustable 1.21 to 20 V Output, 2.1 to 20 V Input, 6-pin SOT-223 (DCQ), -40 to 125 degC, Green (RoHS & no Sb/Br)	DCQ0006A	TL1963ADCQR	Texas Instruments
U20	0		3-Pin Supply Voltage Supervisors for Automotive, DBV0003A (SOT-23-3)	DBV0003A	TPS3809I50QDBVRQ1	Texas Instruments
U21	0		Single Inverter Buffer/Driver With Open-Drain Output, DCK0005A	DCK0005A	SN74LVC1G06DCKT	Texas Instruments
U24	0		Single Buffer/Driver With Open-Drain Output, DBV0005A (SOT-23-5)	DBV0005A	SN74LVC1G07DBVT	Texas Instruments

5.2 PCB Layouts

Figure 12 through Figure 17 illustrate the PCB layout.

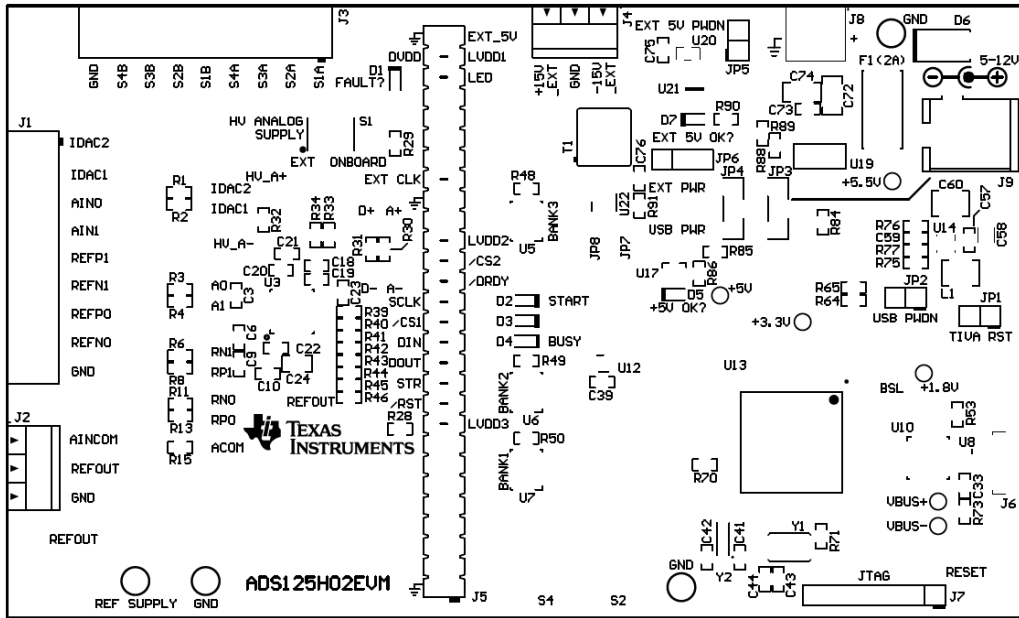


Figure 12. Top Silkscreen

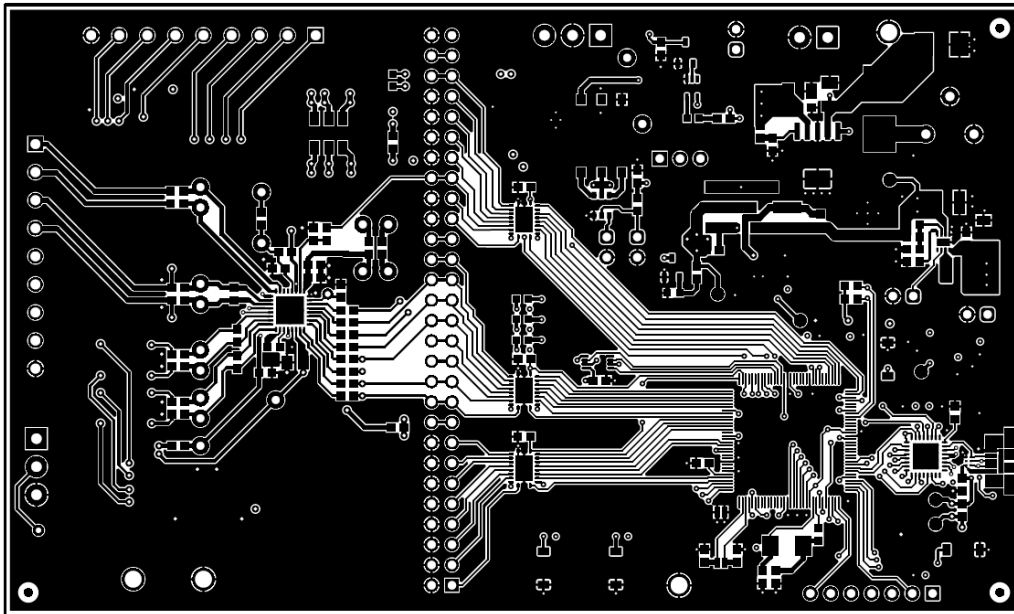


Figure 13. Top Layer (Positive)

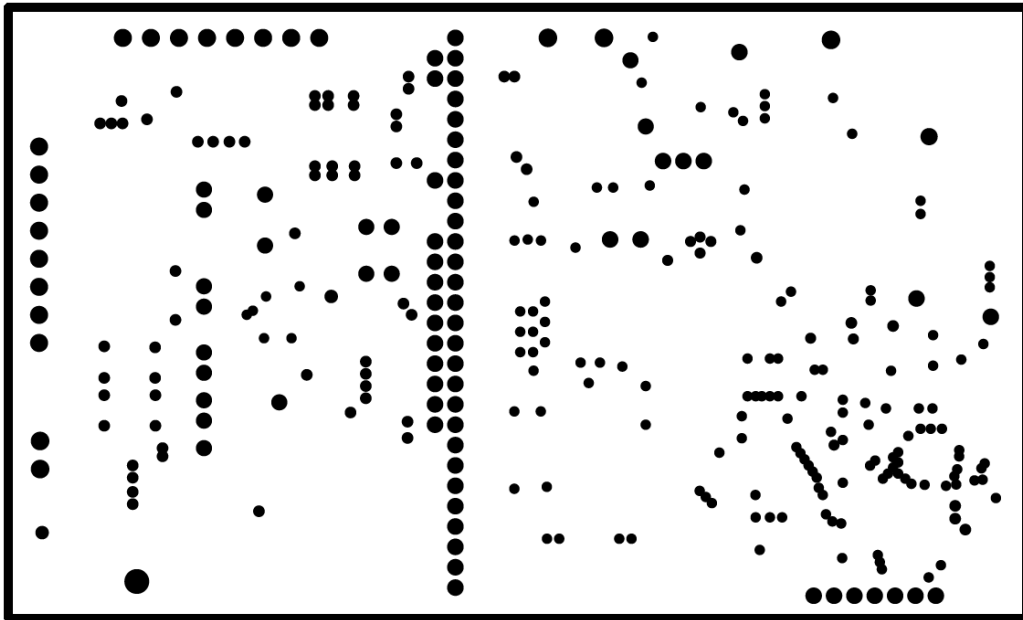


Figure 14. Ground Layer (Negative)

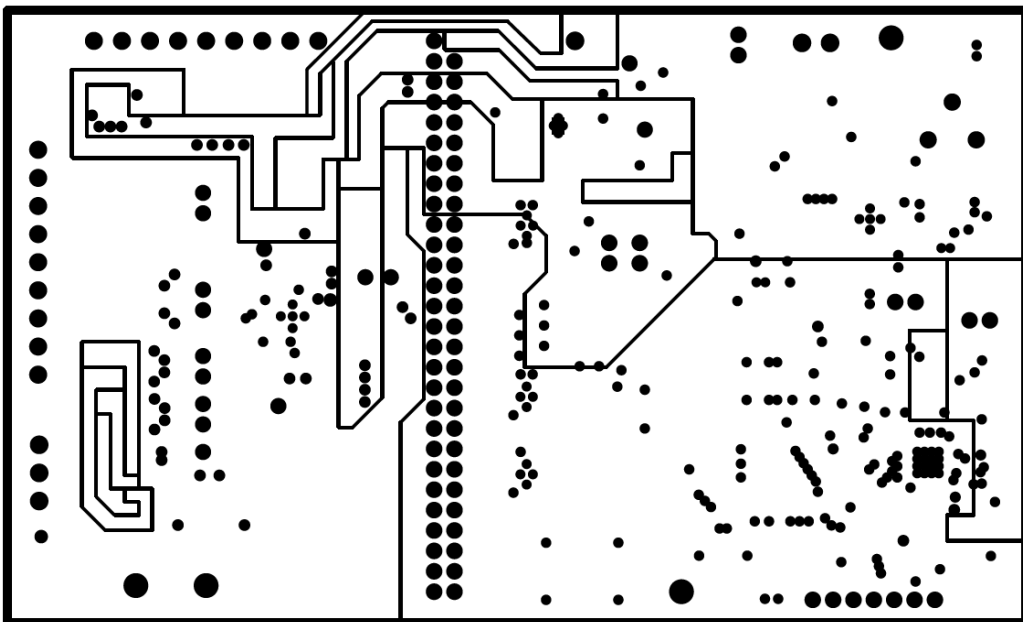


Figure 15. Power Layer (Negative)

5.3 Schematic

Figure 18 through Figure 25 illustrate the ADS125H02EVM schematics.

Schematic Block Diagram

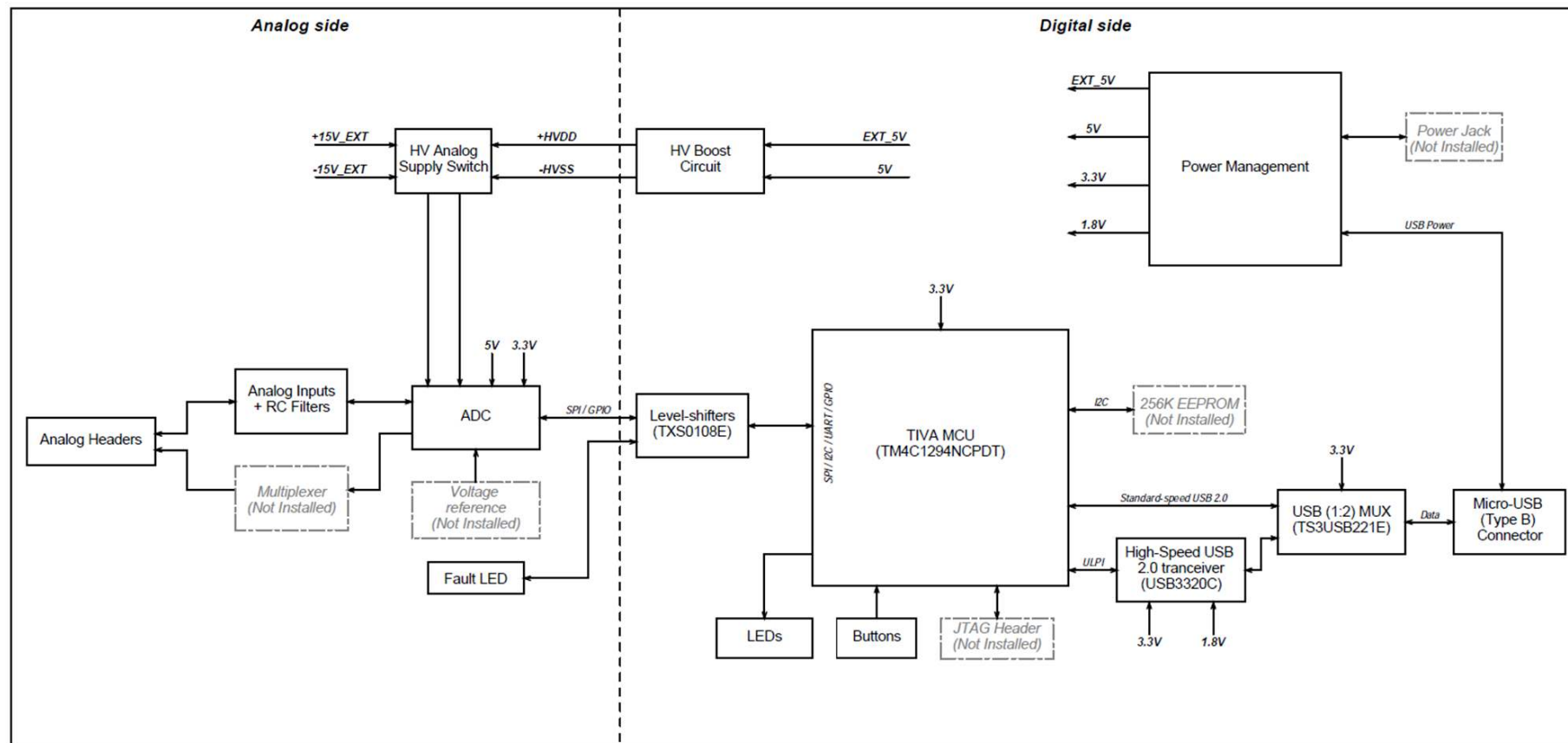


Figure 18. ADS125H02EVM Block Diagram Schematic

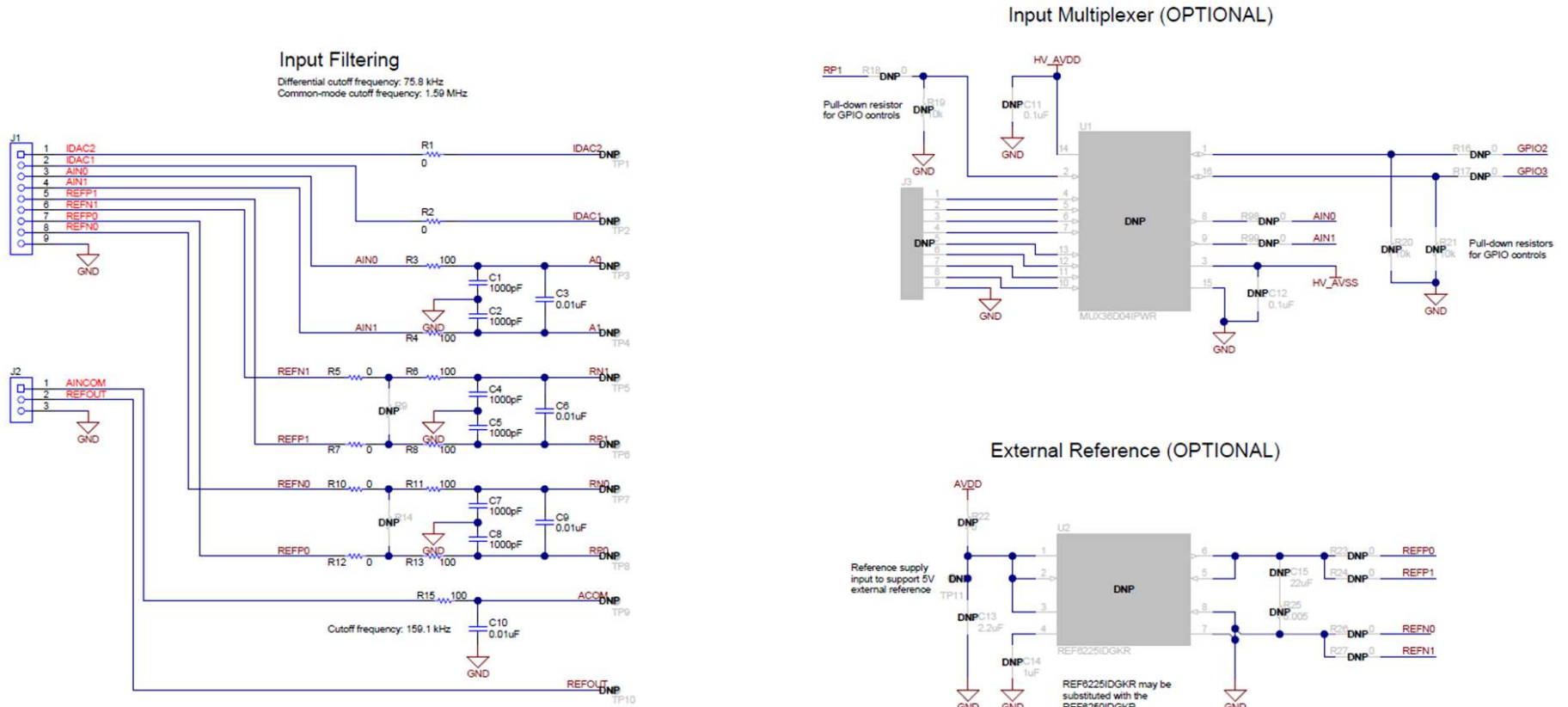


Figure 19. ADS125H02EVM Analog Inputs Header Schematic

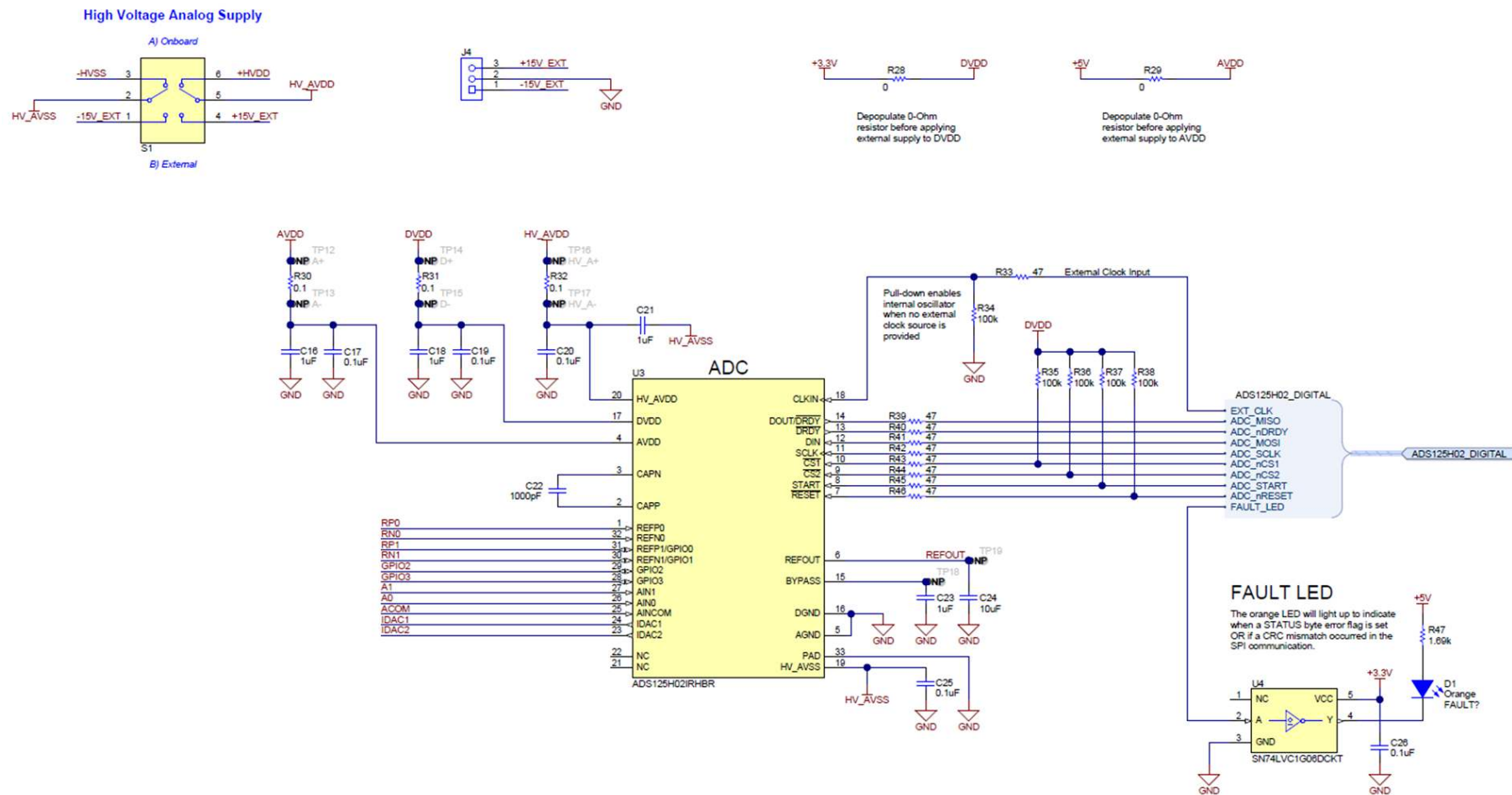


Figure 20. ADS125H02EVM ADC Main Schematic

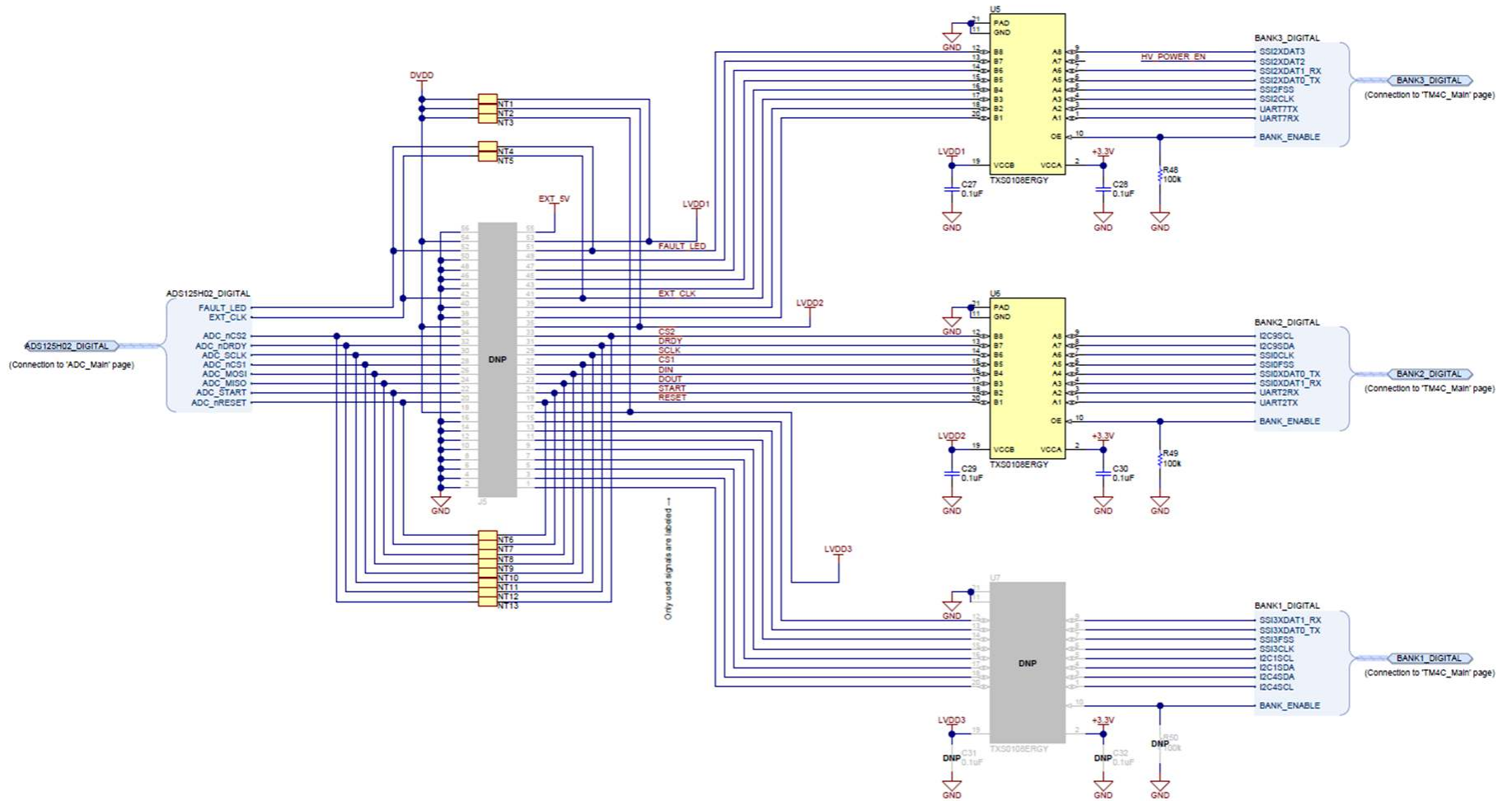


Figure 21. ADS125H02EVM Digital Header Schematic

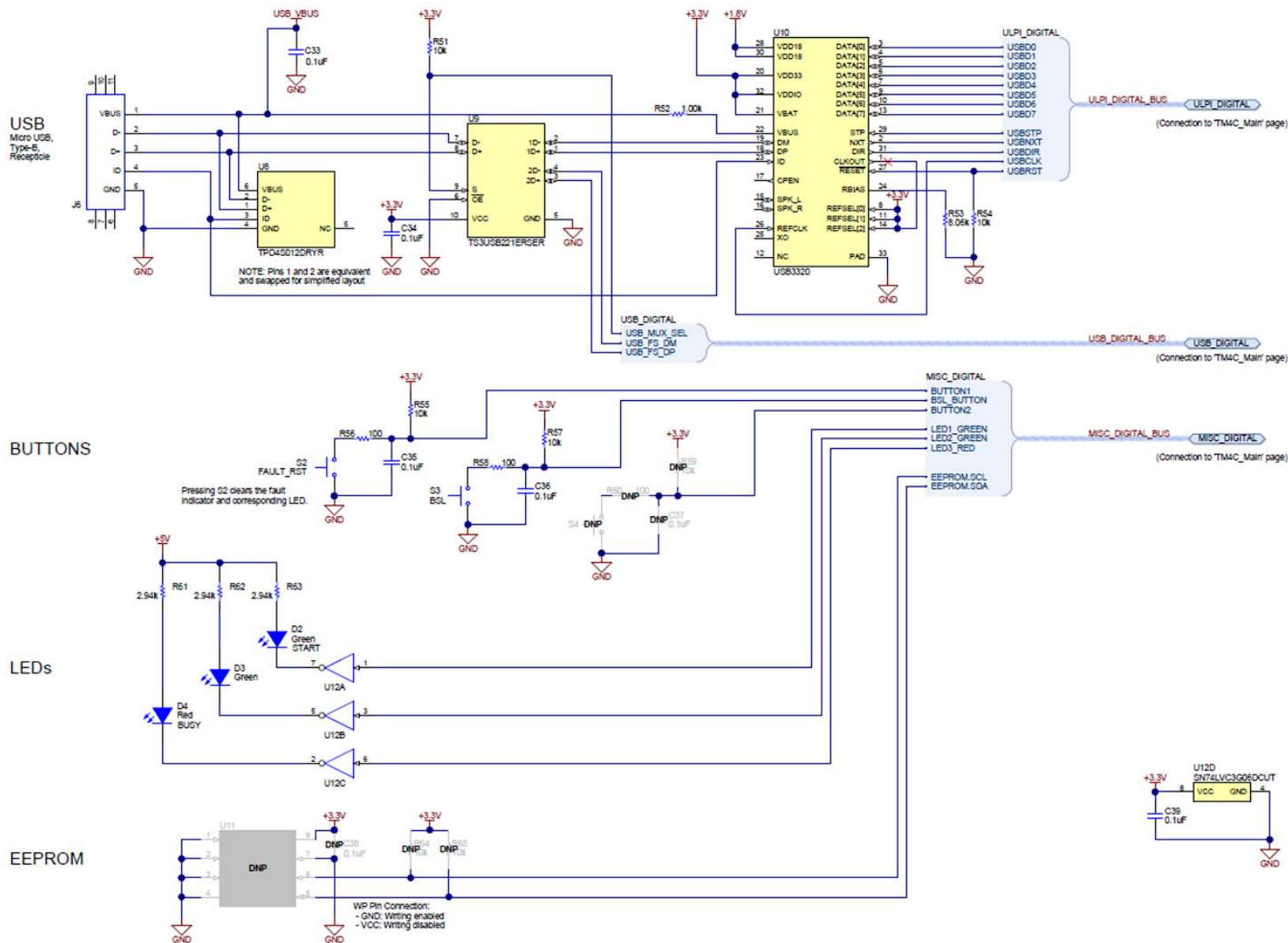


Figure 22. ADS125H02EVM USB and Peripherals Schematic

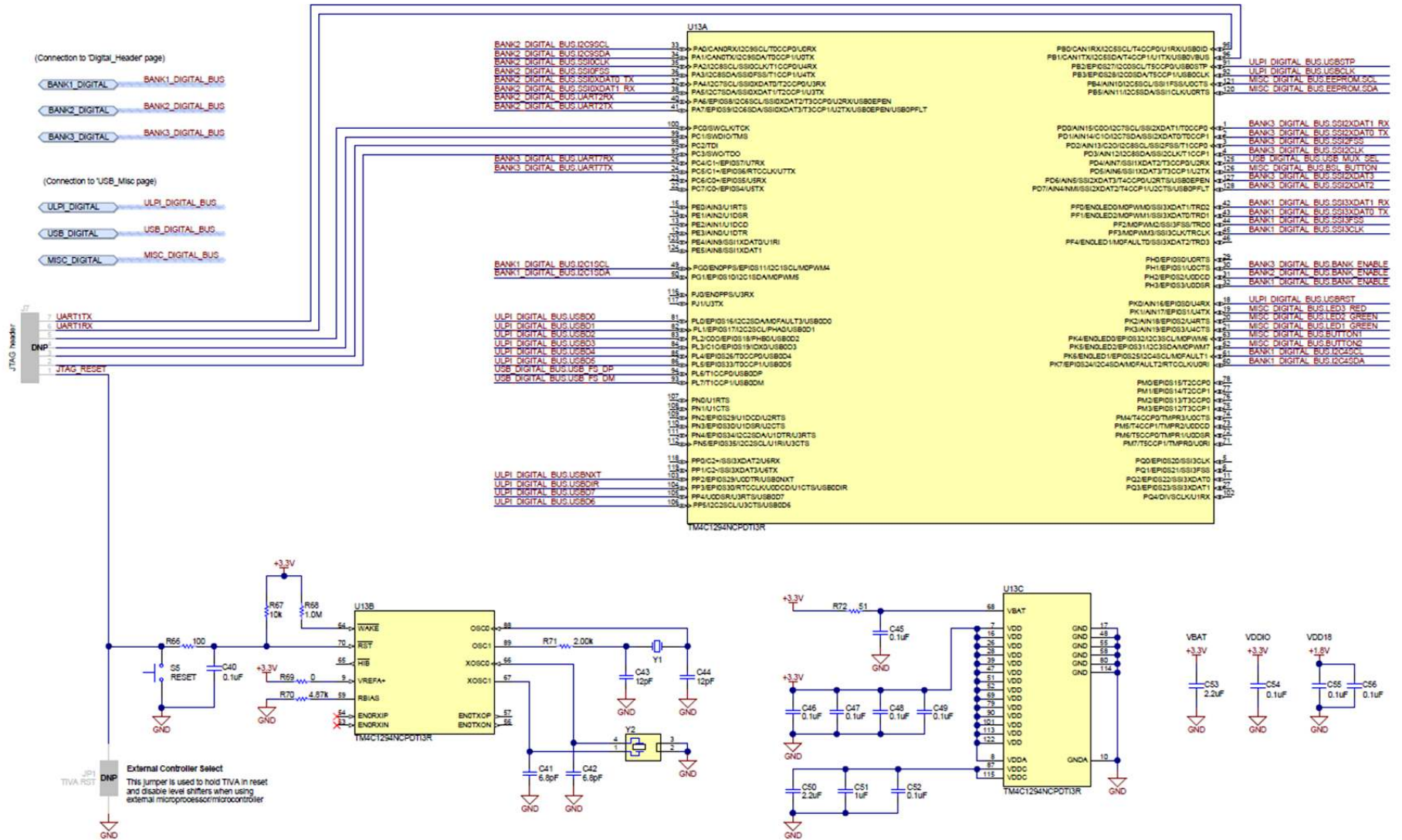


Figure 23. ADS125H02EVM Processor Main Schematic

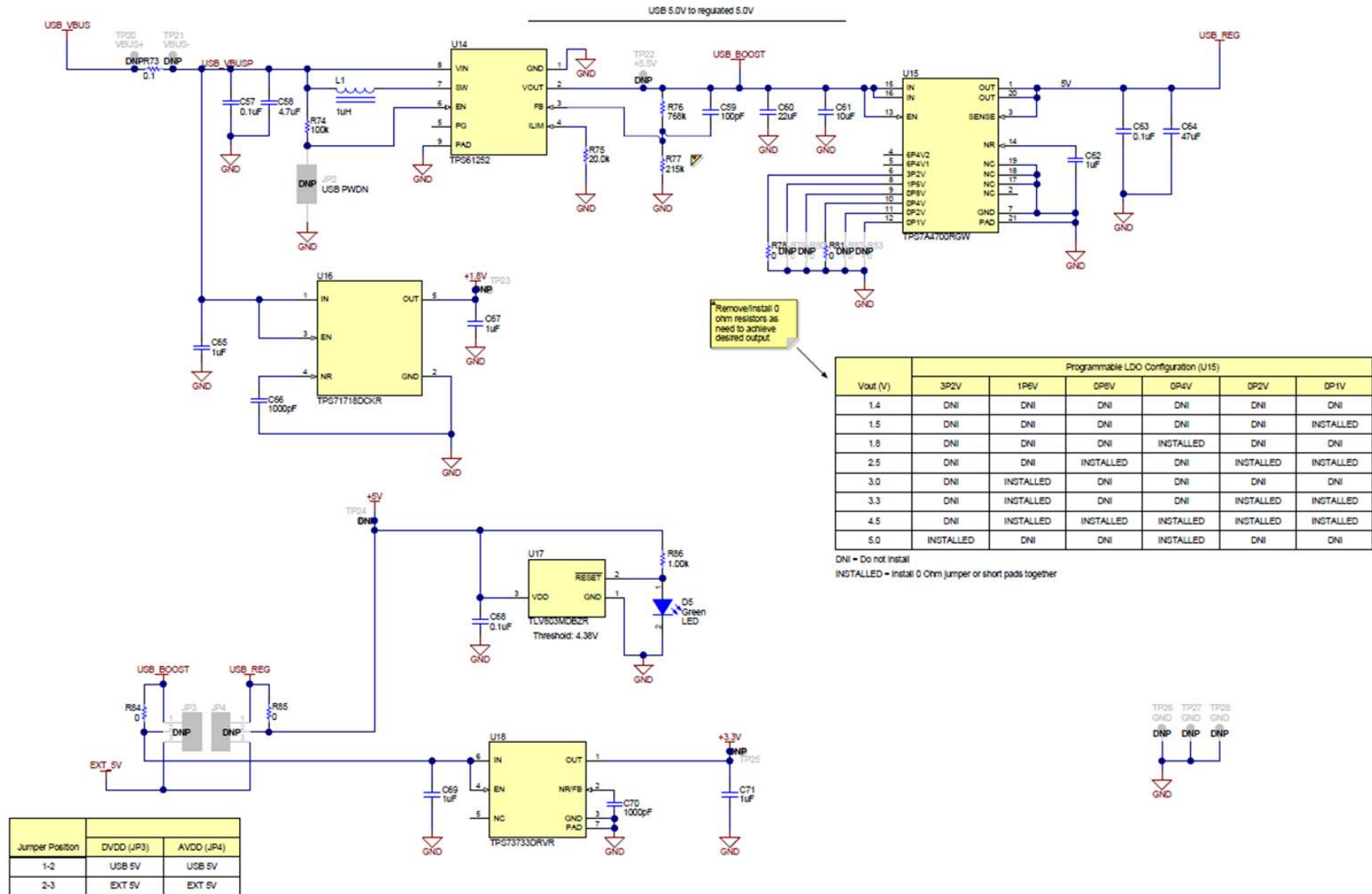


Figure 24. ADS125H02EVM USB Power Schematic

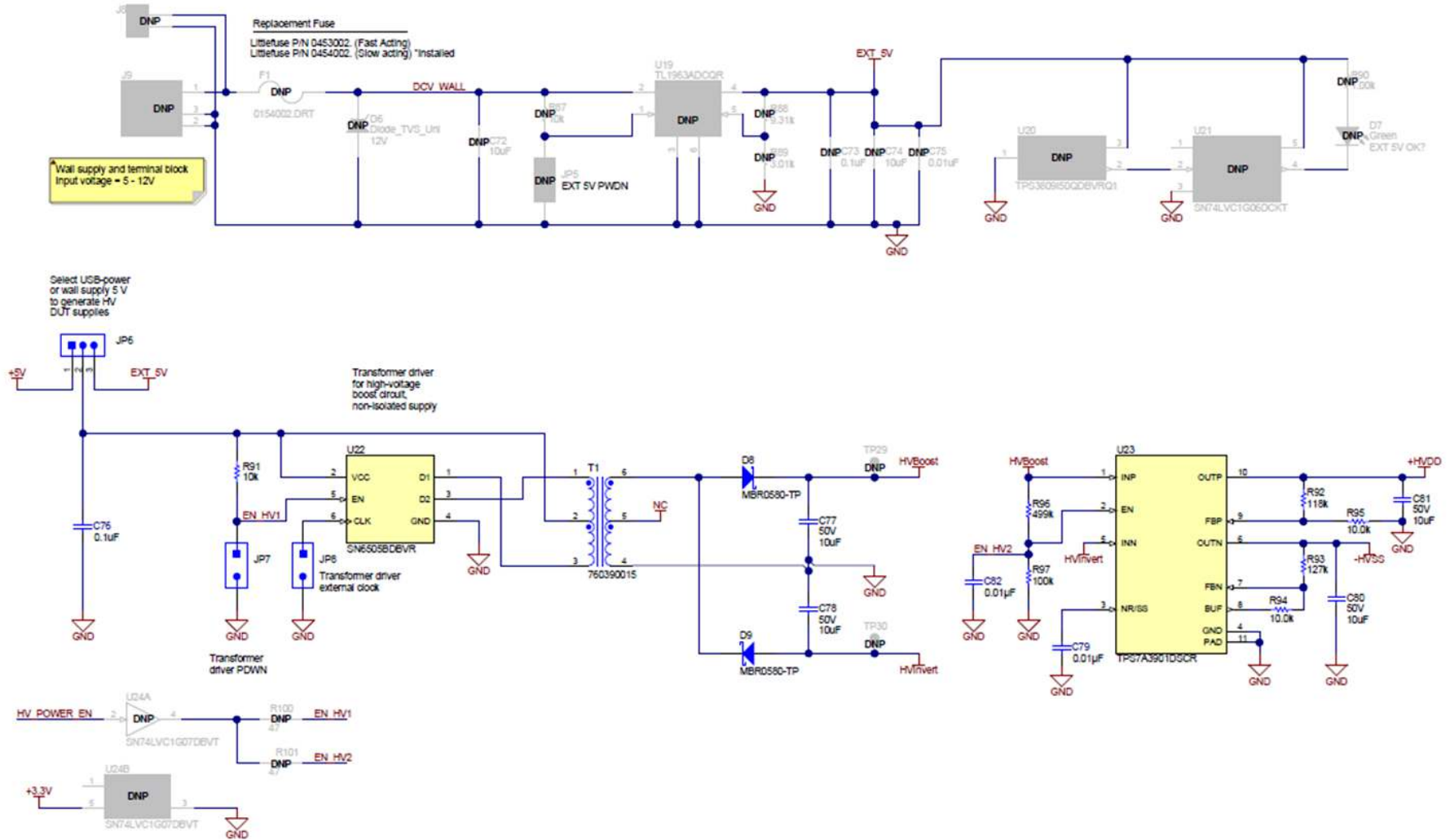


Figure 25. ADS125H02EVM External Power Schematic

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2018) to A Revision	Page
• Changed EVM figures throughout the document	1
• Added text references for all figures throughout document.....	1
• Changed <i>Power Supply</i> section	3
• Deleted (<i>not installed</i>) from third bullet in <i>Hardware Functionality</i> section	3
• Changed JP5 to JP8 rows in <i>Default Settings</i> table	4
• Changed main <i>Powering the EVM</i> section.....	4
• Changed <i>High-Voltage Analog Supply Configuration of the ADC</i> section	5
• Changed JP6, JP7, and JP8 rows in <i>Jumper and Switch Options</i> table.....	6
• Changed last two columns in pins 3 to 8 rows of <i>Analog Input Terminal Blocks, J1–J3</i> table.....	8
• Changed first sentence of <i>High-Voltage Supply Terminal</i> section.....	9
• Deleted high voltage linear regulator rows from <i>Test Points</i> table	11
• Changed first sentence of <i>Powering Up the EVM</i> section	15
• Changed <i>EVM Bill of Materials</i> table	18
• Added <i>Header</i> to <i>ADS125H02EVM Analog Inputs Header Schematic</i> title.....	27

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