ISL81805EVAL3Z

The ISL81805EVAL3Z dual-output evaluation board, with negative-to-positive voltage conversion (shown in Figure 4) features the ISL81805, which is an 80V high voltage, dual synchronous boost controller that offers external soft-start and independent enable functions and integrates UV/OV/OC/OT protection. A programmable switching frequency ranging from 100kHz to 1MHz helps optimize the inductor size as the strong gate driver delivers up to 20A for each output.

Specifications

The ISL81805EVAL3Z dual-output evaluation board is designed for negative-to-positive voltage conversion and high output voltage applications. The current rating of the ISL81805EVAL3Z is limited by the FETs and inductor selection. The ISL81805EVAL3Z electrical ratings are shown in Table 1.

Table 1. ISL81805EVAL3Z Electrical Ratings

Parameter	Rating
Input Voltage	-36V to -60V
Switching Frequency	200kHz
Output Voltage 1	12V
Output Current 1	20A
Output Voltage 2	5V
Output Current 2	20A
OCP Set Point (input average)	Minimum 8A for 12V output, 3.3A for 5V output at ambient room temperature

Features

- Negative-to-positive voltage conversion
- Wide input range: -36V to -60V
- Programmable soft-start
- Optional DEM/PWM operation
- Optional input/output constant current OCP protection
- Supports pre-bias output with soft-start
- PGOOD indicator
- OVP, OTP, and UVP protection

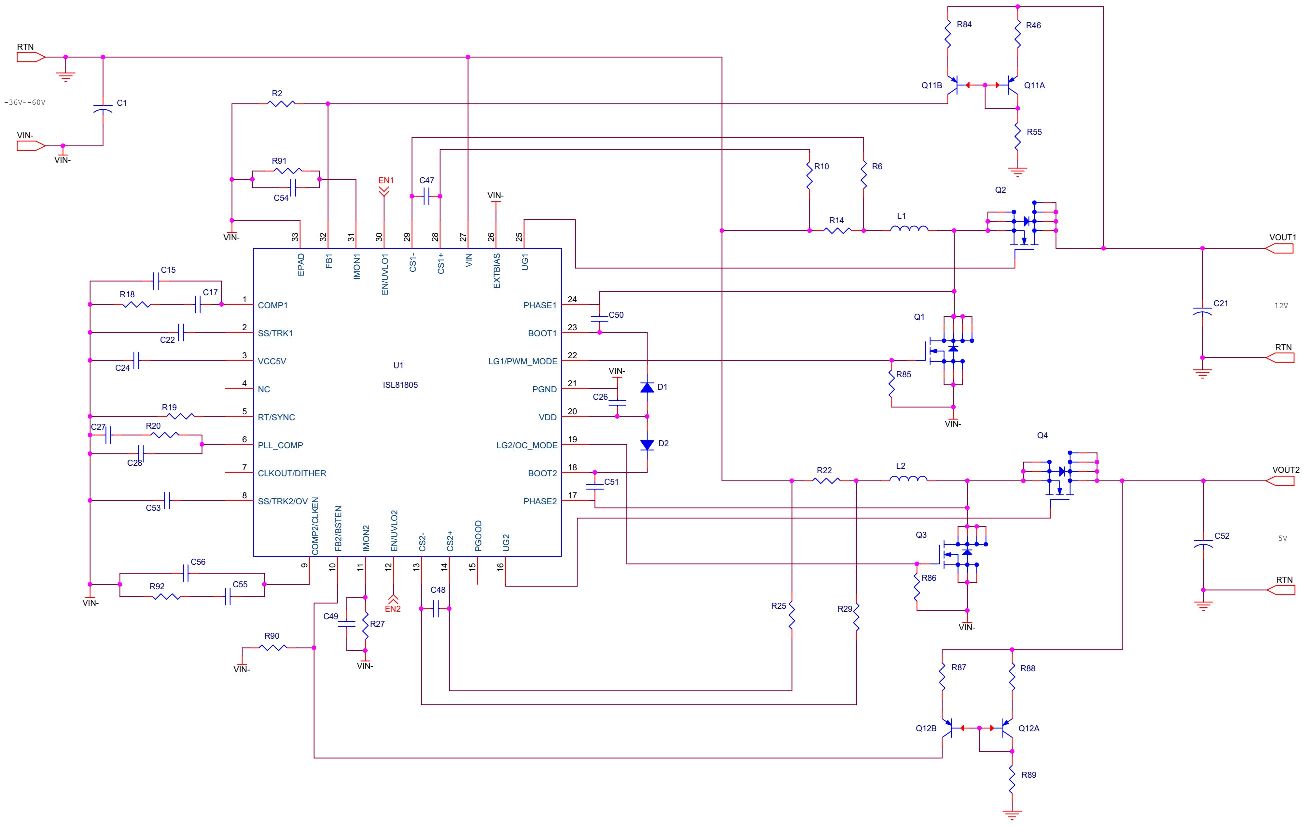


Figure 1. ISL81805EVAL3Z Block Diagram

Contents

1. Functional Description

The ISL81805EVAL3Z is the same test board used by Renesas application engineers and IC designers to evaluate the performance of the ISL81805 TQFN IC. The board provides an easy and complete evaluation of all the IC and board functions.

As shown in Figure 3, -36V to -60V V_{IN} is supplied to J1 (+) and J2 (-). The regulated 12V output is on J4 (+) and J5 (-), while the regulated 5V output is on J6 (+) and J7 (-). Because of the high-power efficiency, the evaluation board can run at 40A in total continuously without airflow at ambient room temperature conditions.

Test points TP1 through TP4 provide easy access to the IC pin and external signal injection terminals.

As shown in Table 2, connector J3 and J8 provide an option to disable each output respectively by shorting their Pin 1 and Pin 2.

1.1 Recommended Testing Equipment

The following materials are recommended for testing:

- 0V to 60V power supply with at least 25A source current capability
- Electronic loads capable of sinking current up to 25A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

1.2 Operating Range

The input voltage range is from -36V to -60V for an output voltage of 28V. If the output voltage is set to a lower value, the minimum V_{IN} can be reset to a lower value by changing the ratio of R_1 and R_5 for 12V output, the ratio of R_{120} and R_{121} for 5V output. The minimum EN threshold that V_{IN} can be set to is -4.5V.

The rated load current is 20A for each output with the OCP point set at a minimum I_{IN} = 25A at ambient room temperature conditions. The operating temperature range of this board is -40°C to +85°C.

Note: Airflow is needed for higher temperature ambient conditions.

1.3 Quick Test Guide

1. See Table 2 for the operating options. Ensure that the circuit is correctly connected to the supply and electronic loads before applying any power. See Figure 3 for the proper setup.
2. Turn on the power supply.
3. Adjust the input voltage (V_{IN}) within the specified range and observe the output voltage. The output voltage variation should be within 3%.
4. Adjust the load current within the specified range and observe the output voltage. The output voltage variation should be within 3%.
5. Use an oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, see Figure 2 for the proper test setup.

Table 2. Operating Options

Jumper	Position	Function
3	EN1-GND	Disable 12V output
	EN1 Floating	Enable 12V output
8	EN2-GND	Disable 5V output
	EN2 Floating	Enable 5V output

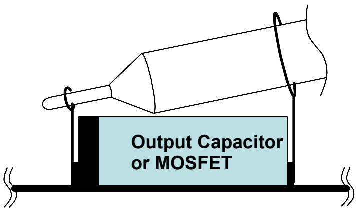


Figure 2. Proper Probe Setup to Measure Output Ripple and Phase Node Ringing

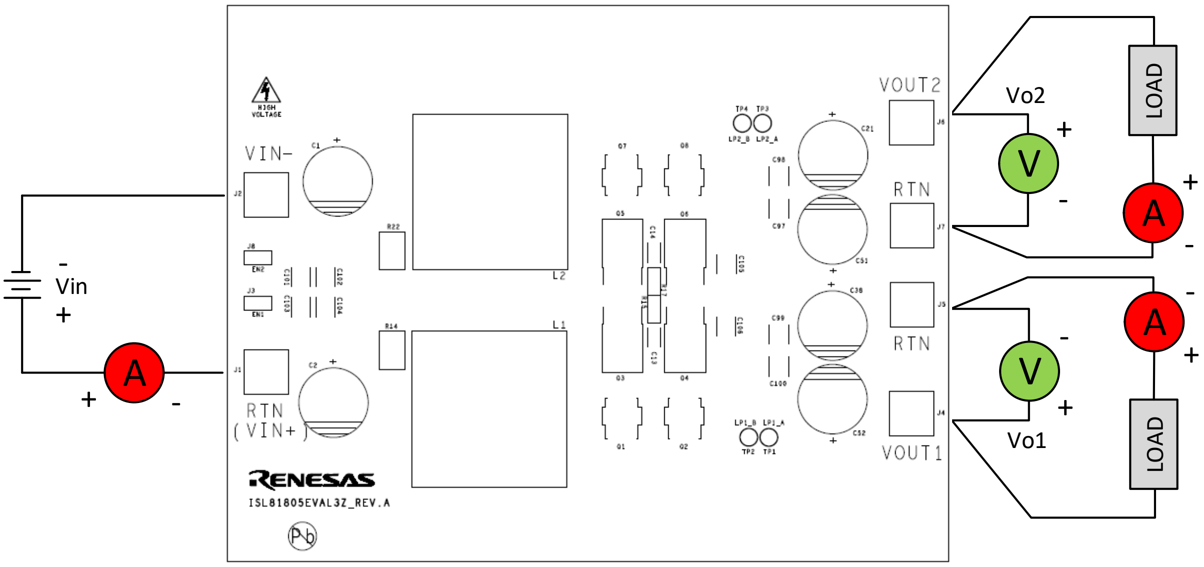


Figure 3. Proper Test Setup

2. Board Design

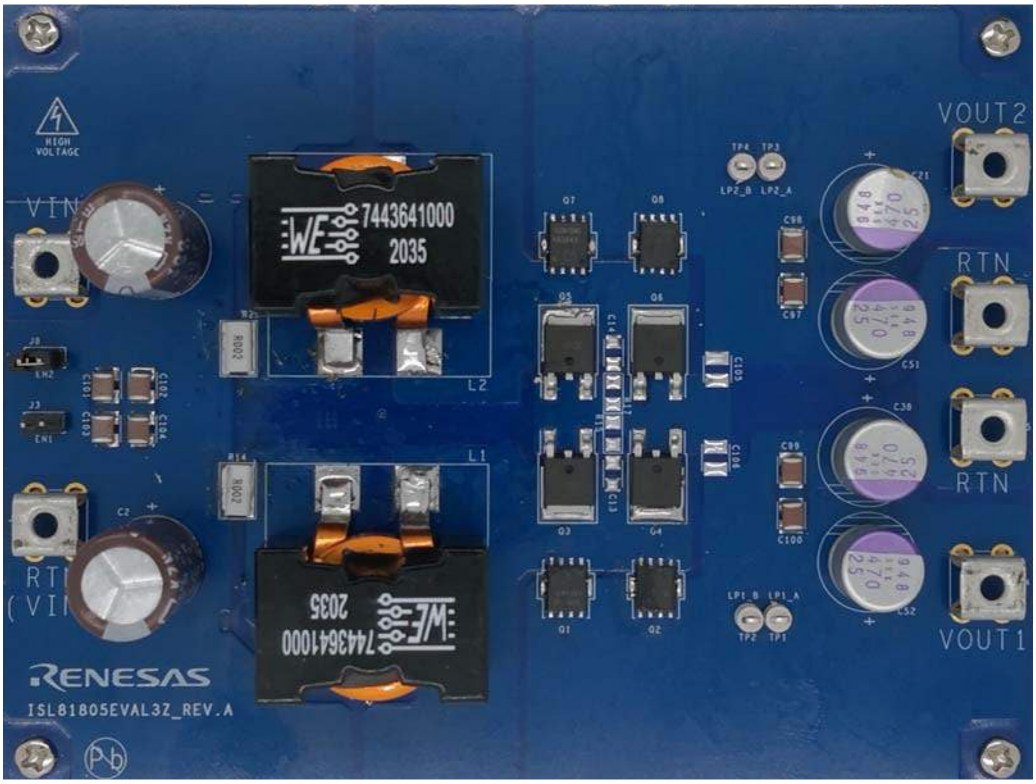


Figure 4. ISL81805EVAL3Z Evaluation Board, Top View

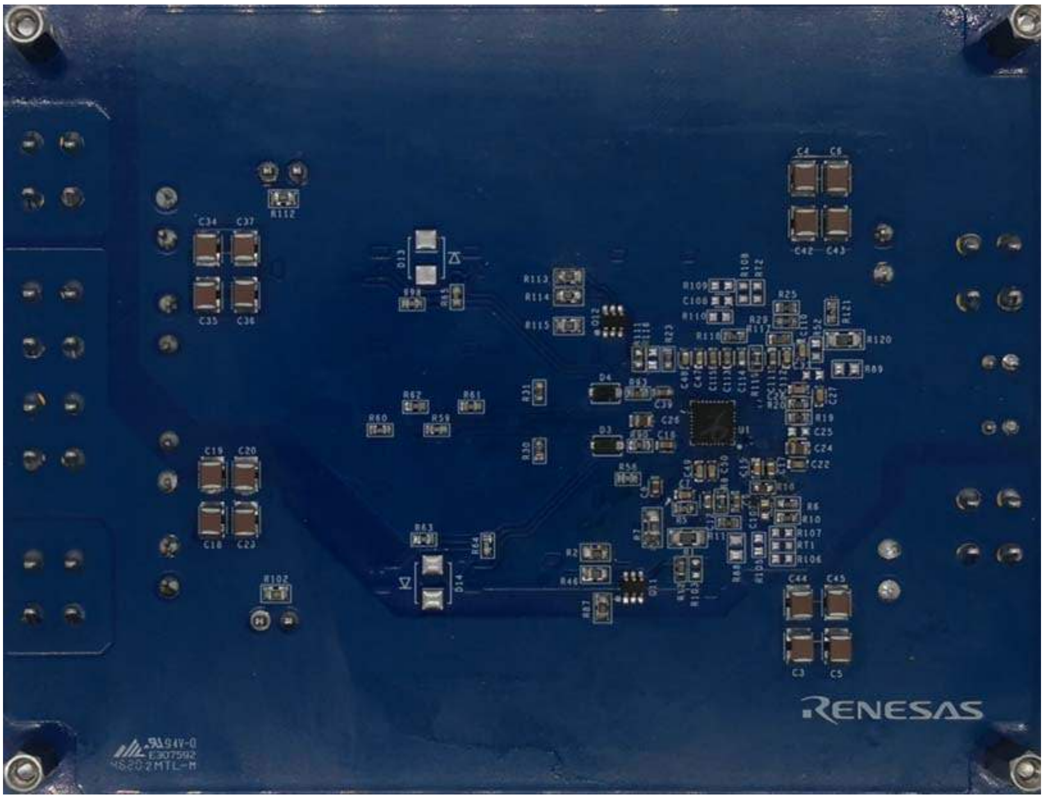


Figure 5. ISL81805EVAL3Z Evaluation Board, Bottom View

2.1 PCB Layout Guidelines

Careful attention to the printed circuit board (PCB) layout requirements is necessary for the successful implementation of an ISL81805 based DC/DC converter. The ISL81805 switches at a high frequency; therefore, the switching times are short. At these switching frequencies, even the shortest trace has significant impedance and the peak gate drive current rises significantly in an extremely short time. The transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes.

Three sets of components are critical when using the ISL81805 DC/DC converter:

- Controller
- Switching power components
- Small-signal components

The switching power components are the most critical to the layout because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small-signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer PCB is recommended.

Complete the following steps to optimize the PCB layout.

- Place the input capacitors, FETs, inductor, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high frequency decoupling ceramic capacitors as close as possible to the MOSFETs.
- If signal components and the IC are placed in a separate area to the power train, use full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for the power ground and the small-signal ground. Connect the SGND and PGND close to the IC. DO NOT connect them anywhere else.
- Keep the loop formed by the output capacitor, the boost top FET, and the boost bottom FET as small as possible.
- Keep the current paths from the input capacitor to the FETs, the boost FETs, and the output capacitor as short as possible with maximum allowable trace widths.
- Place the PWM controller IC close to the lower FETs. The low-side FETs gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
- Place the VDD bypass capacitor close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane using a via. Do not directly connect the PGND pin to the SGND EPAD.
- Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
- Place the output capacitors as close to the load as possible. Use short, wide copper regions to connect output capacitors to load to avoid inductance and resistances.
- Use copper filled polygons or wide short traces to connect the junction of the upper FET, lower FET, and output inductor. Also, keep the PHASE nodes connection to the IC short. DO NOT oversize the copper islands for the PHASE nodes. Because the phase nodes are subjected to high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
- Route all high-speed switching nodes away from the control circuitry.
- Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small signal grounding paths including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.
- Use a pair of traces with minimum loop for the input or output current sensing connection.
- Ensure the feedback connection to the output capacitor is short and direct.

2.2 Schematic Drawing

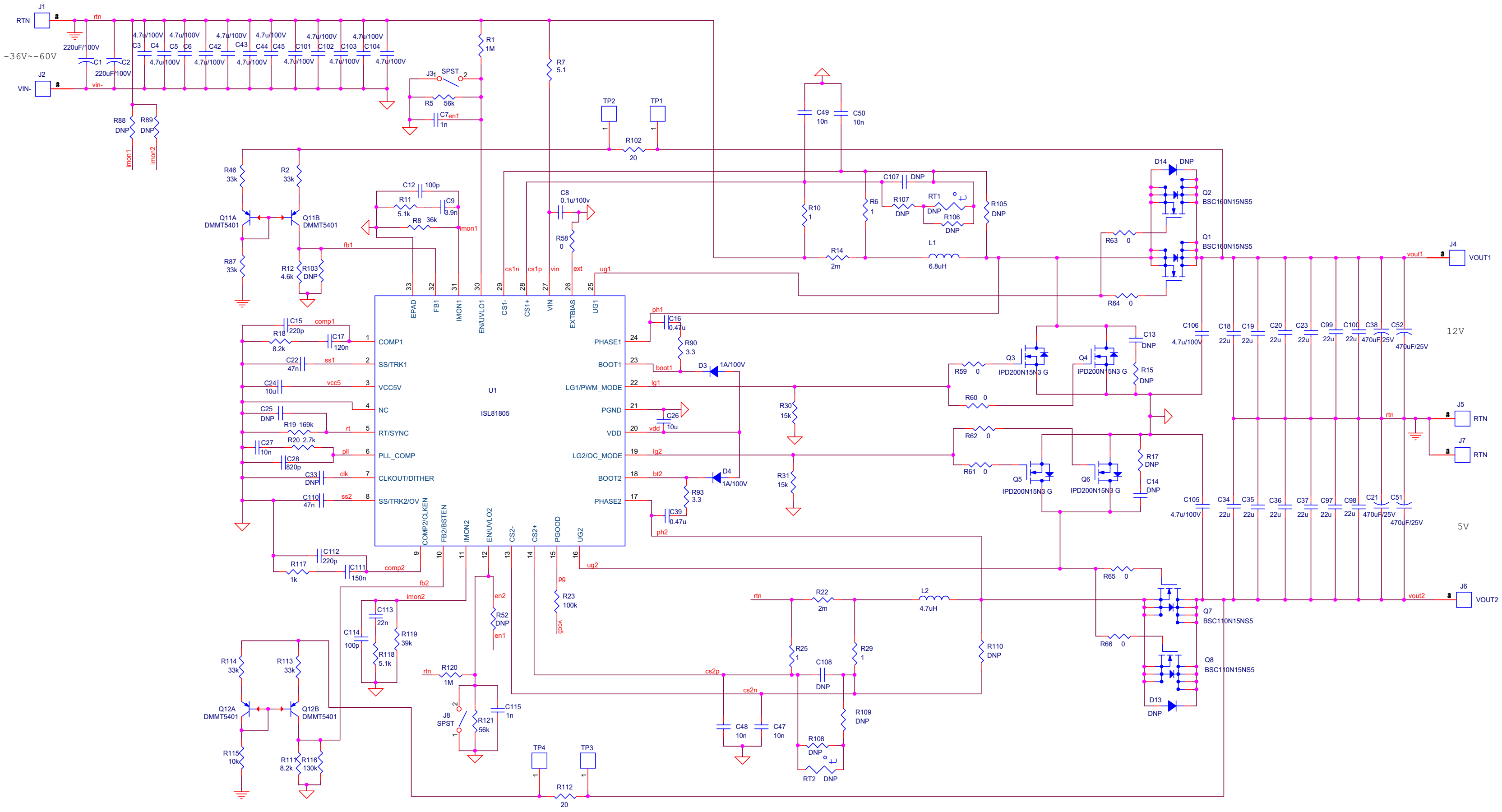


Figure 6. ISL81805EVAL3Z Schematic Drawing

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL81805EVAL3Z, REVA, ROHS	Multilayer PCB Technology	ISL81805EVAL3ZREVAPCB
2	C1, C2	CAP, RADIAL, 12.5x26.5, 220µF, 100V, 20%, ALUM.ELEC., 5mm, ROHS	United Chemi-Con	EKZN101ELL221MK25S
14	C3, C4, C5, C6, C42, C43, C44, C45, C101, C102, C103, C104, C105, C106	CAP-AEC-Q200, SMD, 1210, 4.7µF, 100V, 10%, X7S, ROHS	TDK	CGA6M3X7S2A475K200AB
12	C18, C19, C20, C23, C34, C35, C36, C37, C97, C98, C99, C100	CAP, SMD, 1210, 22µF, 100V, 10%, X7R, ROHS	Murata	GRM32ER71E226KE15L
2	C7, C115	CAP, SMD, 0603, 1000pF, 50V, 10%, X7R, ROHS	TDK	C1608X7R1H102K080AE
1	C8	CAP, SMD, 0603, 0.1µF, 100V, 10%, X7R, ROHS	Murata	GRJ188R72A104KE11D
2	C9, C113	CAP, SMD, 0603, 3900pF, 50V, 10%, X7R, ROHS	Kemet	C0603C392K5RACTU
2	C12, C114	CAP, SMD, 0603, 100PF, 50V, X7R, 10%, ROHS	Kemet	C0603C101K5RACTU
2	C15, C112	CAP, SMD, 0603, 220pF, 50V, 10%, X7R, ROHS	Murata	GRM188R71H221KA01D
2	C16, C39	CAP, SMD, 0603, 0.47µF, 25V, 10%, X7R, ROHS	Murata	GRM188R71E474KA12D
1	C17	CAP, SMD, 0603, 0.12µF, 50V, X7R, ROHS	Kemet	C0603C124K5RAC7867
1	C21	CAP, Radial, 10x13, 1000µF, 16V, ALUM POLY, 14mΩ	Panasonic	16SEPF1000M
2	C38, C52	CAP, RADIAL, 10x13, 470µF, 25V, 20%, ALUM.ELEC., ROHS	Panasonic	25SEK470M
2	C22, C110	CAP, SMD, 0603, 0.047µF 25V X7R, ROHS	Kemet	C0603C473K3RACTU
4	C24, C26, C89, C92	CAP, SMD, 0805, 10µF, 16V, 10%, X7S, ROHS	Murata	GRM21BC71C106KE11L
1	C28	CAP, SMD, 0603, 820pF, 50V, 10%, X7R, ROHS	Kemet	C0603C821K5RACTU
2	C56, C91	CAP, SMD, 0603, 0.47µF, 25V, X7R, ROHS	Murata	GRM188R71E474KA12D
1	C57	CAP, SMD, 0805, 2.2µF, 16V, X7R, ROHS	TDK	C2012X7R1C225M085AB
3	C87, C90, C93	CAP, SMD, 0805, 0.1µF, 16V, X7S, ROHS	Murata	GRM21BC71C106KE11L
2	C105, C106	CAP, SMD, 0.33µF, 200V, X7T, 1210, ROHS	TDK	CGJ6M3X7T2D334K200AA
1	C111	CAP, SMD, 0805, 0.15µF, 50V, X7S, ROHS	KEMET	C0603C154K5RAC7867

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
0	C25, C33, C107, C108	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
0	C13, C14	CAP, SMD, 1206, DNP-PLACE HOLDER, ROHS		
0	C51	CAP, TH, 10x13, DNP-PLACE HOLDER, ROHS		
2	D3, D4	DIODE-RECTIFIER, SMD, 2P, S0D-123FL, 100V, 1A, ROHS	ON Semiconductor	MBR1H100SFT3G
2	D13, D14	DIODE, SMB, DNP		
6	J1, J2, J4, J5, J6, J7	HDWARE, TERMINAL, M4 METRIC SCREW, TH, 4P, SNAP-FIT, ROHS	Keystone	7795
2	J3, J8	CONN-HEADER, 1x2, BRKAWY 1x36, 2.54mm, ROHS	BERG/FCI	69190-202HLF
1	L1	COIL-PWR INDUCTOR, SMD, 6.8µH, 20%, 30A, 2.4mΩ, ROHS	Wurth	7443640680
1	L2	COIL-PWR INDUCTOR, SMD, 4.7µH, 20%, 30A, 2.4mΩ, ROHS	Wurth	7443640470
1	U1	80V DUAL-BOOST PWM CONTROLLER, 32P, TQFN, 5x5, ROHS	Renesas Electronics America	ISL81805FRTZ
2	Q1, Q2	TRANSISTOR-MOS, N-CHANNEL, SMD, 8P, PPK SO-8, 150V, 56A, ROHS	Infineon	BSC160N15NS5ATMA1
2	Q7, Q8	TRANSISTOR-MOS, N-CHANNEL, SMD, 8P, PPK SO-8, 150V, 76A, ROHS	Infineon	BSC110N15NS5ATMA1
4	Q3, Q4, Q5, Q6	TRANSISTOR-MOS, N-CHANNEL, SMD, DPAK-2, 150V, 50A, ROHS	Infineon	IPD200N15N3GATMA1
2	Q11, Q12	TRANS 2PNP 150V 0.2A SOT26	Diodes	DMMT5401
2	R1, R120	RES SMD 1MΩ 1% 1/4W 1206	Yageo	RC1206FR-071ML
5	R2, R46, R87, R113, R114	RES SMD 33kΩ 1% 1/10W 0805	Yageo	RC0805FR-0733KL
2	R5, R121	RES SMD 56kΩ 1% 1/10W 0603	Yageo	RC0603FR-0756KL
4	R6, R10, R25, R29	RES SMD 1Ω 1% 1/10W 0603	Panasonic	ERJ-3RQF1R0V
1	R7	RES SMD 5.1Ω 1% 1/10W 1206	Yageo	RC1206FR-075R1L
1	R8	RES SMD 36kΩ 1% 1/10W 0603	Yageo	RC0603FR-0736KL
2	R11, R118	RES SMD 5.1kΩ 1% 1/10W 0603	Yageo	RC0603FR-075K1L

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	R12	RES SMD 4.64kΩ 1% 1/10W 0603	Yageo	RC0603FR-074K64L
2	R14, R22	RES SMD 0.002Ω 3W 2512 WIDE	Susumu	KRL6432E-M-R002-G-T1
2	R18, R111	RES SMD 8.2kΩ 1% 1/10W 0603	Yageo	RC0603FR-078K2L
1	R19	RES SMD 169kΩ 1% 1/10W 0603	Yageo	RC0603FR-07169KL
1	R20	RES SMD 2.7kΩ 1% 1/10W 0603	Yageo	RC0603FR-072K7L
1	R23	RES SMD 100kΩ 1% 1/10W 0603	Yageo	RC0603FR-07100KL
2	R30, R31	RES SMD 15kΩ 1% 1/10W 0603	Yageo	RC0603FR-0715KL
9	R58, R59, R60, R61, R62, R63, R64, R65, R66	RES SMD 0Ω 1% 1/10W 0603	Yageo	RC0603FR-070RL
2	R83, R89	RES SMD 2.2Ω 1% 1/10W 0603	Yageo	AC0603JR-072R2L
2	R85, R86	RES SMD 27kΩ 1% 1/10W 0603	Yageo	RC0603FR-0727KL
2	R90, R93	RES SMD 3.3Ω 1% 1/10W 0603	Yageo	RC0603FR-073R3L
2	R102, R112	RES SMD 20Ω 1% 1/10W 0603	Yageo	RC0603FR-0720RL
1	R115	RES SMD 10 Ω 1% 1/10W 0805	Yageo	RC0805FR-0710KL
1	R116	RES SMD 130KΩ 1% 1/10W 0603	Yageo	RC0603FR-07130KL
1	R117	RES SMD 1KΩ 1% 1/10W 0603	Yageo	RC0603FR-071KL
1	R119	RES SMD 39KΩ 1% 1/10W 0603	Yageo	RC0603FR-0739KL
0	RT1, RT2, R52, R103, R105, R106, R107, R108, R109, R110	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS		
0	R15, R17	RES, SMD, 1206, DNP-PLACE HOLDER, ROHS		
0	R88, R89	RES, SMD, 0805, DNP-PLACE HOLDER, ROHS		
4	TP1, TP2, TP3, TP4	CONN-COMPACT TEST PT, VERTICAL, WHT, ROHS	Keystone	5007
4	Four corners	SCREW, 4-40x1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Keystone	2204
4	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX,ALUMINUM, 0.25 OD, ROHS	Keystone	7795

2.4 Board Layout

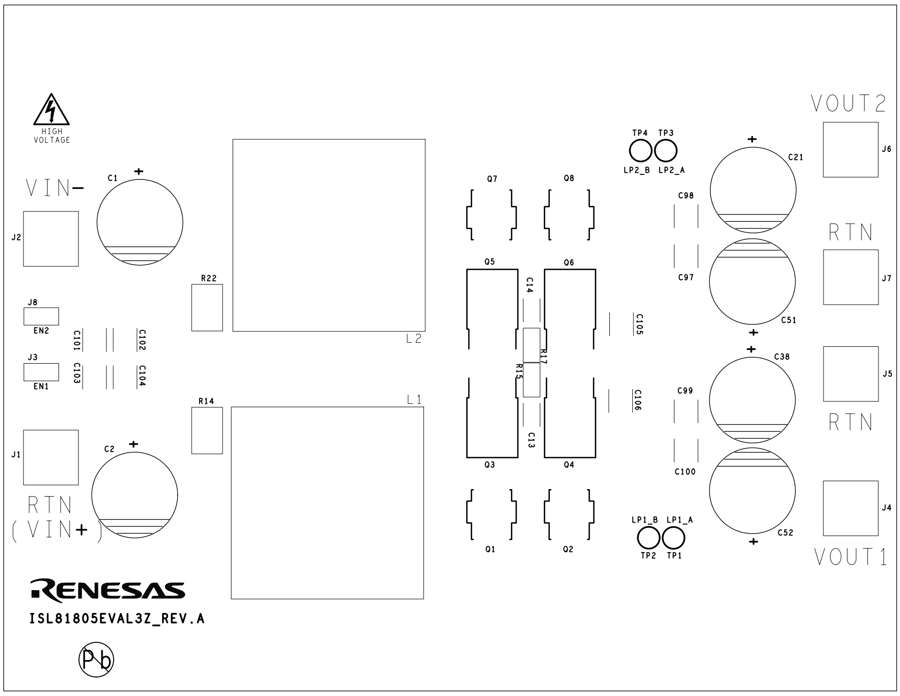


Figure 7. Silkscreen Top

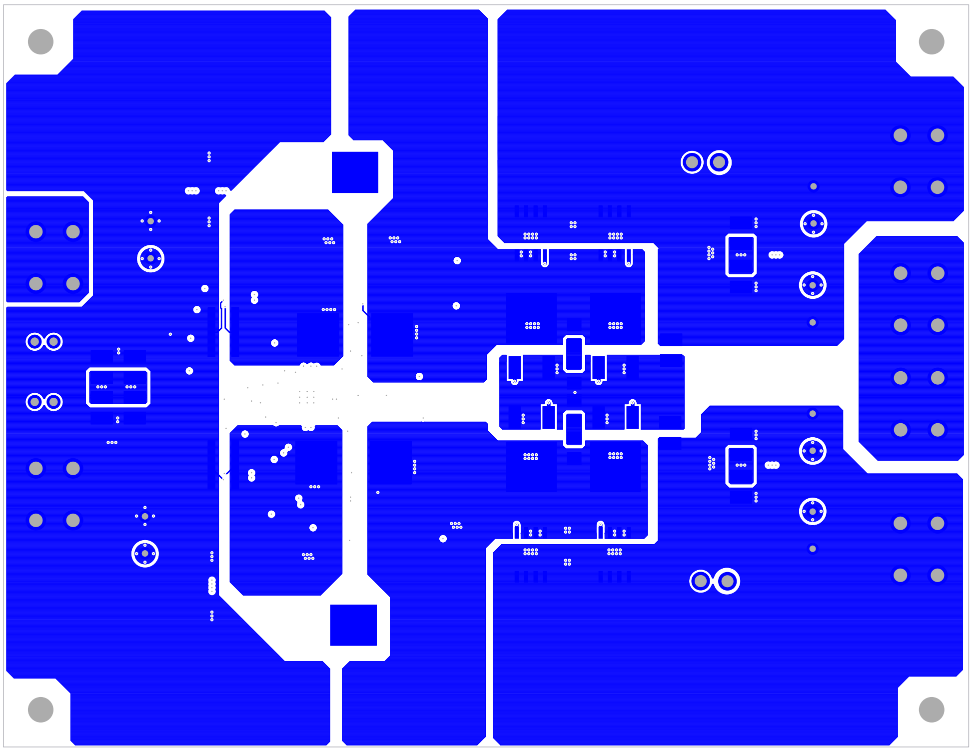


Figure 8. Top Layer

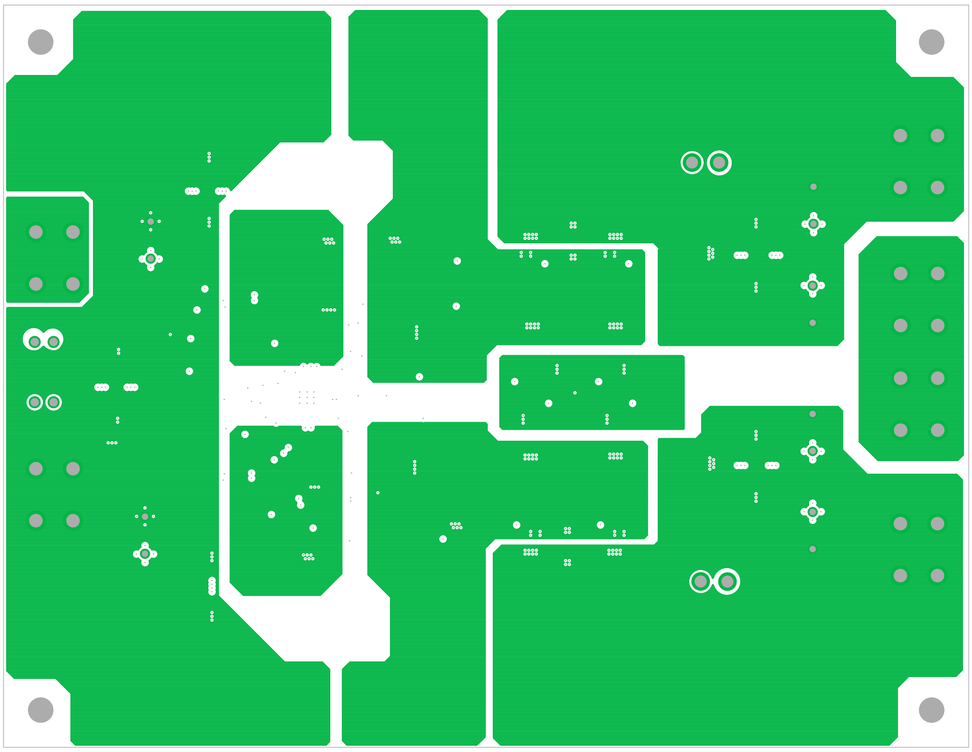


Figure 9. Second Layer

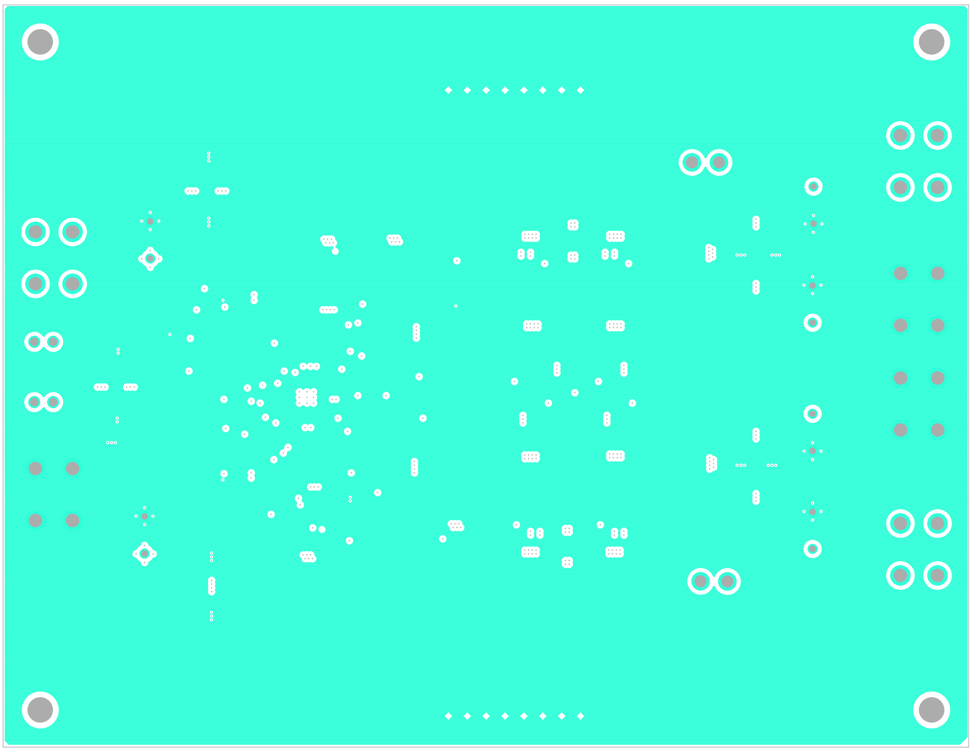


Figure 10. Third Layer

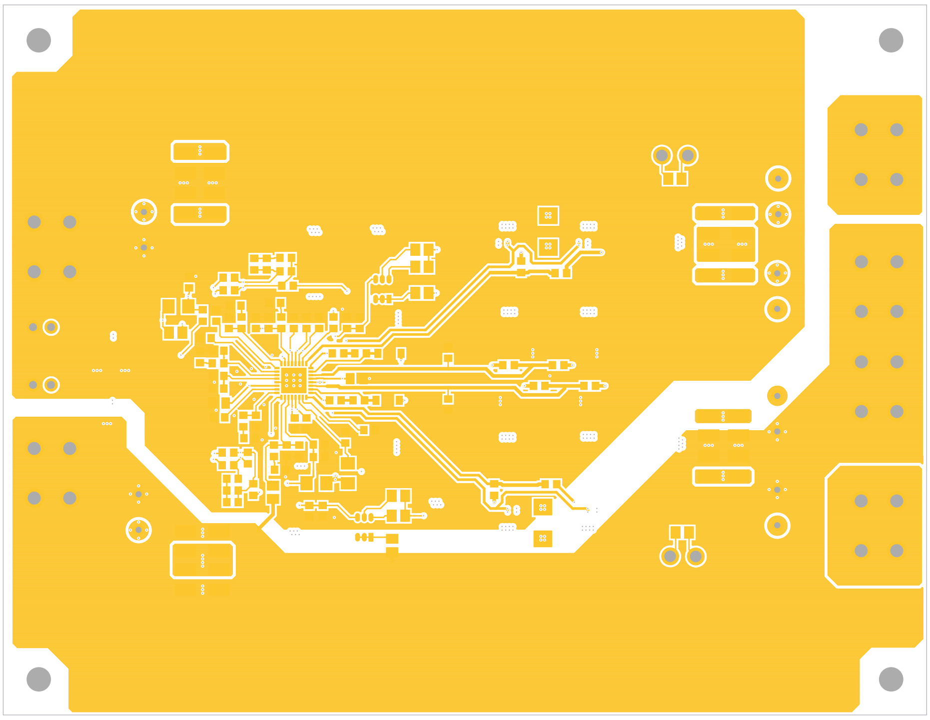


Figure 11. Bottom Layer

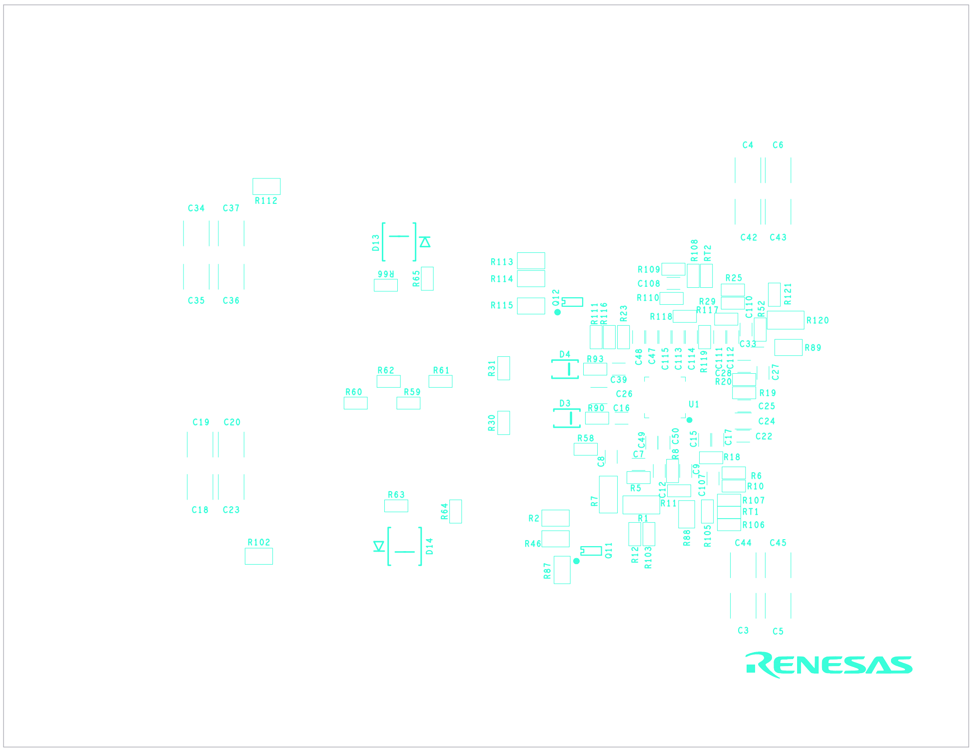


Figure 12. Silkscreen Bottom

2.5 Design Procedure

2.5.1 Design Requirements

Parameter	Rating
Input Voltage	-36V to -60V
Switching Frequency	200kHz
Output Voltage 1	12V
Output Current 1	20A
Output Voltage 2	5V
Output Current 2	20A
OCP Set Point (input average)	Minimum 8A for 12V output, 3.3A for 5V output at ambient room temperature
Output Mode	Dual output
PWM Mode	Forced PWM
OCP Mode	Constant current

2.5.2 Frequency Setting

The default switching frequency of the PWM controller is determined by the resistor R_T (R19). It adjusts the default switching frequency from 100kHz to 1MHz. The R_T value for f_{SW} = 200kHz is calculated using Equation 1.

(EQ. 1)

$$R_T = \left(\frac{34.7}{f_{SW}} - 4.78\right) = \frac{34.7}{0.2} - 4.78 = 168.72k\Omega$$

where f_{SW} is the switching frequency in MHz. Select a standard value resistor R_T = 169kΩ.

2.5.3 Output Voltage Setting

The ISL81805 is configured to be inverting buck-boost operation on this board. The GND pin of ISL81805 is connected to the negative input voltage terminal (VIN-), so the ground of ISL81805 is different with the load on output side. The two outputs voltage are sampled and feed back to the FB1 and FB2 pins using a current mirror circuit, respectively.

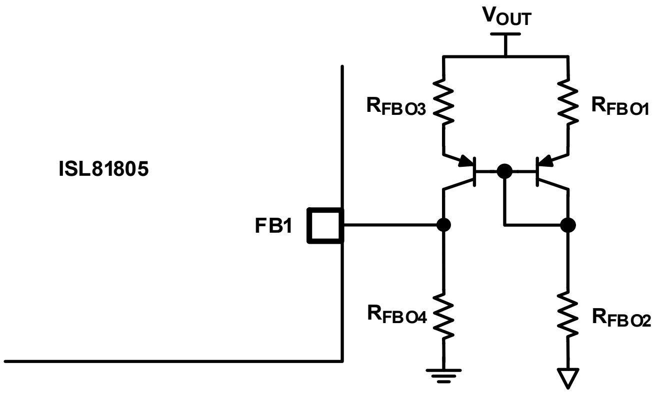


Figure 13. Output Voltage Feedback Network

V_{OUT} is calculated using Equation 2.

(EQ. 2)

$$V_{OUT} = \frac{0.8V}{R_{FBO4}} \times (R_{FBO1} + R_{FBO2}) + V_{BE}$$

where R_{FBO1} and R_{FBO3} are the top resistors of the current mirror network and they should be the same value. R_{FBO2} is the bottom resistor connected to ground of output/load side. R_{FBO4} is the bottom resistor connected between FB1 pin and chip ground (VIN-). V_{BE} is Base-Emitter saturation voltage of Q1A, typical 0.6V for DMMT5401. V_{OUT} can be set by changing the value of resistor R_{FBO4} for convenience.

With V_{OUT1} = 12V, R_{FBO1} (R46) = R_{FBO3} (R2) = 33kΩ, and R_{FBO2} (R87) = 33kΩ, then R_{FBO4} (R12) value can be calculated using Equation 3.

(EQ. 3)

$$R_{FBO4} = \frac{0.8V}{(V_{OUT1} - V_{BE})} \times (R_{FBO1} + R_{FBO2}) = \frac{0.8V}{(12V - 0.6V)} \times (33k\Omega + 33k\Omega) = 4.63k\Omega$$

Select a standard value resistor R_{FBO4} = 4.6kΩ.

2.5.4 UVLO Setting

The ISL81805 has input UVLO protection. When the voltage on the EN/UVLO pin reaches 1.8V, the PWM modulator is enabled. Accurate UVLO feature can be implemented by feeding the V_{IN} into the EN/UVLO pin using a voltage divider, R_{UV1} (R1) and R_{UV2} (R5). The V_{IN} UVP rising threshold is calculated using Equation 4.

(EQ. 4)

$$V_{UVRISE} = \frac{V_{UVLO\_THR}(R_{UV1} + R_{UV2}) - I_{LEAK}R_{UV1}R_{UV2}}{R_{UV2}} = \frac{1.8V(1M\Omega + 56k\Omega) - 2.8\mu A(1M\Omega)(56k\Omega)}{56k\Omega} = 32.54V$$

The V_{IN} UVP falling threshold is calculated using Equation 5.

(EQ. 5)

$$V_{UVFALL} = \frac{V_{UVLO\_THR}(R_{UV1} + R_{UV2}) - I_{UVLO\_HYST}R_{UV1}R_{UV2}}{R_{UV2}} = \frac{1.8V(1M\Omega + 56k\Omega) - 6.8\mu A(1M\Omega)(56k\Omega)}{56k\Omega} = 30.54V$$

where V_{UVLO_THR} is the 1.8V UVLO rising threshold and I_{UVLO_HYST} is the 6.8μA UVLO hysteresis current.

2.5.5 Soft-Start Capacitor

The soft-start time for dual-phase is set by the value of the soft-start capacitor C_{SS1} (C22) connected from SS/TRK1 to GND and C_{SS2} (C110) connected from SS/TRK2 to GND separately. The soft-start time with C_{SS1} = C_{SS2} = 47nF is calculated using Equation 6.

(EQ. 6)

$$t_{SS} = 0.8V\left(\frac{C_{SS}}{4\mu A}\right) = 0.8V \times \left(\frac{47nF}{4\mu A}\right) = 9.4ms$$

When the soft-start time set by external C_{SS} or tracking is less than 1.7ms, an internal soft-start circuit of 1.7ms takes over the soft-start.

2.5.6 MOSFET Considerations

The MOSFETs are selected based on $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The power loss of the upper and lower MOSFETs for each phase is calculated using Equation 7 and Equation 8. The equations assume linear voltage current transitions and ignore the power loss cause by the reverse recovery of the body diode of the lower MOSFET.

(EQ. 7)

$$P_{LOWERMAX} = \left(\frac{I_{OUT1}}{1-D_{MAX}}\right)^2\frac{(V_{OUT1})(r_{DS(ON)})}{(V_{OUT1}+V_{INMIN})} + \frac{\left(\frac{I_{OUT1}}{1-D_{MAX}}\right)(V_{OUT1}+V_{INMIN})(t_{SW})(f_{SW})}{2}$$

$$= \left(\frac{20A}{1-0.25}\right)^2\frac{(12V)\left(\frac{16m\Omega}{2}\right)}{(12V+36V)} + \frac{\left(\frac{20A}{1-0.25}\right)(12V+36V)\left(\frac{4nC\times 2}{\left(\frac{8V-5.8V}{4.3\Omega}\right)} + \frac{4nC\times 2}{\left(\frac{5.8V}{1\Omega}\right)}\right)(200kHz)}{2} = 1.422W + 4.356W = 5.778W$$

(EQ. 8)

$$P_{UPPERMAX} = \frac{\left(\frac{I_{OUT1}}{1-D_{MAX}}\right)^2(V_{INMIN})(r_{DS(ON)})}{(V_{OUT1}+V_{INMIN})} = \frac{\left(\frac{20A}{1-0.25}\right)^2(36V)\left(\frac{16m\Omega}{2}\right)}{(12V+36V)} = 4.266W$$

Ensure that all MOSFETs are within their maximum junction temperature with enough margin at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

2.5.7 Inductor Selection

The inductor value determines the ripple current of the converter. To limit the inductor core less, the inductor ripple current is usually 40% to 80% of the rated output current. Assume the ripple current ratio is 30% of the inductor average current at the minimum input voltage and the full output load condition. The inductor value for the 12V output is calculated using Equation 9.

(EQ. 9)

$$L_{INMIN} = \frac{(V_{OUT1})(V_{INMIN})}{(f_{SW})\left(0.3\times\frac{I_{OUT1}}{1-D_{MAX}}\right)(V_{OUT1}+V_{INMIN})} = \frac{(12V)(36V)}{(200kHz)\left(0.3\times\frac{20A}{1-0.25}\right)(12V+36V)} = 5.62\mu H$$

The recommended inductor value is 6.8µH for lower current ripple. Then the ripple current and peak current are calculated using Equation 10, Equation 11, and Equation 12.

(EQ. 10)

$$\Delta I_{LMAX} = \frac{(V_{OUT1})(V_{INMIN})}{(f_{SW})(L)(V_{OUT1}+V_{INMIN})} = \frac{(12V)(36V)}{(200kHz)(6.8\mu H)(12V+36V)} = 6.6A$$

(EQ. 11)

$$I_{LRMSMAX} = \frac{I_{OUT1}}{1-D_{MAX}}\times\sqrt{1+\frac{(0.3)^2}{12}} = \frac{20A}{1-0.25}\times\sqrt{1+\frac{(0.3)^2}{12}} = 26.76A$$

(EQ. 12)

$$I_{LPEAKMAX} = \frac{I_{OUT1}}{1-D_{MAX}} + \frac{\Delta I_{LMAX}}{2} = \frac{20A}{1-0.25} + \frac{6.6A}{2} = 29.97A$$

The saturation current of the inductor should be larger than 29.97A. The heat rating current of the inductor should be larger than 26.76A.

With inductor 7443640680 from Wurth Electronics, the maximum DC power dissipation in the inductor is approximately calculated using Equation 13.

(EQ. 13) $$P_{LMAX} = (I_{LRMSMAX})^2(DCR) = (26.76A)^2 \times (2.4m\Omega) = 1.718W$$

2.5.8 Output Capacitor Selection

The minimum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown in Equation 14.

(EQ. 14) $$C_{OUTMIN} = \frac{I_{OUT1} \times V_{OUT1}}{f_{SW} \times \Delta V_{OUT} \times (V_{OUT1} + V_{INMIN})} = \frac{20A \times 12V}{200kHz \times 100mV \times (12V + 36V)} = 250\mu F$$

where C_{OUTMIN} is the minimum output capacitor(s) required. Choose a capacitor no less than 250µF for the 12V output. 940µF electrolytic capacitor and 132µF MLCC in total are used for the 12V output on this board.

2.5.9 Input Capacitor Selection

The important parameters for the input capacitors are the voltage rating and the RMS current rating. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline. The maximum RMS current supplied by the input capacitance occurs at D = 0.5. Therefore, the maximum AC RMS current is shown in Equation 15.

(EQ. 15) $$I_{RMSMAX} = \sqrt{D \times (1 - D)} \times \frac{I_{OUT1}}{1 - D_{MAX}} = \sqrt{0.5 \times (1 - 0.5)} \times \frac{20A}{1 - 0.25} = 13.33A$$

Renesas recommends using a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Two 220µF electrolytic capacitors and twelve 4.7µF ceramic capacitors are used to share the input RMS current on this board.

2.5.10 First Level Peak Current Limit and Sense Resistor Selection

The inductor peak current is sensed by the sense resistor R_S (R14). When the voltage drop on R_S reaches the set point $V_{OCSET\text{-}CS}$ typical 85mV, it triggers the pulse-by-pulse peak current limit. With the current limit set point I_{OCPP1} >= 1.5xI_{INMAX} = 40A for the 12V output, the value of the sense resistor is calculated using Equation 16.

(EQ. 16) $$R_S = \frac{V_{OCSET-CS}}{I_{OCPP1}} = \frac{82mV}{40A} = 2.05m\Omega$$

Select a standard value resistor R_S = 2mΩ. Then the actual peak current limit is calculated using Equation 17.

(EQ. 17) $$I_{OCPP1} = \frac{V_{OCSET-CS}}{R_S} = \frac{82mV}{2m\Omega} = 41A$$

The maximum power dissipation in R_S is calculated using Equation 18.

(EQ. 18) $$P_{RSMAX} = (I_{LRMSMAX})^2 R_S = (26.67A)^2(2m\Omega) = 1.42W$$

Therefore, a sense resistor with 2W power rating is sufficient for this application.

2.5.11 Second Level Hiccup Peak Current Protection

In the condition that V_{IN} is close to V_{OUT}, the inductor current runs away with the minimum on PWM duty. The ISL81805 integrates a second level hiccup type of peak current protection. The second level peak current protection set point I_{OCPP2} is calculated using Equation 19.

(EQ. 19)
$$I_{OCPP2} = \frac{V_{OCSET\text{-}CS\text{-}HIC}}{R_S} = \frac{98mV}{2m\Omega} = 49A$$

2.5.12 Input Average Overcurrent Protection and R_{IM} Selection

The ISL81805 provides either constant current or hiccup type of overcurrent protection for input average current. The OCP mode is set by a resistor connected between the LG2/OC_MODE pin and ground. With input constant current/hiccup set point I_{INOCP1} = 8A for the 12V output, the current monitoring resistor R_{IM} (R8) is calculated using Equation 20.

(EQ. 20)
$$R_{IM} = \frac{1.2}{\left(\frac{I_{INOCP1} \times V_{IN}}{V_{OUT1}} + I_{INOCP1}\right) \times R_S \times Gm_{CS} + I_{CSOFFSET}} = \frac{1.2V}{\left(\frac{8A \times 36V}{12V} + 8A\right) x2m\Omega x200\mu S + 20\mu A} = 36.58k\Omega$$

where $I_{CSOFFSET}$ is the output current sense op amp internal offset current, typical 20µA. Select a standard value resistor R_{IM} = 36kΩ.

2.5.13 Output Mode Selection

When the IMON2 pin voltage is lower than 3V, the IC is set for dual output application.

2.5.14 PWM Mode Selection

You can set the ISL81805 to either forced PWM mode or DE mode. The mode is set by a resistor $R_{PWMMODE}$ (R30) connected between the LG1/PWM_MODE pin and GND. The boundary resistor value for $R_{PWMMODE}$ is calculated using Equation 21.

(EQ. 21)
$$R_{PWMMODE} = \frac{0.3V}{10\mu A} = 30k\Omega$$

A resistor less than 30kΩ sets the converter to forced PWM mode, while a resistor higher than 30kΩ sets the converter to DE mode. Considering the tolerance in all temperature ranges, Renesas recommends using 15kΩ to set Forced PWM mode and 51kΩ to set DE mode.

2.5.15 Overcurrent Protection Mode Selection

The ISL81805 is set to either a constant current or hiccup type of overcurrent protection for input average current by selecting a different value of the resistor R_{OCMODE} (R31) connected between LG2/OC_MODE and GND. The boundary resistor value for R_{OCMODE} is calculated using Equation 22.

(EQ. 22)
$$R_{OCMODE} = \frac{0.3V}{10\mu A} = 30k\Omega$$

A resistor less than 30kΩ sets the converter to constant current mode, while a resistor higher than 30kΩ sets the converter to Hiccup mode. Considering the tolerance in all temperature ranges, Renesas recommends using 15kΩ to set constant current mode and 51kΩ to set the Hiccup mode.

2.5.16 Phase Lock Loop (PLL)

The PLL of the ISL81805 ensures the wide range of accurate clock frequency and phase setting. It also makes the internal clock easily synchronized to an external clock with the frequency either lower or higher than the internal setting. The external compensation network of R_{PLL} (R20), C_{PLL1} (C27), and C_{PLL2} (C28) is needed to connect to the PLL_COMP pin to ensure PLL stable operation. Renesas recommends choosing 2.7kΩ for R_{PLL}, 10nF for C_{PLL1}, and 820pF for C_{PLL2}.

2.5.17 Feedback Loop Compensation

To adapt the different applications, the controller is designed with an externally compensation network. Figure 14 shows the peak current mode buck-boost converter circuit.

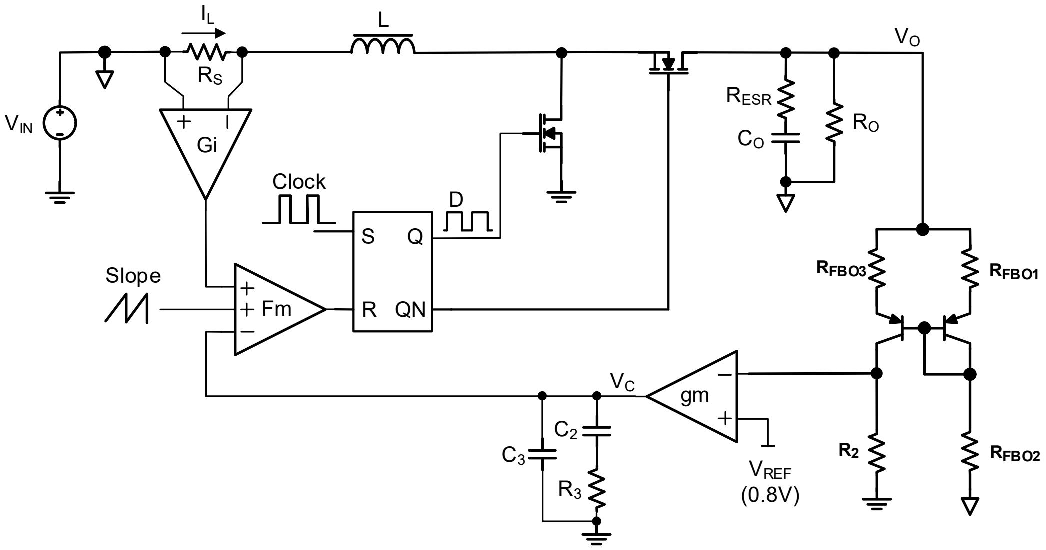


Figure 14. Peak Current Mode Buck-Boost Converter Circuit

In the current loop, the control to output simplified transfer function is shown in Equation 23.

(EQ. 23)
$$\frac{\hat{V}_O}{\hat{V}_C} = \frac{R_O \times (1-D)}{R_I \times K_d} \times \frac{\left(1-\frac{s}{\omega_{RHPZ}}\right)\left(1+\frac{s}{\omega_{z(esr)}}\right)}{\left(1+\frac{s}{\omega_{po}}\right)\left(1+\frac{s}{\omega_{pi}}\right)}$$

where:

(EQ. 24)
$$K_d = 1+D+\frac{R_O\cdot(1-D)^2}{R_I}\cdot\left(\frac{1}{K_m}+\frac{K}{1-D}\right)$$

(EQ. 25)
$$K_m = \frac{1}{(0.5-D)R_I\times\frac{T_s}{L}+\frac{V_{SL}}{V_O}}$$

(EQ. 26)
$$K = 0.5R_I\times\frac{T_s}{L}\times D\times(1-D)$$

(EQ. 27) $$R_I = G_I \times R_S$$

- R_O is the load resistor
- C_O is the output capacitor
- L is the inductor
- R_S is the current sense resistor
- V_O is the output voltage
- T_S is the period of one switching cycle
- D is the duty cycle of lower MOSFET
- V_{SL} = 0.843V, is the slope compensation voltage
- V_{IN} is the input voltage of the buck-boost
- V_C is the output of the error amplifier
- G_I = 5.472, is the gain of the current sensor

The low frequency pole frequency is shown in Equation 28.

(EQ. 28) $$\omega_{p0} = 2\pi f_{p0} = \frac{K_d}{C_o \times R_o}$$

The high frequency pole frequency is shown in Equation 29.

(EQ. 29) $$\omega_{pi} = 2\pi f_{pi} = \frac{K_m \times R_I}{L}$$

The output capacitor ESR (R_{ESR}) zero frequency is shown in Equation 30.

(EQ. 30) $$\omega_{z(esr)} = 2\pi f_{z(esr)} = \frac{1}{C_O \times R_{ESR}}$$

The output voltage is regulated by an error amplifier EA. The EA compensation network parameters can be determined by compensating the current loop poles and zero so as to implement an ideal -20dB/decade close-loop gain with crossover frequency around 1/50~1/20 of f_{sw} crossover frequency.

For buck-boost topology, the maximum crossover frequency is also limited by the RHPZ. Estimate the RHPZ at the input voltage with minimum absolute value using Equation 31.

(EQ. 31) $$\omega_{RHPZ} = 2\pi f_{RHPZ} = \frac{R}{L} \times \frac{(1 - D_{max})^2}{D_{max}}$$

If the crossover frequency $f_c << f_{pi}$, a type-2 compensation network is enough to achieve the goal.

The type-2 EA amplifier transfer function is simplified to Equation 32.

(EQ. 32) $$\frac{\hat{V}_c}{\hat{V}_o} = -\frac{R_2}{R_{FBO1} + R_{FBO2}} \cdot g_m \cdot \frac{1 + sR_3C_2}{s(C_2 + C_3) + s^2R_3C_2C_3} = -\frac{R_2}{R_{FBO1} + R_{FBO2}} \cdot \frac{g_m}{C_2 + C_3} \cdot \frac{1 + sR_3C_2}{s\left(1 + \frac{sR_3C_2C_3}{C_2 + C_3}\right)}$$

To simplify the model, assuming $C_3 << C_2$, the type-2 EA amplifier transfer function is simplified to Equation 33.

(EQ. 33) $$\frac{\hat{V}_c}{\hat{V}_o} = -\frac{R_2}{R_{FBO1}+R_{FBO2}} \cdot \frac{g_m}{C_2+C_3} \cdot \frac{1+sR_3C_2}{s(1+sR_3C_3)}$$

Where g_m is the gain of error amplifier, typical 1.75mS.

The transfer function has one pole and one zero.

- The pole is at the frequency of $f_{p1} = 1/2\pi R_3C_3$. This is the frequency where the impedance of R_3 is equal to C_3.
- The zero is at the frequency of $f_{z1} = 1/2\pi R_3C_2$. This is the frequency where the impedance of R_3 is equal to C_2.

To achieve ideal compensation, Renesas recommends making $f_{z1} = f_{p0}$ and $f_{p1} = f_{z(esr)}$ as shown in Figure 15.

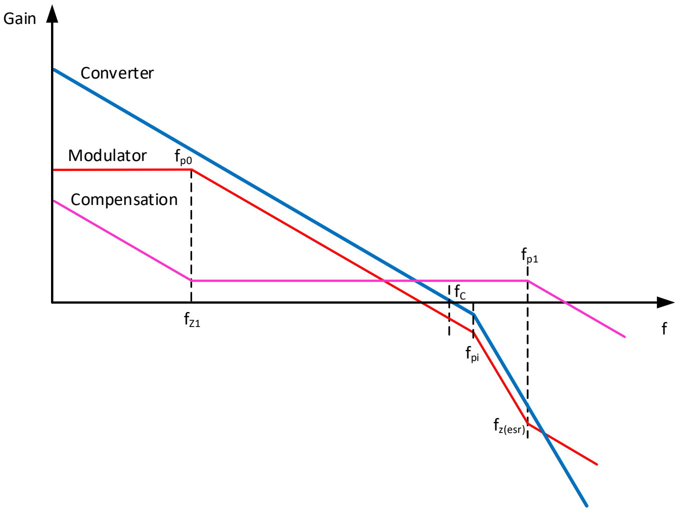


Figure 15. Feedback Loop Compensation

The close-loop transfer function is then simplified to Equation 34.

(EQ. 34) $$G_{loop}(s) = \frac{R_O \times (1-D)}{R_I \times K_d} \times \frac{\left(1-\frac{s}{\omega_{RHPZ}}\right)\left(1+\frac{s}{\omega_{z(esr)}}\right)}{\left(1+\frac{s}{\omega_{p0}}\right)\left(1+\frac{s}{\omega_{pi}}\right)} \times \left(-\frac{R_2}{R_{FBO1}+R_{FBO2}} \cdot \frac{g_m}{C_2+C_3}\right) \cdot \frac{1+sR_3C_2}{s(1+sR_3C_3)}$$

The Loop design example for the 12V output under -36V input voltage is shown in the following:

V_{IN} = -36V, V_{OUT} = 12V, I_{OUT} = 20A, f_{sw} = 200kHz, T_s = 5µs, D = $V_{OUT}/(-V_{IN}+V_{OUT})$ = 0.25, L = 10µH, C_O = 968.2µF (470µFx2+4.7µFx6), $R_O = V_{OUT}/I_{OUT}$ = 0.6Ω, R_s = 2mΩ, R_{esr} = 5mΩ.

(EQ. 35) $$K_m = \frac{1}{(0.5-D)R_I \times \frac{T_s}{L} + \frac{V_{SL}}{V_O}} = \frac{1}{(0.5-0.25)(2m\Omega \times 5.472) \times \frac{5\mu s}{10\mu H} + \frac{0.843V}{12V}} = 13.96$$

(EQ. 36) $$K_d = 1 + D + \frac{R_O \cdot (1-D)^2}{R_I} \cdot \left(\frac{1}{K_m} + \frac{K}{1-D}\right) = 1 + 0.25 + \frac{0.6 \cdot (1-0.25)^2}{2m\Omega \times 5.472} \cdot \left(\frac{1}{13.96} + 0.5 \times 2m\Omega \times 5.472 \times \frac{5\mu s}{10\mu H} \times 0.25\right) = 3.48$$

(EQ. 37) $$\omega_{p0} = \frac{K_d}{C_o \times R_o} = \frac{3.48}{968.2\mu F \times 0.6\Omega} = 5.99kHz$$

(EQ. 38) $$f_{p0} = \frac{\omega_{p0}}{2\pi} = 0.953kHz$$

(EQ. 39) $$\omega_{pi} = \frac{K_m \times R_I}{L} = \frac{13.96 \times 2m\Omega \times 5.472}{10\mu H} = 15.36kHz$$

(EQ. 40) $$f_{pi} = \frac{\omega_{pi}}{2\pi} = 2.445kHz$$

(EQ. 41) $$\omega_{z(esr)} = \frac{1}{C_O \times R_{ESR}} = \frac{1}{968.2\mu F \times 5m\Omega} = 206.6kHz$$

(EQ. 42) $$f_{z(esr)} = \frac{\omega_{z(esr)}}{2\pi} = 32.88kHz$$

The minimum value of RHPZ is calculated using Equation 43.

(EQ. 43) $$f_{RHPZ} = \frac{R_O}{2\pi \times L} \times \frac{(1 - D_{max})^2}{D_{max}} = \frac{0.6\Omega}{2\pi \times 10\mu H} \times \frac{(1 - 0.25)^2}{0.25} = 21.49kHz$$

Therefore make 0.05 x f_{RHPZ} as crossover frequency and make the gain -20dB/decade:

(EQ. 44) $$f_c = 0.05 \times f_{RHPZ} = 1.07kHz$$

If R_3 (R18) = 8.2k, set the frequency of this zero f_{z1}= f_{p0}, then C_2 (C17) is calculated using Equation 45.

(EQ. 45) $$C_2 = \frac{1}{2\pi R_3 f_{p0}} = \frac{1}{2\pi \times 8.2k\Omega \times 0.953kHz} = 20.37nF$$

Select a standard value capacitor C_2 (C17) = 22nF.

Set the frequency of this pole f_{p1} = $f_{z(esr)}$, and should make sure f_c<< f_{p1} << f_{sw}. C_3 (C15) is calculated using Equation 46.

(EQ. 46) $$C_3 = \frac{1}{2\pi R_3 f_{z(esr)}} = \frac{1}{2\pi \times 8.2k\Omega \times 32.88kHz} = 590pF$$

Select a standard value capacitor C_3 (C15) = 470pF.

3. Typical Performance Curves

V_{IN} = -48V, V_{OUT1} = 12V, V_{OUT2} = 5V, T_A = 25°C, unless otherwise noted.

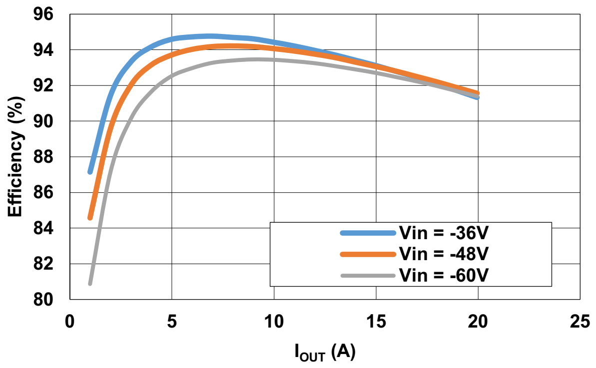


Figure 16. 12V Output Efficiency, CCM

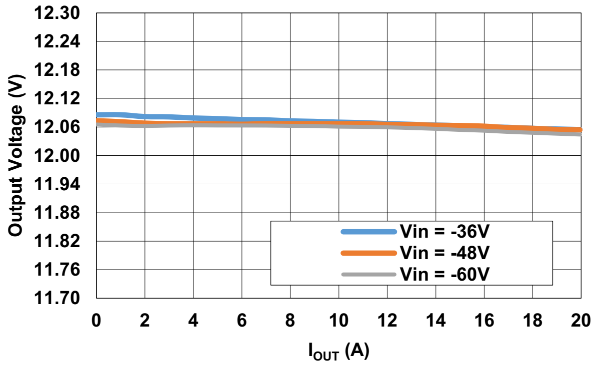
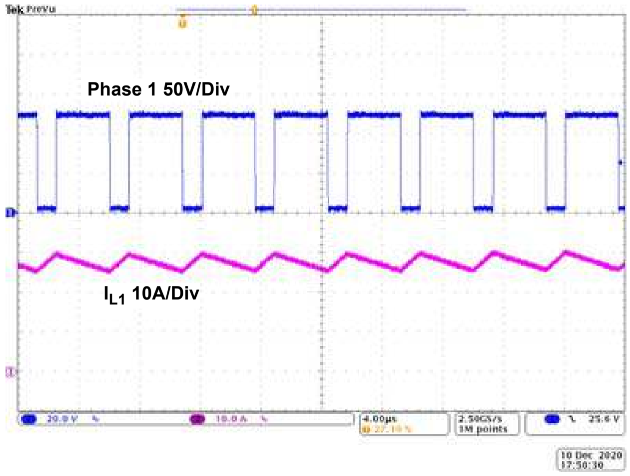
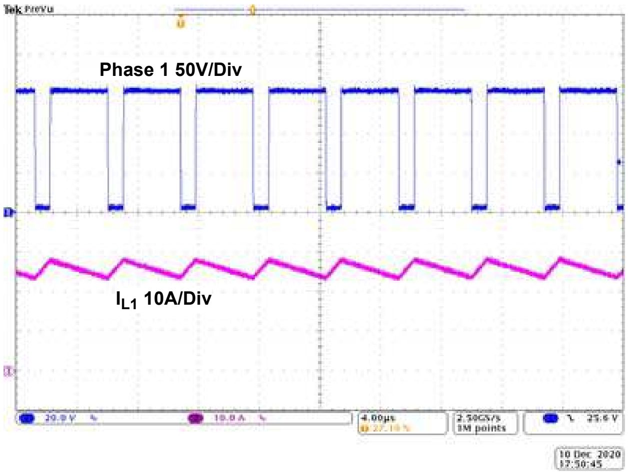


Figure 17. 12V Output Load Regulation, CCM



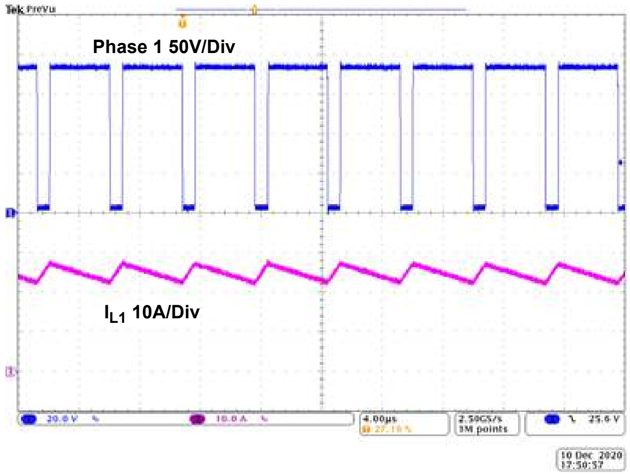
4µs/Div

Figure 18. Phase 1, I_{L1}, V_{IN} = -36V, I_{OUT1} = 20A



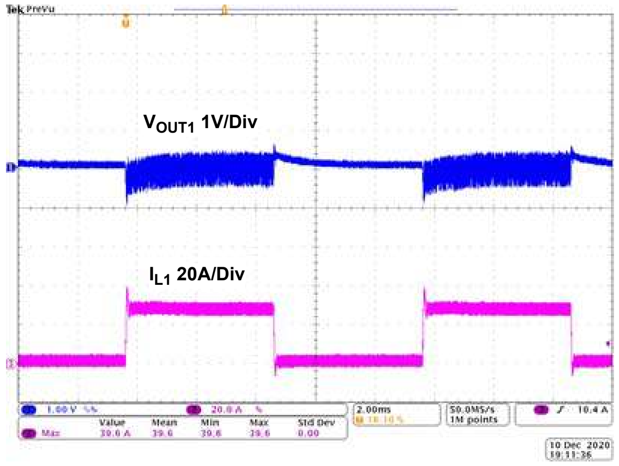
4µs/Div

Figure 19. Phase 1, I_{L1}, V_{IN} = -48V, I_{OUT1} = 20A



4µs/Div

Figure 20. Phase 1, I_{L1}, V_{IN} = -60V, I_{OUT1} = 20A



2ms/Div

Figure 21. 12V Output Load Transient, V_{IN} = -36V, I_{OUT1} = 0A to 20A, 2.5A/µs, CCM

V_{IN} = -48V, V_{OUT1} = 12V, V_{OUT2} = 5V, T_A = 25°C, unless otherwise noted. (Cont.) (Cont.)

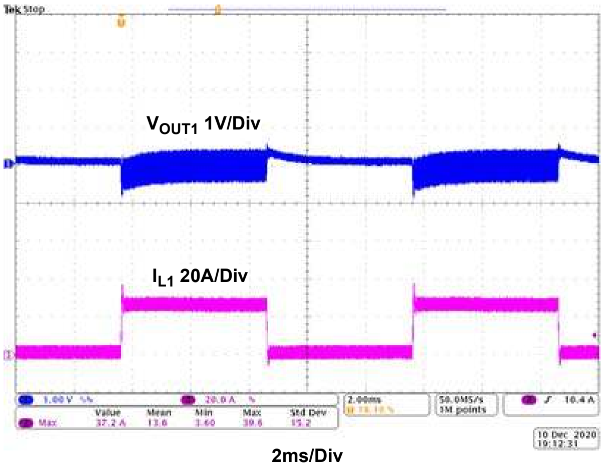


Figure 22. 12V Output Load Transient, V_{IN} = -48V, I_{OUT1} = 0A to 20A, 2.5A/µs, CCM

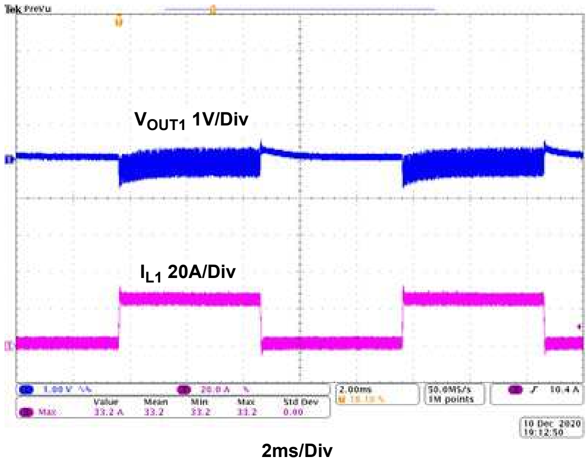


Figure 23. 12V Output Load Transient, V_{IN} = -60V, I_{OUT1} = 0A to 20A, 2.5A/µs, CCM

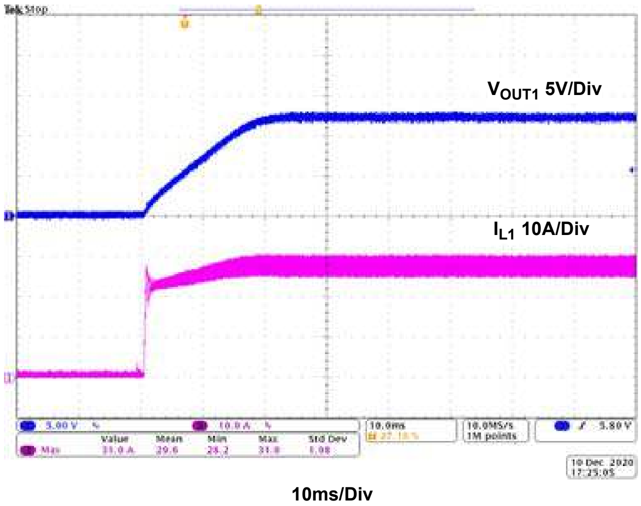


Figure 24. 12V Output Start-Up Waveform, V_{IN} = -36V, I_{OUT1} = 20A, CCM

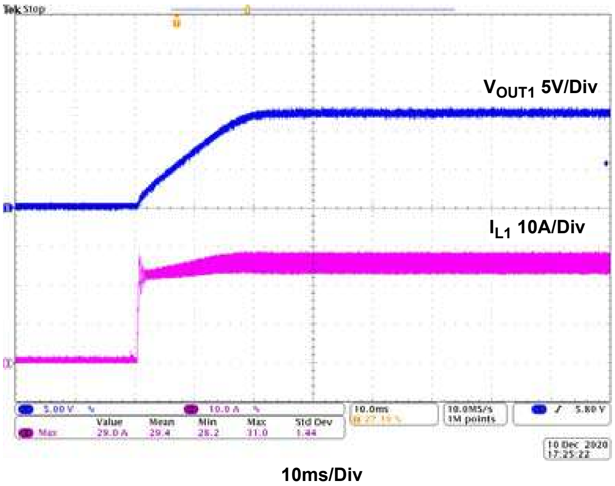


Figure 25. 12V Output Start-Up Waveform, V_{IN} = -48V, I_{OUT1} = 20A, CCM

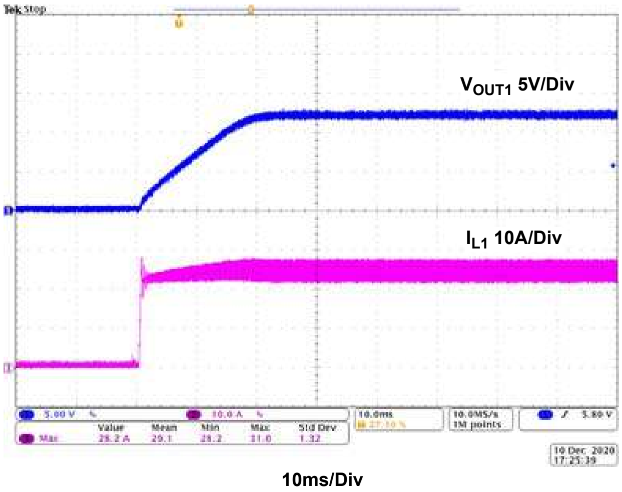


Figure 26. 12V Output Start-Up Waveform, V_{IN} = -60V, I_{OUT1} = 20A, CCM

Figure 27. Output Voltage Ripple, V_{IN} = -48V, I_{OUT1} = 20A

V_{IN} = -48V, V_{OUT1} = 12V, V_{OUT2} = 5V, T_A = 25°C, unless otherwise noted. (Cont.) (Cont.)

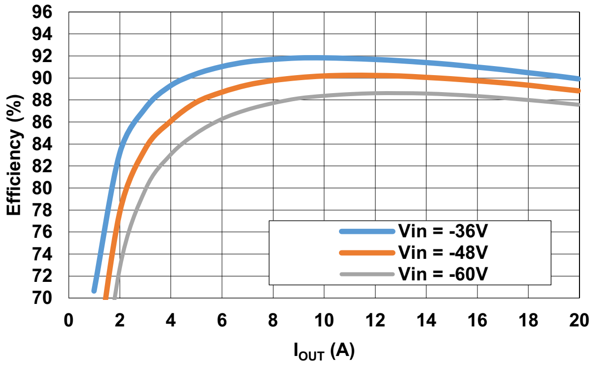


Figure 28. 5V Output Efficiency, CCM

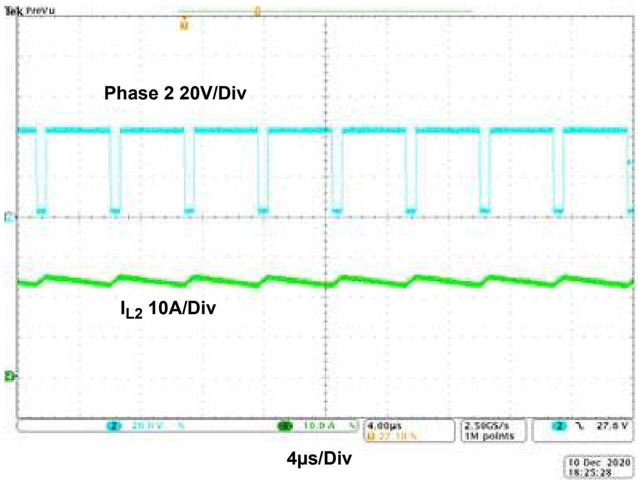


Figure 29. Phase 2, I_{L2}, V_{IN} = -36V, I_{OUT2} = 20A

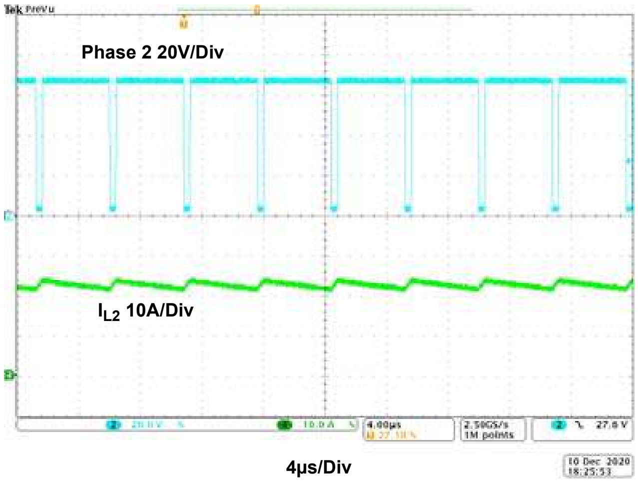


Figure 30. Phase 2, I_{L2}, V_{IN} = -60V, I_{OUT2} = 20A

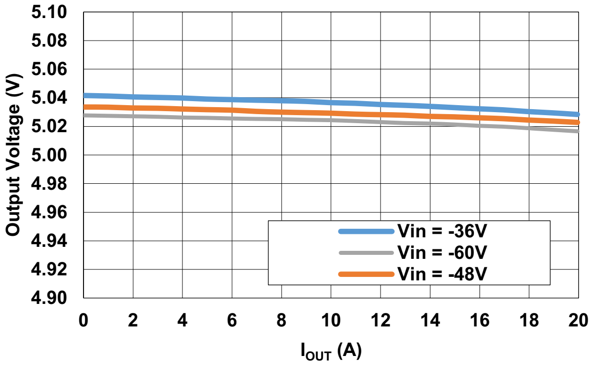


Figure 31. 5V Output Load Regulation, CCM

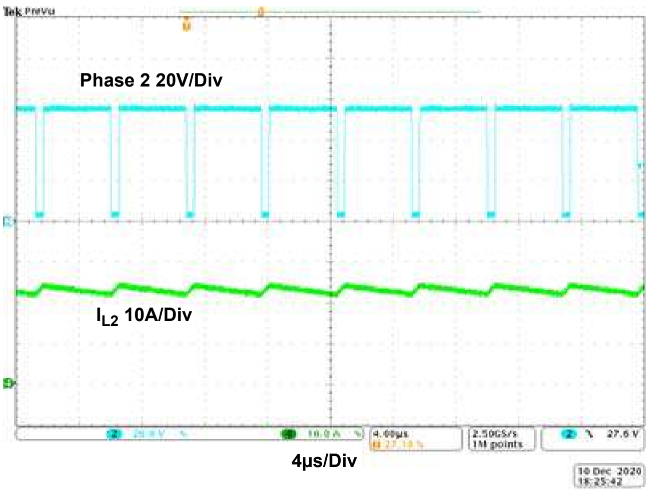


Figure 32. Phase 2, I_{L2}, V_{IN} = -48V, I_{OUT2} = 20A

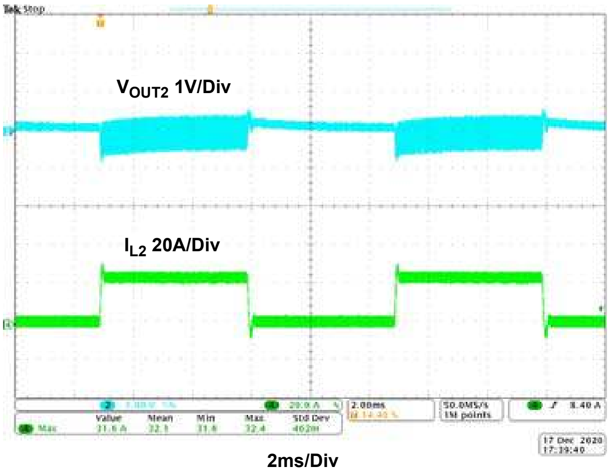


Figure 33. 5V Output Load Transient, V_{IN} = -36V, I_{OUT1} = 0A to 20A, 2.5A/µs, CCM

V_{IN} = -48V, V_{OUT1} = 12V, V_{OUT2} = 5V, T_A = 25°C, unless otherwise noted. (Cont.) (Cont.)

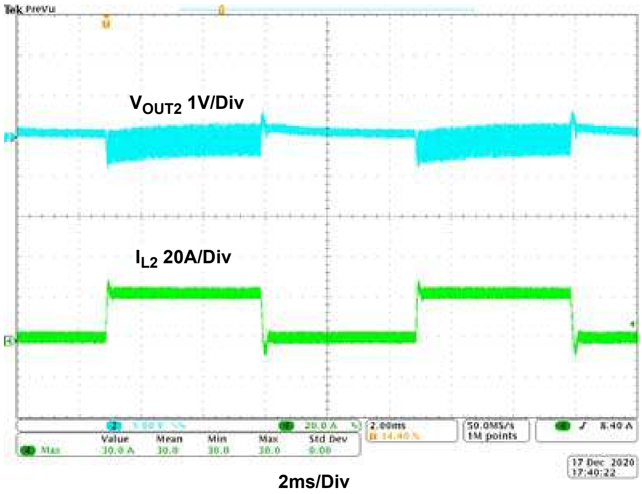


Figure 34. 5V Output Load Transient, V_{IN} = -48V, I_{OUT1} = 0A to 20A, 2.5A/µs, CCM

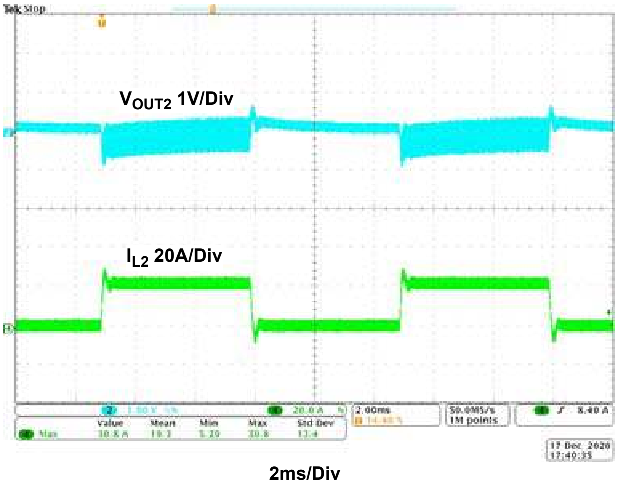


Figure 35. 5V Output Load Transient, V_{IN} = -60V, I_{OUT1} = 0A to 20A, 2.5A/µs, CCM

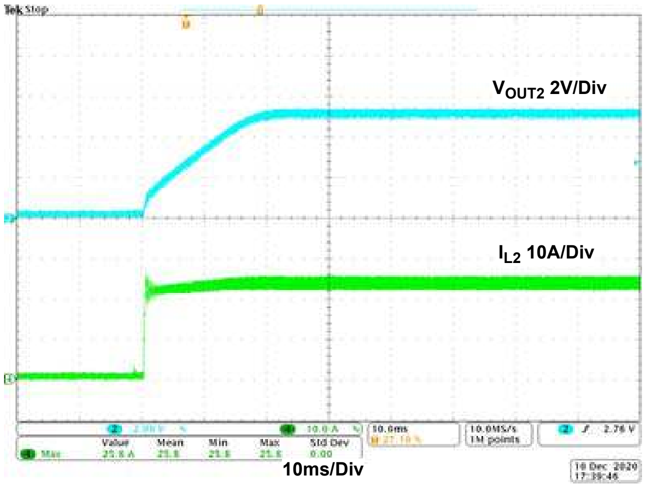


Figure 36. 5V Output Start-Up Waveform, V_{IN} = -36V, I_{OUT1} = 20A, CCM

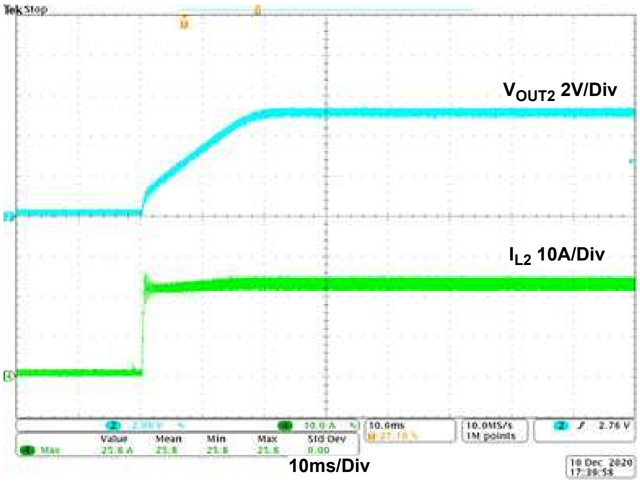


Figure 37. 5V Output Start-Up Waveform, V_{IN} = -48V, I_{OUT1} = 20A, CCM

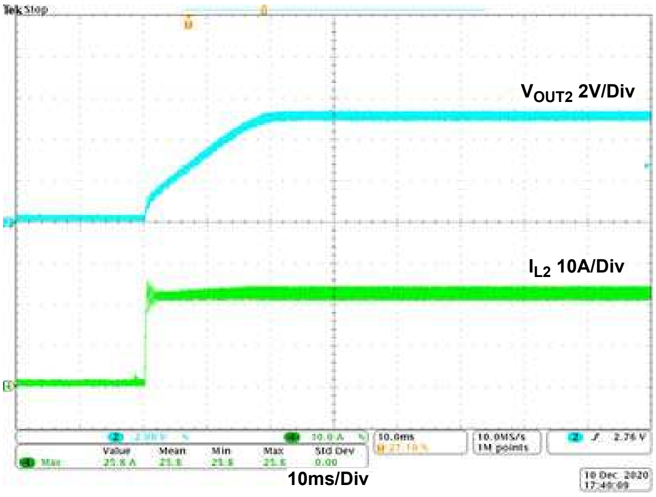


Figure 38. 5V Output Start-Up Waveform, V_{IN} = -60V, I_{OUT1} = 20A, CCM

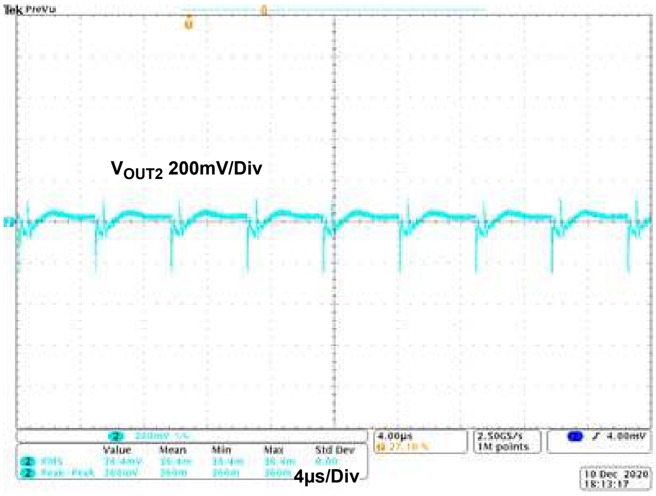


Figure 39. Output Voltage Ripple, V_{IN} = -48V, I_{OUT2} = 20A

4. Ordering Information

Part Number	Description
ISL81805EVAL3Z	High Voltage Dual Boost Controller Evaluation Board

5. Revision History

Revision	Date	Description
1.00	Sep 23, 2021	Initial release

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