FAIRCHILD SEMICONDUCTOR™

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FDG314P

Digital FET, P-Channel

General Description

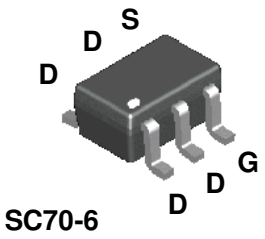
This P-Channel enhancement mode field effect transistor is produced using Fairchild Semiconductor's proprietary, high cell density, DMOS technology. This very high density process is tailored to minimize on-state resistance at low gate drive conditions. This device is designed especially for battery power applications such as notebook computers and cellular phones. This device has excellent on-state resistance even at gate drive voltages as low as 2.5 volts.

Applications

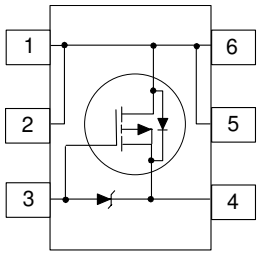
- Power Management
- Load switch
- Signal switch

Features

- -0.65 A, -25 V. $R_{DS(ON)}$ = 1.1 Ω @ V_{GS} = -4.5 V
  $R_{DS(ON)}$ = 1.5 Ω @ V_{GS} = -2.7 V.
- Very low gate drive requirements allowing direct operation in 3V cirucuits ($V_{GS(th)}$ <1.5 V).
- Gate-Source Zener for ESD ruggedness (>6 kV Human Body Model).
- Compact industry standard SC70-6 surface mount package.



SC70-6



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		-25	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current - Continuous	(Note 1a)	-0.65	A
	- Pulsed		-1.8	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.75	W
		(Note 1b)	0.48	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf/1500 Ohm)		6.0	kV

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	260	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.14	FDG314P	7"	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		-19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -20 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-0.65	-0.72	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		2		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -0.5 A V_{GS} = -4.5 V, I_D = -0.5 A @ 125°C V_{GS} = -2.7 V, I_D = -0.25 A		0.77 1.08 1.06	1.1 1.8 1.5	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-1			A
g_{FS}	Forward Transconductance	V_{DS} = -4.5 V, I_D = -0.5 A		0.9		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		63		pF
C_{oss}	Output Capacitance			34		pF
C_{rss}	Reverse Transfer Capacitance			10		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -6 V, I_D = -0.5 A, V_{GS} = -4.5 V, R_{GEN} = 50 Ω		7	20	ns
t_r	Turn-On Rise Time			8	20	ns
$t_{d(off)}$	Turn-Off Delay Time			55	110	ns
t_f	Turn-Off Fall Time			35	70	ns
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -0.25 A, V_{GS} = -4.5 V		1.1	1.5	nC
Q_{gs}	Gate-Source Charge			0.32		nC
Q_{gd}	Gate-Drain Charge			0.25		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.42 A (Note 2)		-0.85	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 170°C/W when mounted on a 1 in^2 pad of 2oz copper.

b) 260°C/W when mounted on a minimum mounting pad.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics

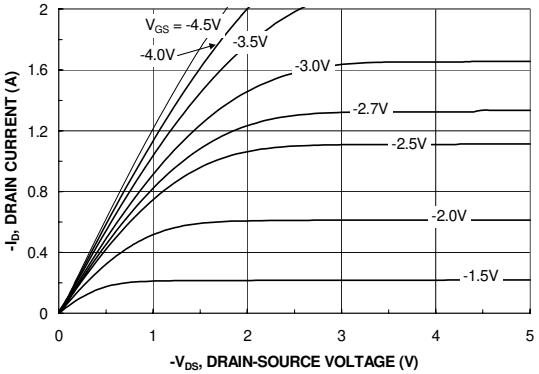


Figure 1. On-Region Characteristics.

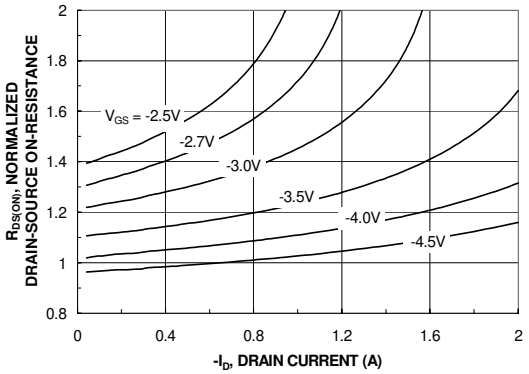


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

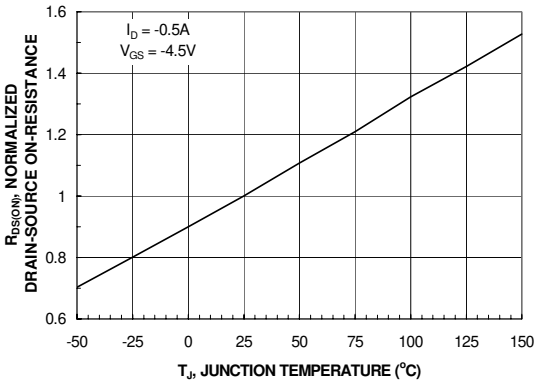


Figure 3. On-Resistance Variation with Temperature.

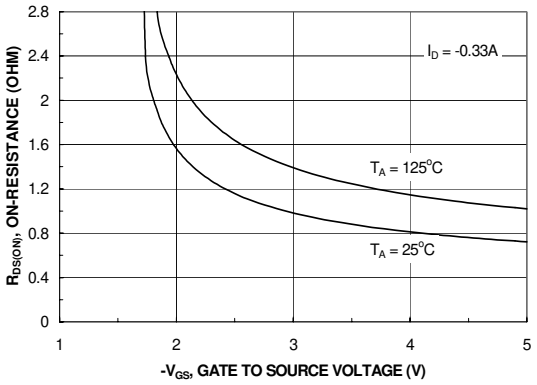


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

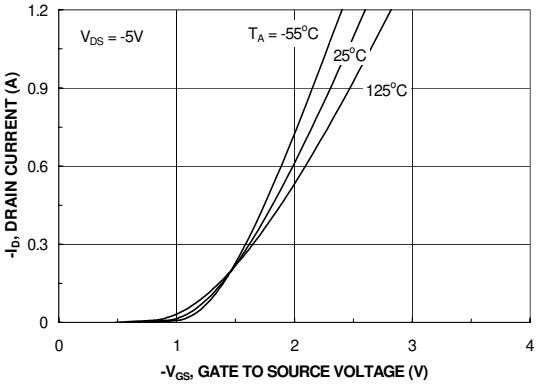


Figure 5. Transfer Characteristics.

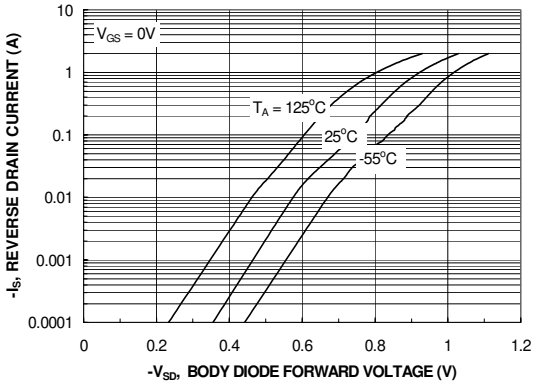


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

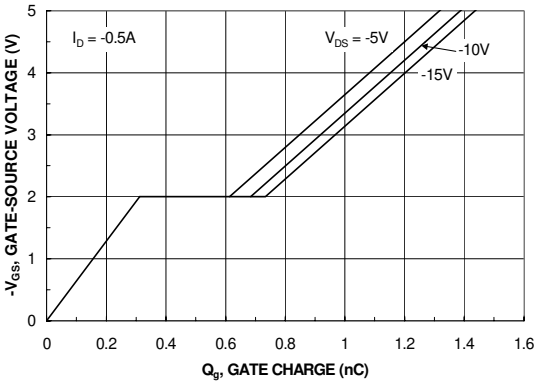


Figure 7. Gate-Charge Characteristics.

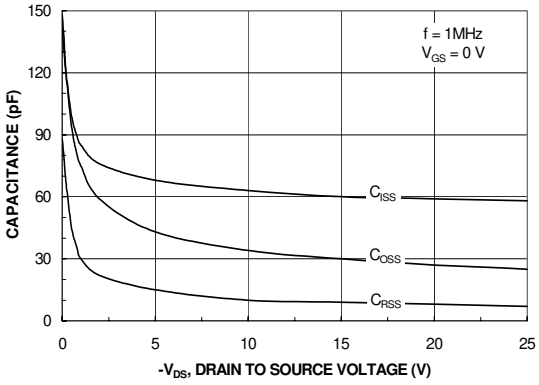


Figure 8. Capacitance Characteristics.

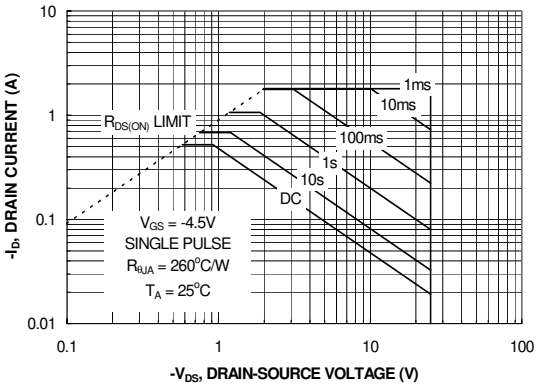


Figure 9. Maximum Safe Operating Area.

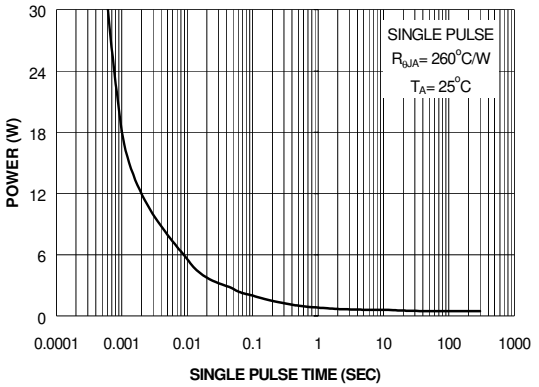


Figure 10. Single Pulse Maximum Power Dissipation.

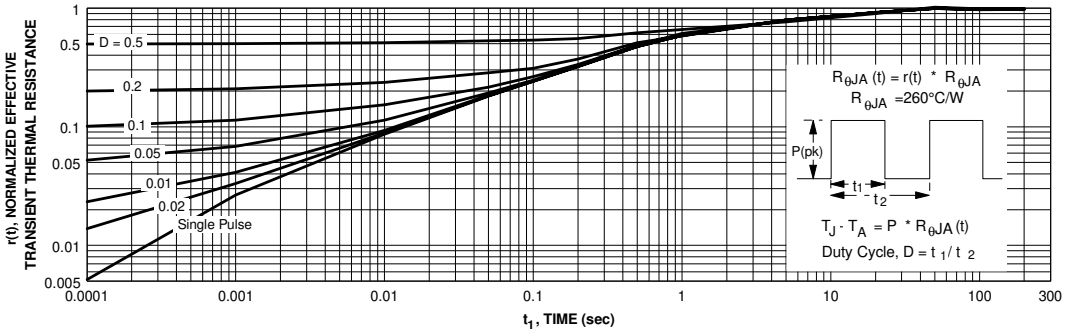


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient themal response will change depending on the circuit board design.

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