Am29C982

4-Bit x 4-Port Multiple Bus Exchange

Advanced Micro Devices

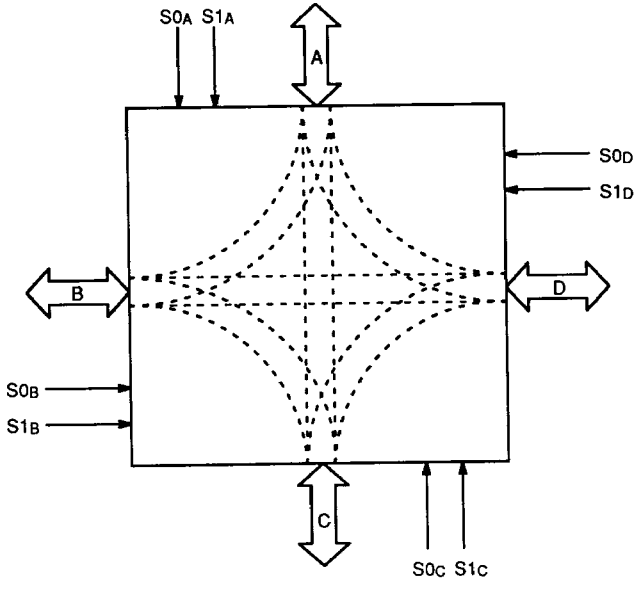
DISTINCTIVE CHARACTERISTICS

- **Four bidirectional I/O ports**
  - Replaces several LS245-type devices
  - TTL Compatibility
  - Permits multiple bus communication
- **Two selection inputs per port**
  - Port-independent interconnect control
- **Matched port decoding**
  - Increased flexibility
  - Simplifies external decode logic
  - Easily cascadable for wider buses
- **Outputs glitch-free during power-up/down**
  - No power-up sequencing needed
  - Ideal for card-edge interface
- **48 mA output drive**
  - High-capacitance bus driving
- **High-performance CMOS**
  - Low power consumption
  - 7 ns (typ.) port-to-port delay
  - 9 ns (typ.) select-to-port delay
- **Available in 400 mil, 28-pin DIP and 28-pin LCC and PLCC packages**

GENERAL DESCRIPTION

The Am29C982 is a high-speed Multiple Bus Exchange device. It is organized as four 4-bit bidirectional I/O ports. Each port can be used either as a source or a destination under independent control to implement a digital cross-point switch. This organization adds data routing flexibility and is ideally suited for multiple bus communication in a multiprocessing environment.

SIMPLIFIED BLOCK DIAGRAM



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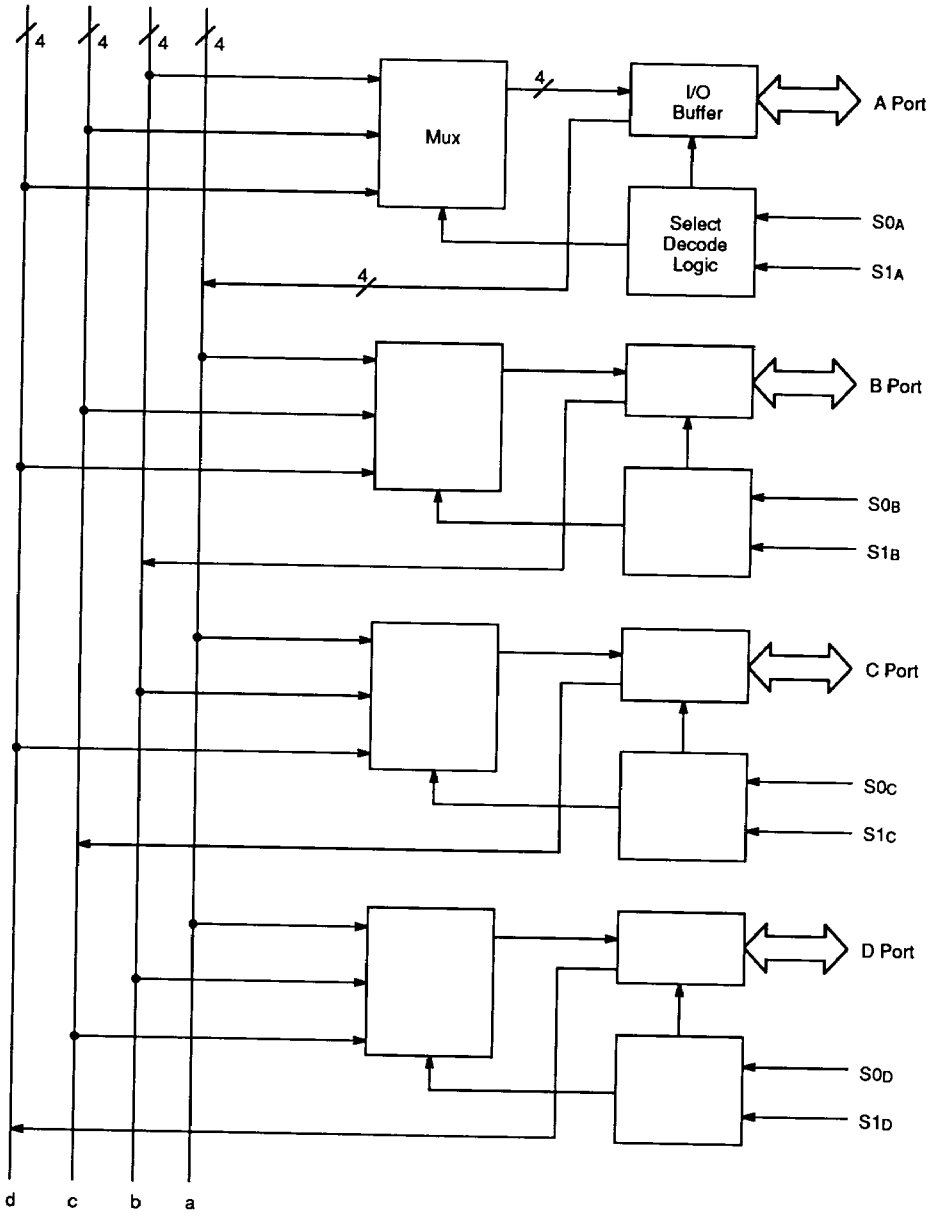
Publication# 09484 Rev. C Amendment/0
Issue Date: October 1990

DETAILED BLOCK DIAGRAM



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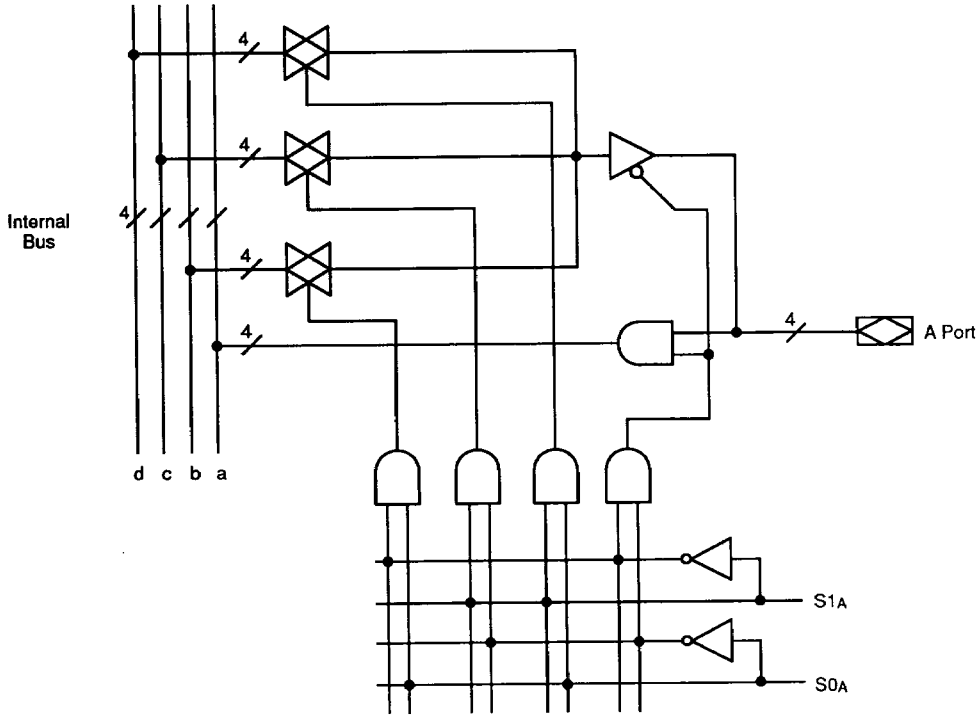
PORT A — DETAILED DIAGRAM



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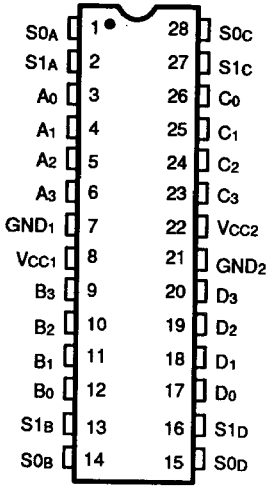
CONNECTION DIAGRAMS
Top View

DIP



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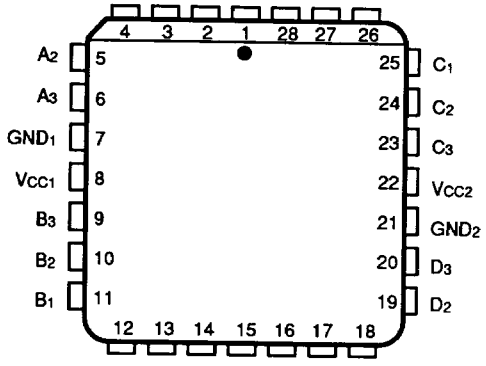
LCC*



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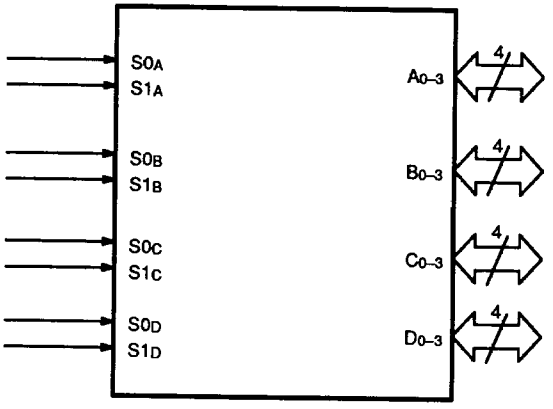
Notes:
Pin 1 is marked for orientation.
*Also available in 28-Pin PLCC; pinout is identical to LCC.

LOGIC SYMBOL



VCC = Power Supply (2)
GND = Ground (2)

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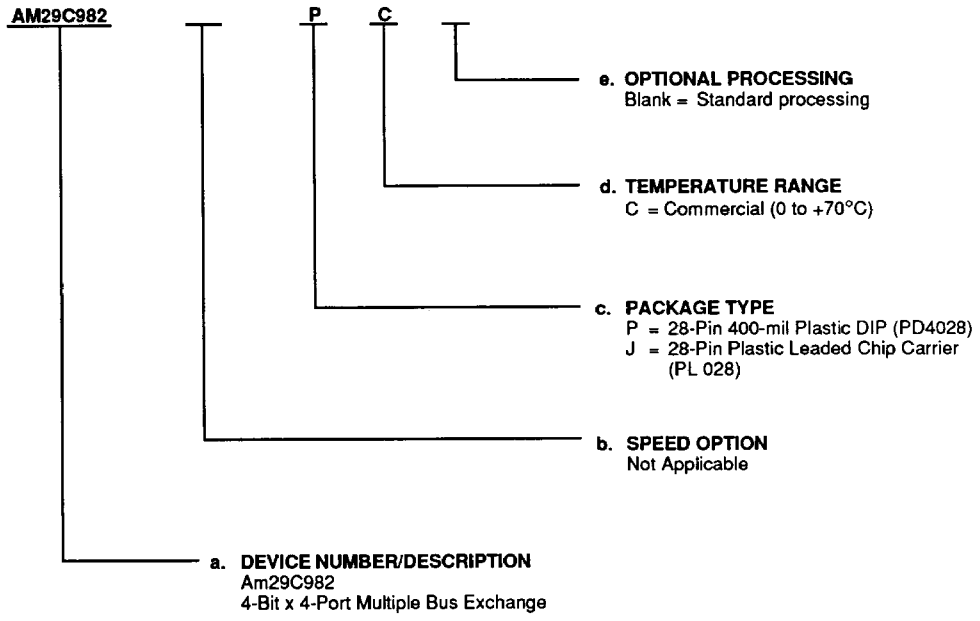
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C982	PC, JC

Valid Combinations

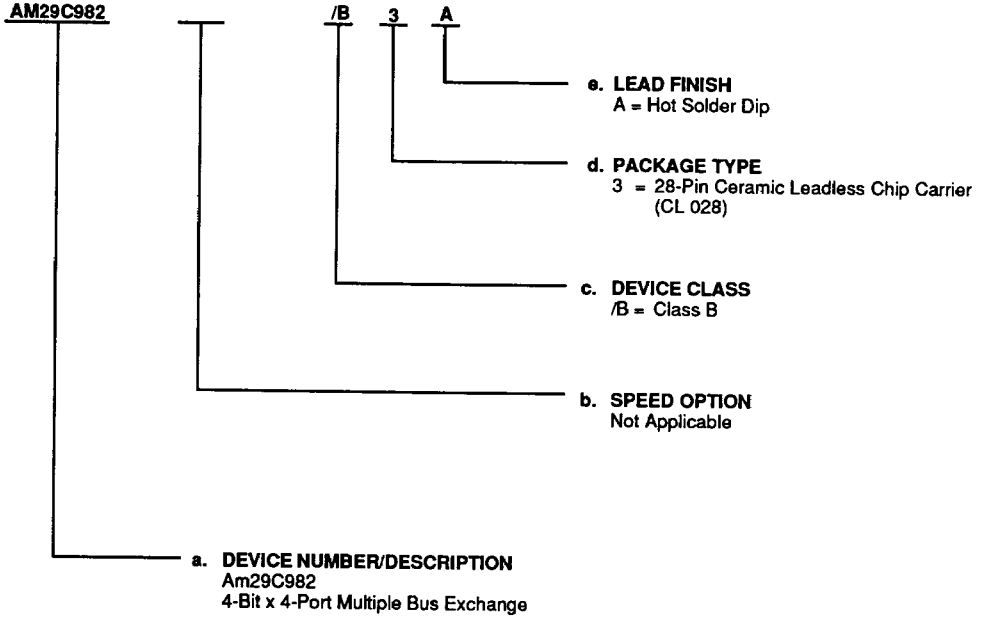
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Device Class**
d. **Package Type**
e. **Lead Finish**



Valid Combinations	
AM29C982	/B3A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A_i, B_i, C_i, & D_i (i = 0-3)

Data Bus I/O Ports (Input/Output)

These four groups of four I/O pins are defined as A, B, C, and D ports respectively. Each port serves as a source (input) or a destination (output). When selected as a source, the output drivers of the port are in the high-impedance state.

Si_A, Si_B, Si_C, & Si_D (i = 0, 1)

Port Select (Inputs)

Each pair of inputs determines the status of its corresponding I/O port as a source (input) or a destination (output). When selected as a destination, the selection inputs determine which port is the source of data.

FUNCTIONAL DESCRIPTION

The Am29C982 Multiple Bus Exchange consists of four 4-bit I/O ports. Each I/O port can either be a source (input) port, or a destination (output) port that accepts data from any one of the three other ports. When the port is an input, its output drivers are in the high-impedance state. The ports that are not intended to be destination ports should be selected as source ports to disable the port.

Independent selection inputs for each port offer flexibility in data routing. Data from one input port can be routed to one or more of the other ports. Two independent channels can also be established by specifying any two ports as sources, and any combination of the other two as destinations.

FUNCTION TABLE

$S1_A$	$S0_A$	A Port Status
L	L	Source
L	H	Destination (B → A)
H	L	Destination (C → A)
H	H	Destination (D → A)
$S1_B$	**$S0_B$**	**B Port Status**
L	L	Destination (A → B)
L	H	Source
H	L	Destination (C → B)
H	H	Destination (D → B)
$S1_C$	**$S0_C$**	**C Port Status**
L	L	Destination (A → C)
L	H	Destination (B → C)
H	L	Source
H	H	Destination (D → C)
$S1_D$	**$S0_D$**	**D Port Status**
L	L	Destination (A → D)
L	H	Destination (B → D)
H	L	Destination (C → D)
H	H	Source

Key:

L = Low

H = High

Destination = Output

Source = Input

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	−0.5 to 7.0 V
DC Input Diode Current	
(I_{IK}) (V_{IN} < 0 V)	−20 mA
(V_{IN} > V_{CC} if applicable)	+20 mA
DC Input Voltage (V_{IN})	−0.5 V to +7.0 V
DC Output Diode Current	
(I_{OK}) (V_{OUT} < 0 V)	−50 mA
(V_{OUT} > V_{CC} if applicable)	+50 mA
DC Output Current Per Output Pin	
I_{SINK}	+70 mA
I_{SOURCE}	−30 mA
DC Output Voltage (V_{OUT})	−0.5 to +7.0 V
Total DC Ground Current (I_{GND})	600 mA
Total DC V_{CC} Current (I_{CC})	220 mA
Storage Temperature	−65 to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to 70°C
Supply Voltage (V_{CC})	4.5 V to 5.5 V

Military (M) Devices

Ambient Temperature (T_A)	−55 to +125°C
Supply Voltage (V_{CC})	4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IL} or V_{IH}	I_{OH} = −15 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	(Note 1)		2.0		V
V_{IL}	Input LOW Voltage	(Note 1)			0.8	V
V_{IC}	Input CLAMP Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
I_{IL}	Input LOW Current	V_{CC} 5.5 V, V_{IN} = 0 V			−10	µA
	(Select Inputs)	V_{CC} 5.5 V, V_{IN} = 0.4 V			−5	µA
I_{IH}	Input HIGH Current	V_{CC} 5.5 V, V_{IN} = 2.7 V			5	µA
	(Select Inputs)	V_{CC} 5.5 V, V_{IN} = 5.5 V			10	µA
I_{OZL}	Off-State Leakage Current	V_{CC} = 5.5 V, V_{OUT} = 0.4 V			−15	µA
	(I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 0 V			−20	µA
I_{OZH}	Off-State Leakage Current	V_{CC} = 5.5 V, V_{OUT} = 2.7 V			15	µA
	(I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 5.5 V			20	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−60		mA
$I_{CC(Q)}$	Quiescent Power Supply	V_{CC} = 5.5 V, V_{IN} = 5.5 V or	MIL		1.5	mA
	(Note 4)	GND Outputs Open	COM'L		1.2	mA

DC CHARACTERISTICS (Continued)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
$I_{CC}(T)$	Power Supply Current TTL	V_{CC} = 5.5 V, V_{IN} = 3.4 V	MIL		1.5	mA/ Input
	Input HIGH (Note 4)	Other Inputs at V_{CC} or GND	COM'L		1.3	
$I_{CC}(D)$ (Note 5)	Dynamic Power Supply Current (Note 4)	V_{CC} = 5.5 V, Outputs Open One Output Toggling (Note 3)			400	µA/ MHz/Bit

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration of short-circuit test not to exceed 100 milliseconds.
3. Measured at a frequency of <10 MHz with 50% duty cycle. Unused inputs are at V_{CC} or GND.
4. Calculation of total device I_{CC}:

$$I_{CC} = I_{CC}(Q) + I_{CC}(T) \times M_T \times D_H + I_{CC}(D) \times ((C_L + 72) + 72) \times f \times N$$

Where C_L = Load Capacitance in pF per output
f = Frequency in MHz
N = Average number of outputs switching
M_T = Number of inputs at logic HIGH
D_H = Duty cycle for each input HIGH

5. Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Test Conditions	Commercial		Military		Unit
				Min.	Max.	Min.	Max.	
1	t_{PLH}	Propagation Delay Data	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		14		16	ns
2	t_{PHL}	Input to Data Output			14		16	ns
3	t_{PLH}	Propagation Delay Select			15		17	ns
4	t_{PHL}	Input to Data Output			15		17	ns
5	t_{PZH}	Output Enable Time Select			15		17	ns
6	t_{PZL}	Input to Data Output			15		17	ns
7	t_{PHZ}	Output Disable Time Select			14		16	ns
8	t_{PLZ}	Input to Data Output			14		16	ns

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

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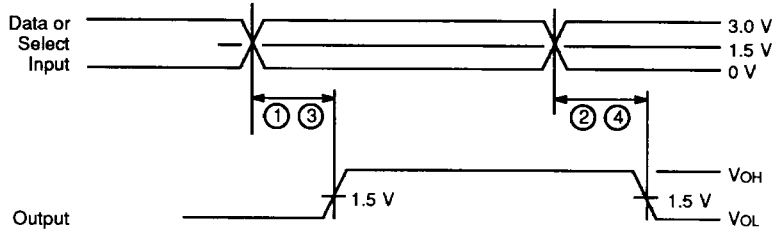
SWITCHING TEST WAVEFORMS



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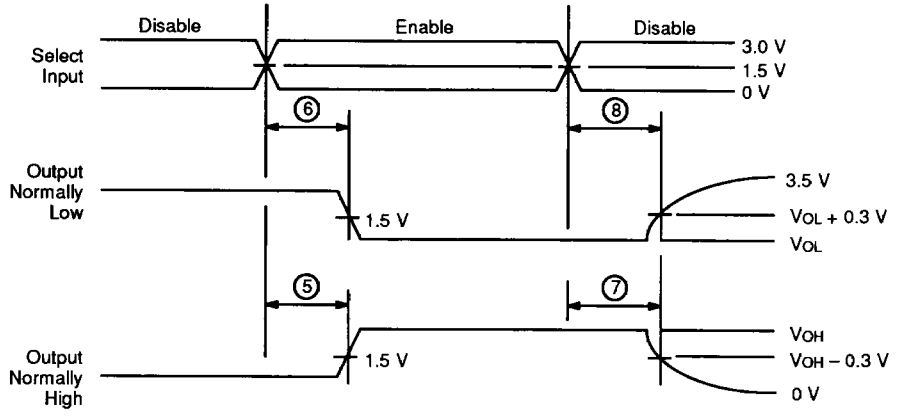
Propagation Delay



Enable and Disable Times

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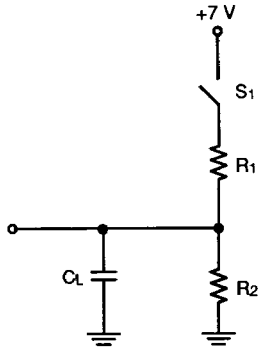
SWITCHING TEST CIRCUIT



S_1 = Open Normally
S_1 = Closed for t_{PZL} and t_{PLZ}

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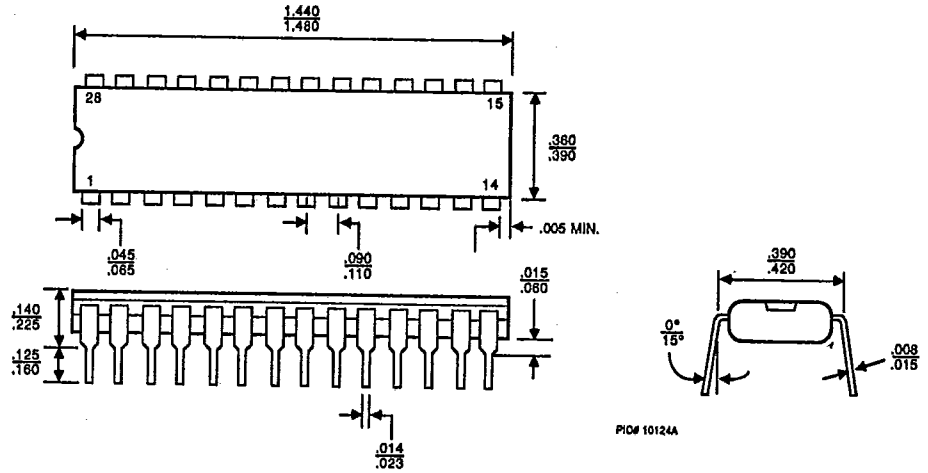

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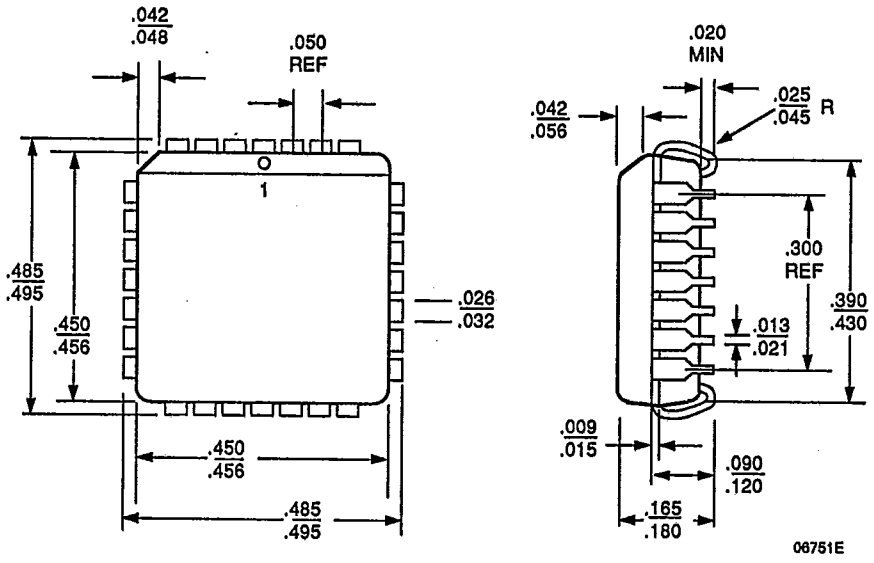

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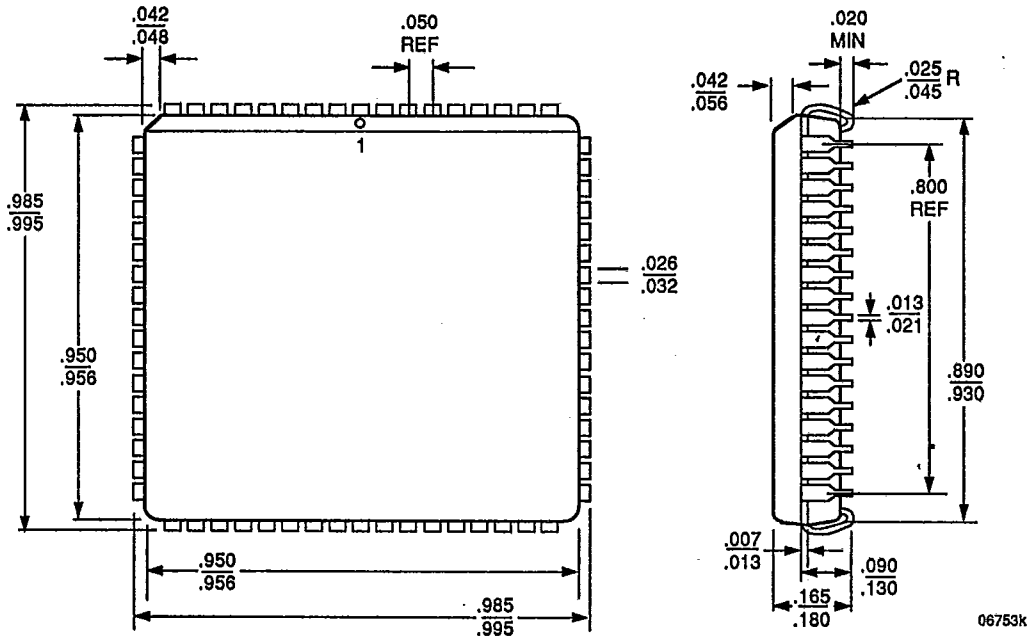
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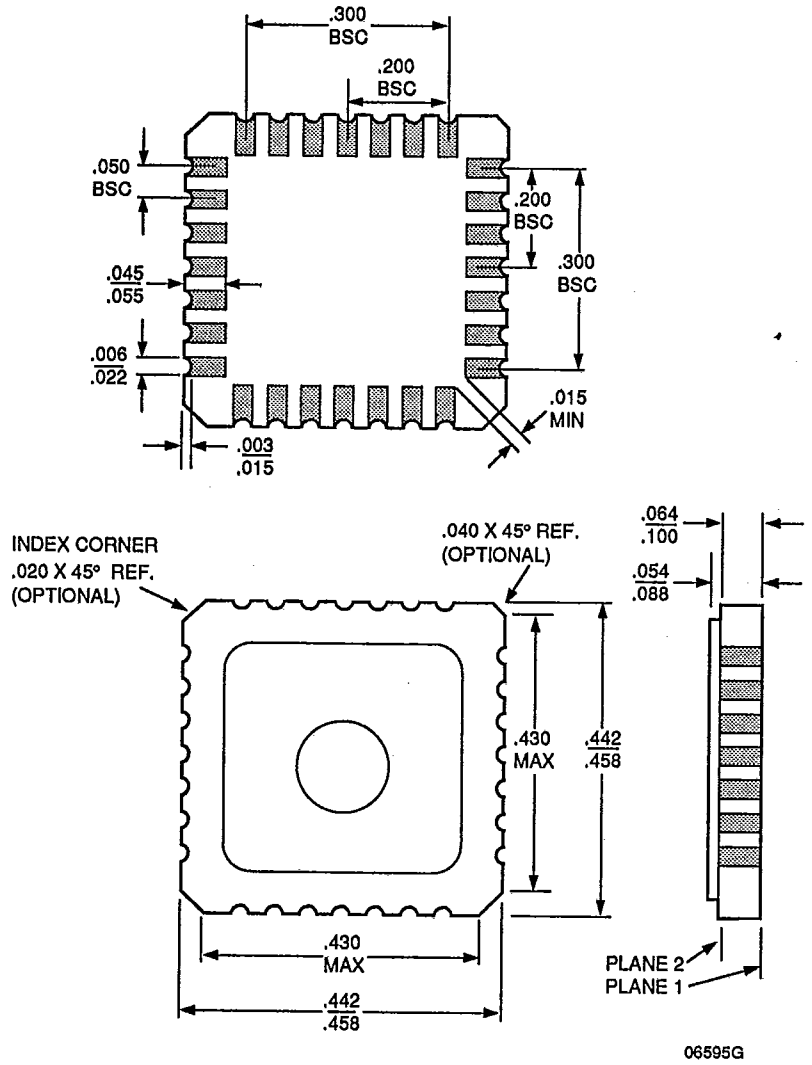
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