

General Description

The MAX9720 stereo headphone amplifier combines Maxim's DirectDrive architecture and SmartSense™, an automatic mono/stereo detection feature. Conventional headphone amplifiers require a bulky DC-blocking capacitor between the headphone and the amplifier. DirectDrive produces a ground-referenced output from a single supply, eliminating the need for large DCblocking capacitors, saving cost, board space, and component height.

SmartSense automatically detects the presence of a short at either the left or right amplifier output. Under a fault condition, the shorted output is automatically disabled and the stereo input signal is automatically mixed and routed to the remaining active channel. This feature is useful in cell phone and PDA applications where a variety of headphone jacks with unknown loads can be inserted into the headphone jack socket. SmartSense prevents both damage to the amplifier and eliminates battery drain into a shorted load.

The MAX9720 delivers up to 50mW per channel into a 16Ω load and has an ultra-low 0.003% THD+N. A high (92dB at 217kHz) power-supply rejection ratio (PSRR) allows the device to operate from noisy digital supplies without additional power conditioning. The gain of the MAX9720 is set internally, further reducing component count. Two gain options are available (-1V/V, MAX9720A and -1.41V/V, MAX9720B). The headphone outputs include a comprehensive click-and-pop circuitry that eliminates audible glitches on startup and shutdown. A shutdown mode provides a fast 250µs turn-on time.

The MAX9720 operates from a single 1.8V to 3.6V supply and consumes only 5mA of supply current. The MAX9720 also features thermal overload protection, and is specified over the extended -40°C to +85°C temperature range. The MAX9720 is available in a tiny (2mm x 2mm x 0.6mm) 16-bump chip-scale package (UCSP™) and a 16-pin TSSOP package.

Applications

PDAs Smart Phones Cellular Phones Tablet PCs

MP3 Players Portable Audio Equipment

Notebook PCs

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Pin Configuration and Typical Application Circuit appear at end of data sheet.

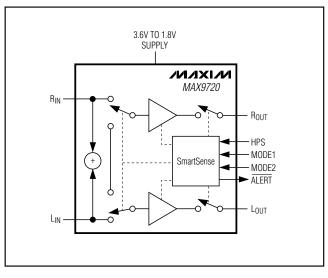
Features

- ♦ DirectDrive Eliminates Bulky DC-Blocking **Capacitors**
- ♦ SmartSense Automatic Short Detection
- ♦ Low 5mA Quiescent Current
- ◆ Fixed Gain Eliminates External Feedback Network MAX9720A: -1V/V MAX9720B: -1.41V/V
- **♦** 50mW per Channel Output Power
- ♦ Ultra-Low 0.003% THD+N
- ♦ High PSRR (92dB at 217Hz)
- **♦ Integrated Click-and-Pop Suppression**
- ♦ 1.8V to 3.6V Single-Supply Operation
- **♦ Thermal Overload Protection**
- ♦ Available in Space-Saving Packages 16-Bump UCSP (2mm x 2mm x 0.6mm) 16-Pin TSSOP

Ordering Information

PART	TEMP RANGE	PIN/BUMP- PACKAGE	GAIN (V/V)
MAX9720AEBE-T	-40°C to +85°C	16 UCSP-16	-1
MAX9720BEBE-T	-40°C to +85°C	16 UCSP-16	-1.41
MAX9720AEUE	-40°C to +85°C	16 TSSOP	-1
MAX9720BEUE	-40°C to +85°C	16 TSSOP	-1.41

Simplified Block Diagram



MIXIM

Maxim Integrated Products 1

ABSOLUTE MAXIMUM RATINGS

0.3V to +0.3V	Output Shor
0.3V to +0.3V	Continuous
0.3V to +4V	16-Bump l
4V to +0.3V	16-Pin TSS
$(SV_{SS} - 0.3V)$ to $(V_{DD} + 0.3V)$	Junction Ter
PGND - 0.3V) to (V _{DD} + 0.3V)	Operating To
V _{SS} - 0.3V) to (PGND + 0.3V)	Storage Ten
0.3V to +4V	Bump Temp
0.3V to (V _{DD} + 0.3V)	Reflow
0.3V to (V _{DD} + 0.3V)	Lead Tempe

Output Short Circuit to GND or VDD	Continuous
Continuous Power Dissipation (T _A = +70°C)	
16-Bump UCSP (derate 8.2mW/°C above +70°C	C)659mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C)	754.7mW
Junction Temperature	+150°C
Operating Temperature Range	40°C to +85°C
Storage Temperature Range6	5°C to +150°C
Bump Temperature (soldering)	
Reflow	+235°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{DD} = V_{MODE1} = V_{MODE2} = 3.0V, PGND = SGND = 0V, R_L = \infty, C1 = C2 = 2.2\mu F. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)$

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL	•			1			
Supply Voltage Range	V_{DD}	Inferred from PSRR to	est	1.8		3.6	V
Company	1	Stereo mode			5	8.4	A
Supply Current	I _{DD}	Mono mode (MODE1 :	= V _{DD} , MODE2 = GND)		3		mA
Shutdown Supply Current	ISHDN	MODE1 = MODE2 =	GND		6	10	μΑ
Turn-On/Turn-Off Time	ts				250		μs
CHARGE PUMP							,
Oscillator Frequency	fosc			272	320	368	kHz
HEADPHONE AMPLIFIERS							
Voltago Cain	۸	MAX9720A		-1.02	-1	-0.98	V/V
Voltage Gain	Av	MAX9720B		-1.443	-1.415	-1.386	
Gain Match	ΔΑγ	Between OUTL and OUTR			±1		%
Total Output Offset Voltage	V/00	MAX9720A		-5	-0.8	+3.6	mV
(Note 3)	Vos	MAX9720B		-6.5	-1	+4.5	IIIV
Input Resistance	R _{IN}			10	15	20	kΩ
		$1.8V \le V_{DD} \le 3.6V$ (Note 3)	DC	76	92		
Power-Supply Rejection Ratio	PSRR	V _{DD} = 3.0V, 200mV _{P-P} ripple (Note 3)	f _{RIPPLE} = 217Hz		92		dB
			fRIPPLE = 1kHz		86		
			fRIPPLE = 20kHz		61		
Output Power	Роит	THD+N = 1%, f _{IN} =	$R_L = 32\Omega$		50		mW
Output Power		$1kHz$, $T_A = +25$ °C	$R_L = 16\Omega$	32	50		11100

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD} = V_{MODE1} = V_{MODE2} = 3.0V, PGND = SGND = 0V, R_L = \infty, C1 = C2 = 2.2\mu F. T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25$ °C.) (Note 1)

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus	THD+N	for the lar	$R_L = 32\Omega$, $P_{OUT} = 30$ mW		0.003		%
Noise	I HD+N	$f_{IN} = 1kHz$	$R_L = 16\Omega,$ $P_{OUT} = 30mW$		0.005		70
Signal-to-Noise Ratio	SNR	$f_{IN} = 1kHz, V_{OUT}$ BW = 22Hz to 22	= 0.5 V_{RMS} , R_L = 16 Ω		97		dB
Slew Rate	SR				0.8		V/µs
Maximum Capacitive Load	CL	No sustained osc	illations		150		рF
Crosstalk		$R_L = 32\Omega$, $P_{OUT} =$	= 1mW, f _{IN} = 10kHz		75		dB
Thermal Shutdown Threshold					140		°C
Thermal Shutdown Hysteresis					15		°C
SmartSense	,			•			
Shorted Load Threshold	Rsms			2.4	4	5.6	Ω
Pulse Duration	tsms				3.1		μs
DEBOUNCE TIME (TIME)		•		•			
TIME Charging Current	ITIME			0.7	1.1	1.8	μA
TIME Discharge Switch Resistance	R _{TIME}	HPS = GND		4		10	kΩ
TIME Threshold	VTIME			1	1.1	1.2	V
HEADPHONE SENSE INPUT (_						I.
		VIH		0.9 x V _{DD}			
HPS Threshold		VIL				0.7 x V _{DD}	V
Input Leakage Current	IIГ	MODE1= MODE2	? = GND			±1	μΑ
Input Capacitance	CIN				10		рF
ALERT							
Output Current High	Гон	V _{ALERT} = V _{DD}				1	μΑ
Output Voltage Low	V _{OL}	$I_{OL} = 3mA$				0.4	V
MODE_ INPUT				<u> </u>			
MODE TO A LA		VIH		0.7 x V _{DD}			.,,
MODE_ Thresholds		VIL				0.3 x V _{DD}	V
MODE_ Input Leakage Current						±1	μΑ

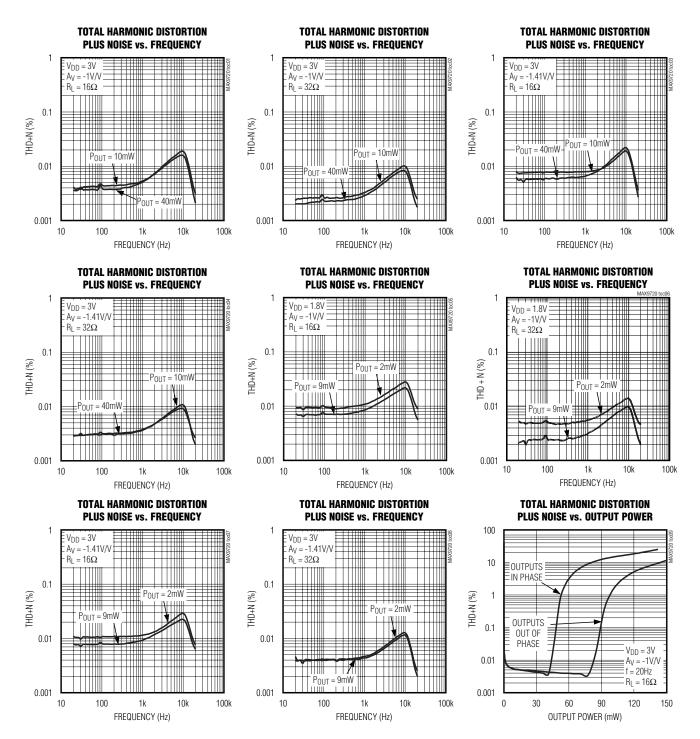
Note 1: All specifications are 100% tested at $T_A = +25^{\circ}C$; temperature limits are guaranteed by design.

Note 2: Inputs are AC-coupled to ground.

Note 3: Inputs are connected directly to ground.

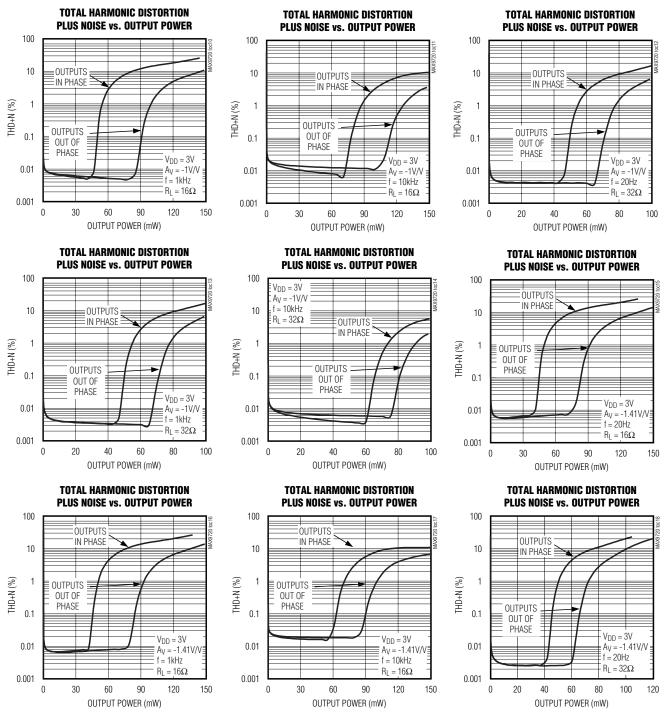
Typical Operating Characteristics

 $(V_{DD} = 3V, THD+N bandwidth = 22Hz to 22kHz, MODE1 = MODE2 = V_{DD}.)$



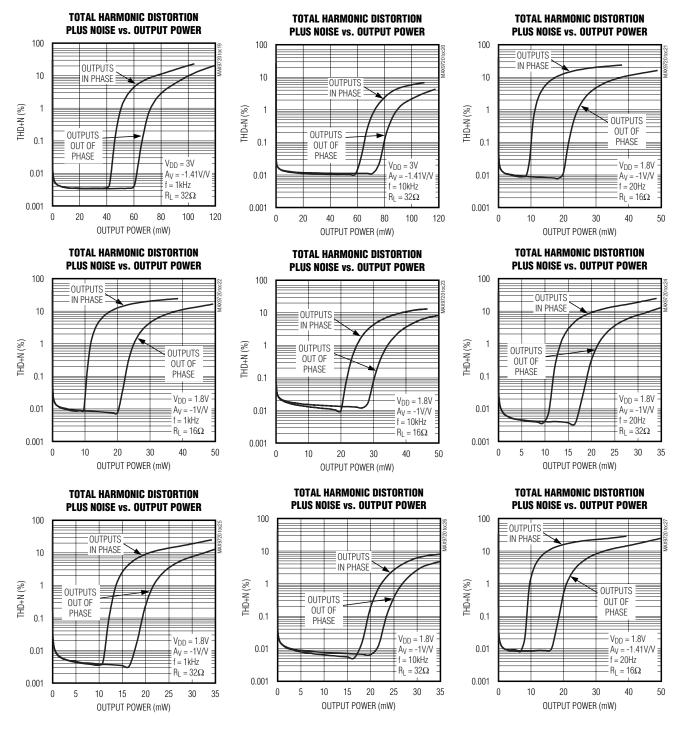
Typical Operating Characteristics (continued)

(V_{DD} = 3V, THD+N bandwidth = 22Hz to 22kHz, MODE1 = MODE2 = V_{DD}.)



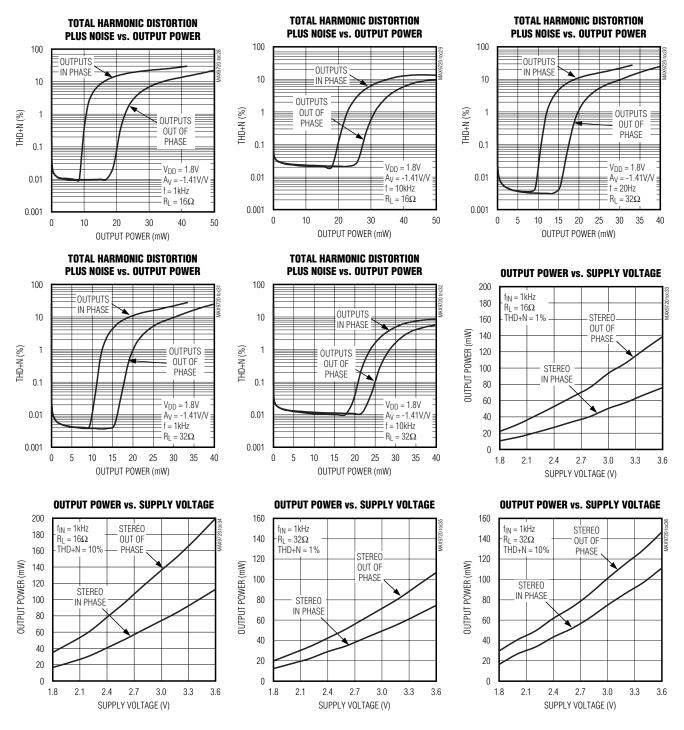
Typical Operating Characteristics (continued)

 $(V_{DD} = 3V, THD+N bandwidth = 22Hz to 22kHz, MODE1 = MODE2 = V_{DD}.)$



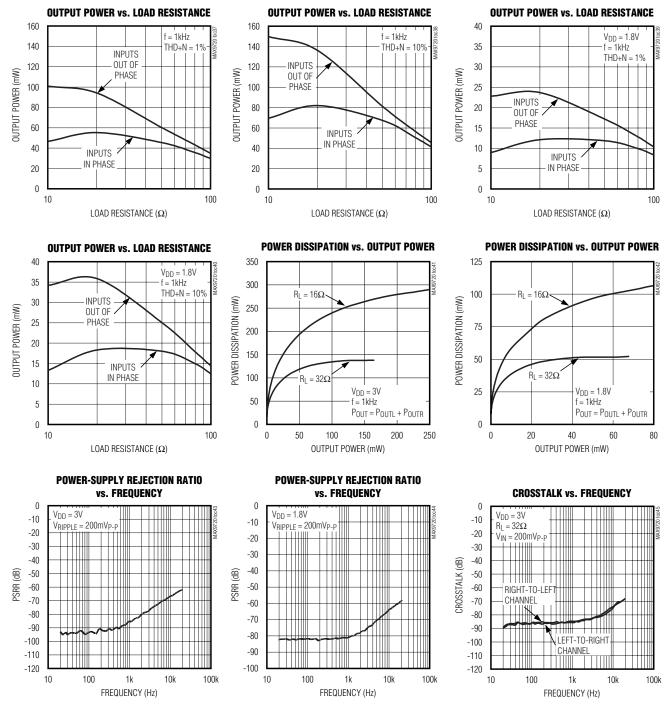
Typical Operating Characteristics (continued)

(V_{DD} = 3V, THD+N bandwidth = 22Hz to 22kHz, MODE1 = MODE2 = V_{DD}.)



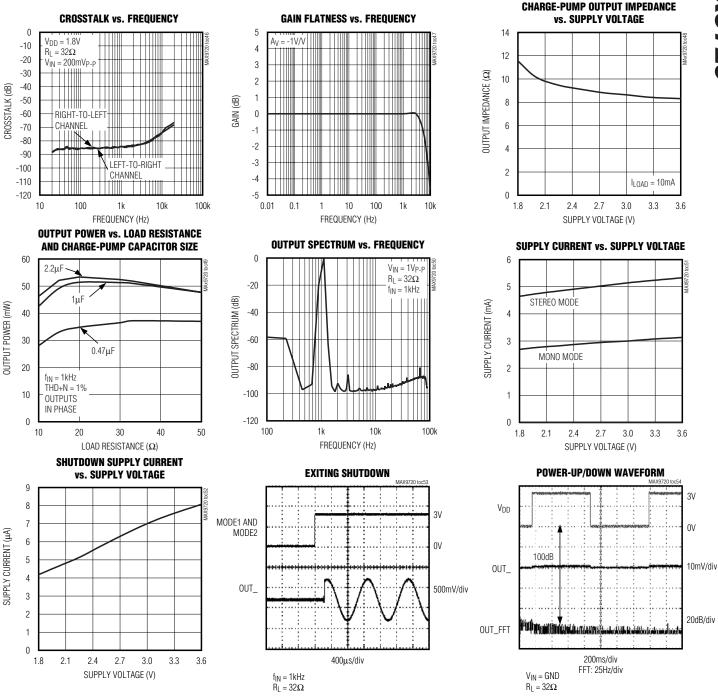
Typical Operating Characteristics (continued)

 $(V_{DD} = 3V, THD+N bandwidth = 22Hz to 22kHz, MODE1 = MODE2 = V_{DD}.)$



Typical Operating Characteristics (continued)

 $(V_{DD} = 3V, THD+N bandwidth = 22Hz to 22kHz, MODE1 = MODE2 = V_{DD}.)$



Pin Description

PIN	BUMP		FUNCTION	
TSSOP	UCSP	NAME	FUNCTION	
1	D2	V _{DD}	Positive Power Supply	
2	C2	MODE1	Mode Select 1 Logic Input	
3	D1	C1P	Flying Capacitor Positive Terminal	
4	C1	PGND	Power Ground. Connect to SGND.	
5	B1	C1N	Flying Capacitor Negative Terminal	
6	A1	PVss	Charge-Pump Output	
7	B2	MODE2	Mode Select 2 Logic Input	
8	A2	ALERT	Open-Drain Interrupt Logic Output	
9	A3	INL	Left-Channel Audio Input	
10	В3	TIME	Debouncing Timer Capacitor	
11	A4	INR	Right-Channel Audio Input	
12	B4	SGND	Signal Ground. Connect to PGND.	
13	C4	SV _{SS}	Amplifier Negative Power Supply. Connect to PV _{SS} .	
14	D4	OUTR	Right-Channel Output	
15	C3	HPS	Headphone Sense Input	
16	D3	OUTL	Left-Channel Output	

Detailed Description

The MAX9720 fixed-gain, stereo headphone amplifier includes Maxim's DirectDrive architecture and SmartSense. DirectDrive eliminates the large output-coupling capacitors required by conventional single-supply headphone amplifiers. SmartSense automatically detects the presence of a short at either output. Under a fault condition, the shorted output is automatically disabled and the stereo input signal is automatically mixed and routed to the remaining active channel. This prevents damage to the amplifier and optimizes power savings by eliminating battery drain into a shorted load.

The device consists of two 50mW Class AB headphone amplifiers, an internal feedback network (MAX9720A: fixed -1V/V gain, MAX9720B: fixed -1.41V/V gain), a mono mixer/attenuator, undervoltage lockout (UVLO)/ shutdown control, SmartSense, a charge pump, and comprehensive click-and-pop suppression circuitry (see *Functional Diagram*). The charge pump inverts the positive supply (VDD), creating a negative supply (PVss). The headphone amplifiers operate from these bipolar supplies with their outputs biased about GND (Figure 1). The amplifiers have almost twice the supply range compared to other single-supply amplifiers, nearly quadrupling the available output power. The benefit of the GND bias is that the amplifier outputs do not have a DC component (typically VDD/2). This elimi-

nates the large DC-blocking capacitors required with conventional headphone amplifiers, conserving board space, system cost, and improving frequency response.

The noninvasive SmartSense feature of the MAX9720 detects a short on either output. The SmartSense routine executes when the device is powered up or brought out of shutdown (see the *SmartSense* section). If a fault is detected, the shorted channel is shut down, the output goes high impedance, and the stereo audio input is mixed/attenuated and fed to the remaining active channel. The device also features an $\overline{\text{ALERT}}$ output that indicates to a host μC that SmartSense has detected a short-circuit condition on either amplifier output.

Forced stereo and forced mono modes can also be selected through the two MODE_ inputs. In forced operation mode, SmartSense is disabled and the device operates as specified by the MODE_ inputs, regardless of output load conditions. A fast low-power shutdown mode is also selected through the MODE_ inputs (see the *Mode_ Selection* section).

The UVLO prevents operation from an insufficient power supply and click-and-pop suppression, which eliminates audible transients on startup and shutdown. Additionally, the MAX9720 features thermal overload protection and can withstand $\pm 4 \text{kV}$ ESD strikes on the output.

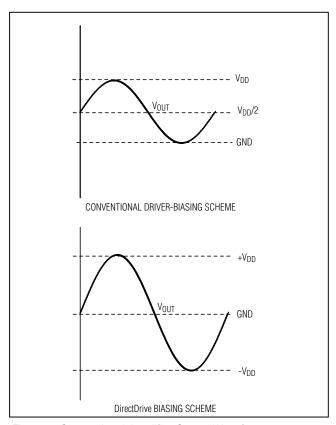


Figure 1. Conventional Amplifier Output Waveform vs. MAX9720 Output Waveform

DirectDrive

Conventional single-supply headphone amplifiers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the MAX9720 output to be biased about GND, almost doubling dynamic range while operating from a single supply. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large capacitors (220µF typ), the MAX9720 charge pump requires only two, small ceramic capacitors (1µF typ), conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Charge-Pump

Capacitance and Load Resistance graph in the *Typical Operating Characteristics* for details of the possible capacitor sizes.

Previous attempts to eliminate the output-coupling capacitors involved biasing the headphone return (sleeve) to the DC bias voltage of the headphone amplifiers. This method raised some issues:

- The sleeve is typically grounded to the chassis.
 Using this biasing approach, the sleeve must be isolated from system ground, complicating product design.
- During an ESD strike, the amplifier's ESD structures are the only path to system ground. The amplifier must be able to withstand the full ESD strike.
- When using the headphone jack as a line out to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in large ground-loop current and possible damage to the amplifiers.
- When using a combination microphone and speaker headset (in a cell phone or PDA application), the microphone typically requires a GND return. Any DC bias on the sleeve conflicts with the microphone requirements (Figure 2).

Low-Frequency Response

In addition to the cost and size disadvantages, the DC-blocking capacitors limit the low-frequency response of the amplifier and distort the audio signal:

 The impedance of the headphone load and the DCblocking capacitor form a highpass filter with the -3dB point determined by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

where R_L is the impedance of the headphone and C_{OUT} is the value of the DC-blocking capacitor.

The highpass filter is required by conventional single-ended, single-supply headphone amplifiers to block the midrail DC component of the audio signal from the headphones. Depending on the -3dB point, the filter can attenuate low-frequency signals within the audio band. Larger values of C_{OUT} reduce the attenuation, but are physically larger, more expensive capacitors. Figure 3 shows the relationship between the size of C_{OUT} and the resulting low-frequency attenuation. Note that the -3dB point for a 16 Ω headphone with a 100 μ blocking capacitor is 100Hz, well within the audio band.

 The voltage coefficient of the capacitor, the change in capacitance due to a change in the voltage across the capacitor, distorts the audio signal. At frequencies around the -3dB point, the reactance of the capacitor dominates, and the voltage coefficient appears as frequency-dependent distortion. Figure 4 shows the THD+N introduced by two different capacitor dielectrics. Note that around the -3dB point, THD+N increases dramatically.

The combination of low-frequency attenuation and frequency-dependent distortion compromises audio reproduction. DirectDrive improves low-frequency reproduction in portable audio equipment that emphasizes low-frequency effects such as multimedia laptops and MP3, CD, and DVD players.

Charge Pump

The MAX9720 features a low-noise charge pump. The 320kHz switching frequency is well beyond the audio range, and does not interfere with the audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. Limiting the switching speed of the charge pump minimizes the di/dt noise caused by the parasitic bond wire and trace inductance. Although not typically required, additional high-frequency ripple attenuation can be achieved by increasing the size of C2 (see *Typical Application Circuit*).

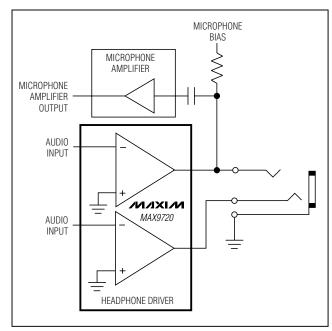


Figure 2. Earbud Speaker/Microphone Combination Headset Configuration

SmartSense

The SmartSense feature detects a short on either output and automatically reconfigures the MAX9720 for optimum power savings. If an output short circuit is detected during the SmartSense routine, the shorted channel is disabled, $\overline{\text{ALERT}}$ is asserted, and the device is set to mono mode (assuming the other channel is not shorted). SmartSense works by applying an inaudible 3µs test voltage pulse to the load. The resulting current from the test pulse and load is sensed. If the load impedance is less than $4\Omega,$ the output is determined to be a short.

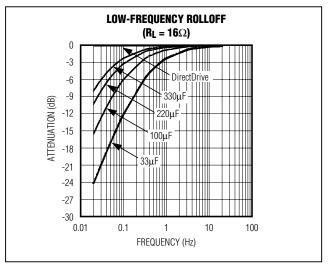


Figure 3. Low-Frequency Attenuation of Common DC-Blocking Capacitor Values

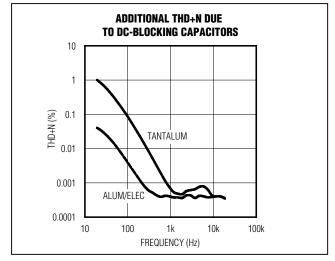


Figure 4. Distortion Contributed by DC-Blocking Capacitors

Mode Selection (MODE)

SmartSense is controlled by the two mode select inputs, MODE1 and MODE2. Table 1 shows the operating modes in relation to the status of the MODE_ inputs. When MODE1 = MODE2 = low, the device is in lowpower shutdown mode. When MODE1 = high and MODE2 = low, the device is in forced mono mode. The right channel is disabled, OUTR goes high impedance, and the stereo audio input is mixed, and the audio signal is reproduced on OUTL. SmartSense is disabled in this mode. When MODE1 = low and MODE2 = high, the device is in forced stereo mode, and SmartSense is disabled. When the device detects the presence of a short BEFORE forced stereo mode is selected, the device remains in mono mode (Figure 5). When MODE1 = MODE2 = high, the device is in automatic detection mode; the operating mode of the device is determined by SmartSense.

MODE1 is also used to execute a host-controlled SmartSense routine and reset the ALERT output. On the rising edge of MODE1, the device invokes a SmartSense routine. The falling edge of MODE1 resets the ALERT output to its idle state.

Automatic Detection Mode

A fault condition is defined as a short (under 4Ω) on either amplifier output to ground. SmartSense automatically detects and disables the shorted output. The mixer/attenuator combines the two stereo inputs (INL and INR), attenuates the resultant signal by a factor of 2, and redirects the audio playback to the remaining active channel. This allows for full reproduction of a stereo signal through a single headphone while maintaining optimum headroom. The mixed mono signal is output only on the properly loaded channel. If both outputs are shorted then both outputs go into a high-impedance state and no audio playback occurs. In automatic detection mode (MODE1 = MODE2 = high),

Table 1. MAX9720 Operating Modes

MODE1	MODE2	SmartSense	OPERATING MODE
High	High	Enabled	Automatic detection mode
Low	Low	Disabled	Shutdown
High	Low	Disabled	Forced left mono
Low	High	Disabled	Forced stereo
	High	Enabled	Host controlled
7	Х	_	Reset ALERT

any of the following events trigger a SmartSense test sequence:

- HPS rises above 0.8 x V_{DD}, indicating a headphone iack has been inserted into the socket.
- The 180mA high-side (sourcing) overcurrent threshold is approached, and the output is near GND.
- The die temperature exceeds the thermal limit (+140°C).
- Power or shutdown is cycled.

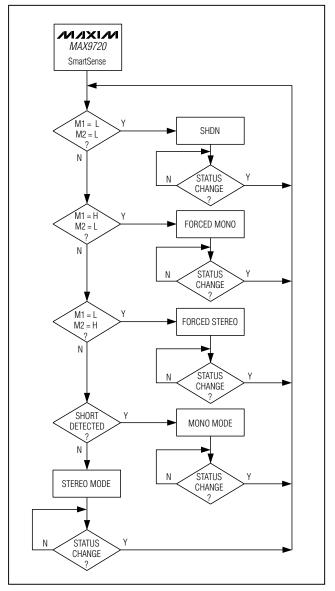


Figure 5. SmartSense Flow Diagram

For automatic headphone detection, connect HPS to the control pin of a 3-wire headphone jack, as shown in Figure 7. With no headphone present, the output impedance of the amplifier pulls HPS to less than 0.8 x VDD. When a headphone plug is inserted into the jack, the control pin is disconnected from the tip contact, and HPS is pulled to VDD through the internal $100k\Omega$ pullup. A debounce delay controls the time between HPS going high and the initiation of the SmartSense test sequence. This time is controlled by an external capacitor on the TIME pin and allows the user to customize the debounce time (see the *TIME Capacitor* section).

Shutdown

Driving MODE1 and MODE2 to GND shuts down the MAX9720, disconnects the internal HPS pullup resistor, disables the charge pump and amplifiers, sets the amplifier output impedance to $1k\Omega$, and reduces supply current to less than $6\mu A$.

Forced Mono Mode

In forced left mono mode (MODE1 = high, MODE2 = low), the right channel is disabled and OUTR goes high impedance. The stereo signal inputs are combined through the mixer/attenuator and output on the left channel. In forced mono mode, the SmartSense routine is disabled.

Forced Stereo Mode

In forced stereo mode (MODE1 = low, MODE2 = high), the device operates as a stereo headphone amplifier. In forced stereo mode, the SmartSense routine is disabled.

ALERT Output

The MAX9720 includes an active-low, open-drain ALERT output that indicates to the master device that SmartSense has detected a fault condition. ALERT triggers when an output short circuit is detected through the SmartSense routine. During normal operation, ALERT idles high. If a fault condition is detected, ALERT pulls the line low. ALERT remains low until MODE1 is toggled from high to low.

Click-and-Pop Suppression

In conventional single-supply audio amplifiers, the output-coupling capacitor is a major contributor of audible clicks and pops. Upon startup, the amplifier charges the coupling capacitor to its bias voltage, typically half the supply. Likewise, during shutdown, the capacitor is discharged to GND. A DC shift across the capacitor results, which in turn appears as an audible transient at the speaker. Since the MAX9720 does not require output-coupling capacitors, no audible transient occurs.

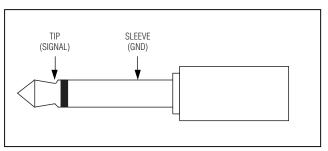


Figure 6. Typical 2-Wire (Mono) Headphone Plug

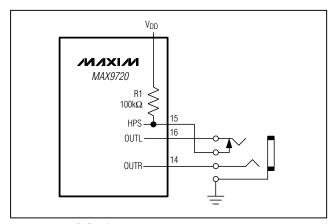


Figure 7. HPS Configuration

Additionally, the MAX9720 features extensive click-andpop suppression that eliminates any audible transient sources internal to the device. The Power-Up/Down Waveform in the *Typical Operating Characteristics* shows that there are minimal spectral components in the audible range at the output upon startup and shutdown

In most applications, the preamplifier output driving the MAX9720 has a DC bias of typically half the supply. During startup, the input-coupling capacitor is charged to the preamplifier's DC bias voltage through the input resistor of the MAX9720, resulting in a DC shift across the capacitor and an audible click/pop. Delaying the startup of the MAX9720 by 4 to 5 time constants (80ms to 100ms) based on R_{IN} and C_{IN}, relative to the startup of the preamplifier, eliminates this click/pop caused by the input filter.

If the SmartSense routine occurs during normal operation, a low-level audible transient may be heard. To prevent this, a host-controlled SmartSense routine should only be executed when ALERT asserts.

Applications Information

Power Dissipation

Under normal operating conditions, linear power amplifiers can dissipate a significant amount of power. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* section under Continuous Power Dissipation or can be calculated by the following equation:

$$P_{\text{DISSPKG(MAX)}} = \frac{T_{\text{J(MAX)}} - T_{\text{A}}}{\theta_{\text{JA}}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section. For example, θ_{JA} of the TSSOP package is +106.38°C/W.

The MAX9720 has two power dissipation sources: the charge pump and the two amplifiers. If the power dissipation for a given application exceeds the maximum allowed for a given package, either reduce V_{DD}, increase load impedance, decrease the ambient temperature, or add heat sinking to the device. Large output traces improve the maximum power dissipation in the package.

Thermal overload protection limits total power dissipation in the MAX9720. When the junction temperature exceeds +140°C, the thermal protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by 15°C, resulting in a pulsing output under continuous thermal overload conditions.

Output Power

The MAX9720 is specified for the worst-case condition—when both inputs are in phase. Under this condition, the amplifiers simultaneously draw current from the charge pump, leading to a slight loss in headroom of Vss. In typical stereo audio applications, the left and right signals present differences in both magnitude and phase, subsequently leading to an increase in the maximum attainable output power. Figure 8 shows the two extreme cases for in- and out-of-phase. In reality, the available power lies between these extremes.

Powering Other Circuits from a Negative Supply

An additional benefit of the MAX9720 is the internally generated, negative supply voltage (PVss). PVss is the negative supply for the MAX9720 headphone amplifiers. PVss can power other devices within a system. Limit the current drawn from PVss to 5mA. Exceeding this affects the operation of the headphone amplifiers. A typical application is a negative supply to adjust the contrast of LCD modules.

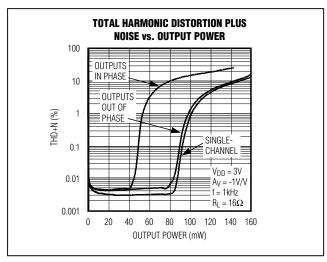


Figure 8. THD+N vs. Output Power with Inputs In-/Out-of-Phase

The charge-pump voltage at PVss is roughly proportional to V_{DD} and is not a regulated voltage. Consider the charge-pump output impedance when powering other devices from PVss. See the Charge-Pump Output Impedance graph in the *Typical Operating Characteristics*. Use 2.2µF charge-pump capacitors for the highest output power; 1µF or lower capacitors can also be used for most applications. See the Output Power vs. Load Resistance and Charge-Pump Capacitance graph for details of the output power vs. capacitor size.

Component Selection

Input Filtering

The input capacitor (C_{IN}), in conjunction with the MAX9720 input impedance, forms a highpass filter that removes the DC bias from an incoming signal (see *Typical Application Circuit*). The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

 $R_{\mbox{\scriptsize IN}}$ is the amplifier's internal input impedance value given in the Electrical Characteristics. Chose $C_{\mbox{\scriptsize IN}}$ such that $f_{\mbox{\scriptsize -3dB}}$ is well below the lowest frequency of interest. Setting $f_{\mbox{\scriptsize -3dB}}$ too high affects the amplifier's low-frequency response. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Table 2. Suggested Capacitor Manufacturers

SUPPLIER	PHONE	FAX	WEBSITE
Taiyo Yuden	800-348-2498	847-925-0899	www.t-yuden.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than $100m\Omega$ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric. Table 2 lists suggested manufacturers.

Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the charge pump's load regulation and output impedance. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. In most applications, 1µF for both C1 and C2 provides adequate performance. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance to an extent. See the Output Power vs. Charge Pump Capacitance and Load Resistance graph in the *Typical Operating Characteristics*. Above 2.2µF, the on-resistance of the switches and the ESR of C1 and C2 dominate.

Hold Capacitor (C2)

The hold capacitor value and ESR directly affect the ripple on PVss. Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output impedance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the Typical Operating Characteristics.

Power-Supply Bypass Capacitor

The power-supply bypass capacitor (C3) lowers the output impedance of the power supply and reduces the impact of the MAX9720's charge-pump switching transients. Bypass V_{DD} with C3, the same value as C1, and place it physically close to the device.

TIME Capacitor

The TIME capacitor (CTIME) sets the HPS debounce time. The debounce time is the delay between HPS exceeding 0.8 x V_{DD} and the execution of the SmartSense routine. The delay ensures that any excessive contact bounce caused by the insertion of a headphone plug into the jack does not cause HPS to register an invalid state (Figure 9). The value of the CTIME in nF equals the nominal delay time in ms, i.e., CTIME = 10nF = tDELAY = 10ms. CTIME values in the 200nF to 600nF range are recommended.

Adding Volume Control

The addition of a digital potentiometer provides simple, digital volume control. Figure 10 shows the MAX9720 with the MAX5408 dual log taper digital potentiometer used as an input attenuator. Connect the high terminal of the MAX5408 to the audio input, the low terminal to GND, and the wiper to $C_{\rm IN}$. Setting the wiper to the top position passes the audio signal unattenuated. Setting the wiper to the lowest position fully attenuates the input.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Connect PGND and SGND together at a single point on the PC board. Connect all components associated with the charge pump (C2 and C3) to the PGND plane. Connect PVss and SVss together at the device. Bypassing of both the positive and negative supplies is accomplished by the charge-pump capacitors, C2 and C3 (see *Typical Application Circuit*). Place capacitors C1 and C3 as close to the device as possible. Place capacitor C2 as close to PVss as possible. Route PGND and all traces that carry switching transients away from SGND, traces, and components in the audio signal path.

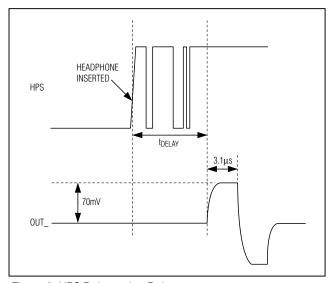
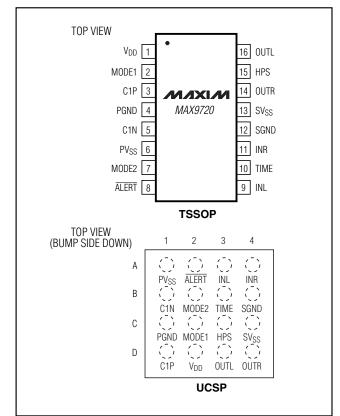


Figure 9. HPS Debouncing Delay

LEFT AUDIO 5 HO INPUT 6 LO WOA 7 P INL OUTL MAX5408 RIGHT AUDIO 12 H1 INPUT 11 L1 11 L1 INR OUTR 14

Figure 10. MAX9720 and MAX5408 Volume Control Circuit

Pin Configurations



UCSP Applications Information

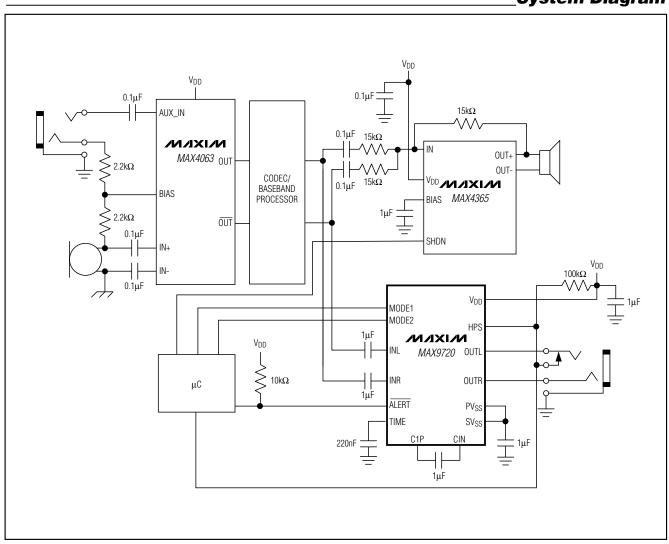
For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and the recommended reflow temperature profile, as well as the latest information on reliability testing results, go to Maxim's website at www.maxim-ic.com/ucsp and look up Application Note: UCSP—A Wafer-Level Chip-Scale Package.

_Chip Information

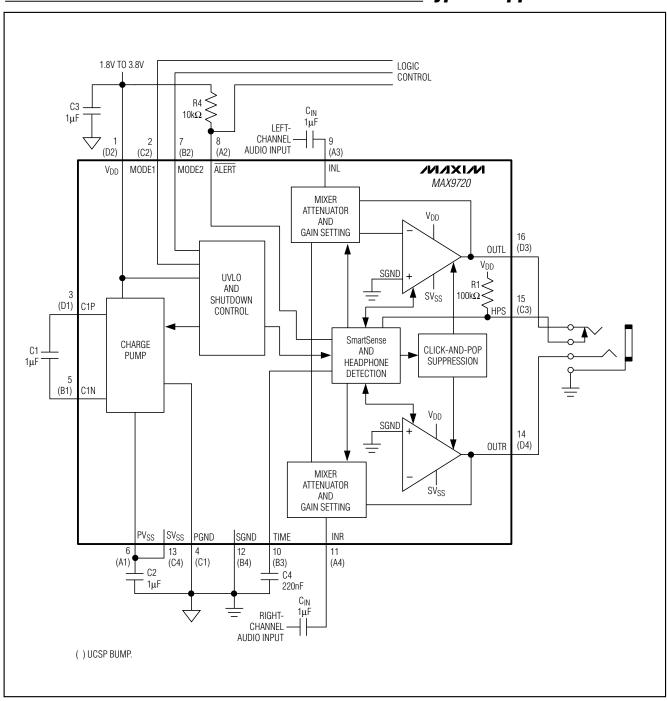
TRANSISTOR COUNT: 4858

PROCESS: BiCMOS

System Diagram

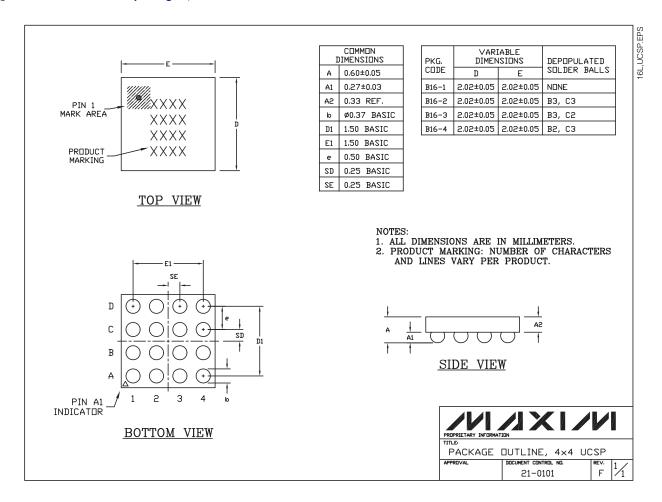


Typical Application Circuit



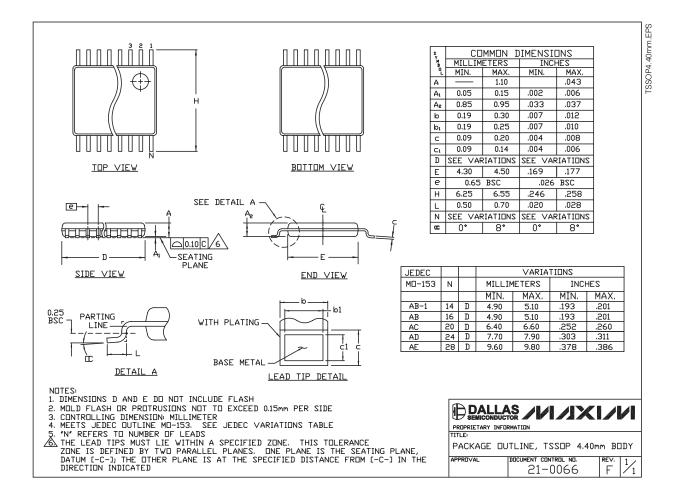
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



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