Ph. 480-503-4295 | NOPP@FocusLCDs.com

TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

Graphic Display Module

Part Number

G24064B-FTW-DW63

Overview:

- 240x64 Graphic LCD
- FSTN Gray
- 149.5x51.7mm Module
- Parallel and Serial Interface(s)
- White LED Backlight
- Transflective
- Wide Temp Range
- 3.0V
- LCD IC: NT7534
- RoHS Compliant

Graphic LCD Features

Resolution: 240x64 Dots
Interface(s): Parallel and Serial
RoHS Compliant.

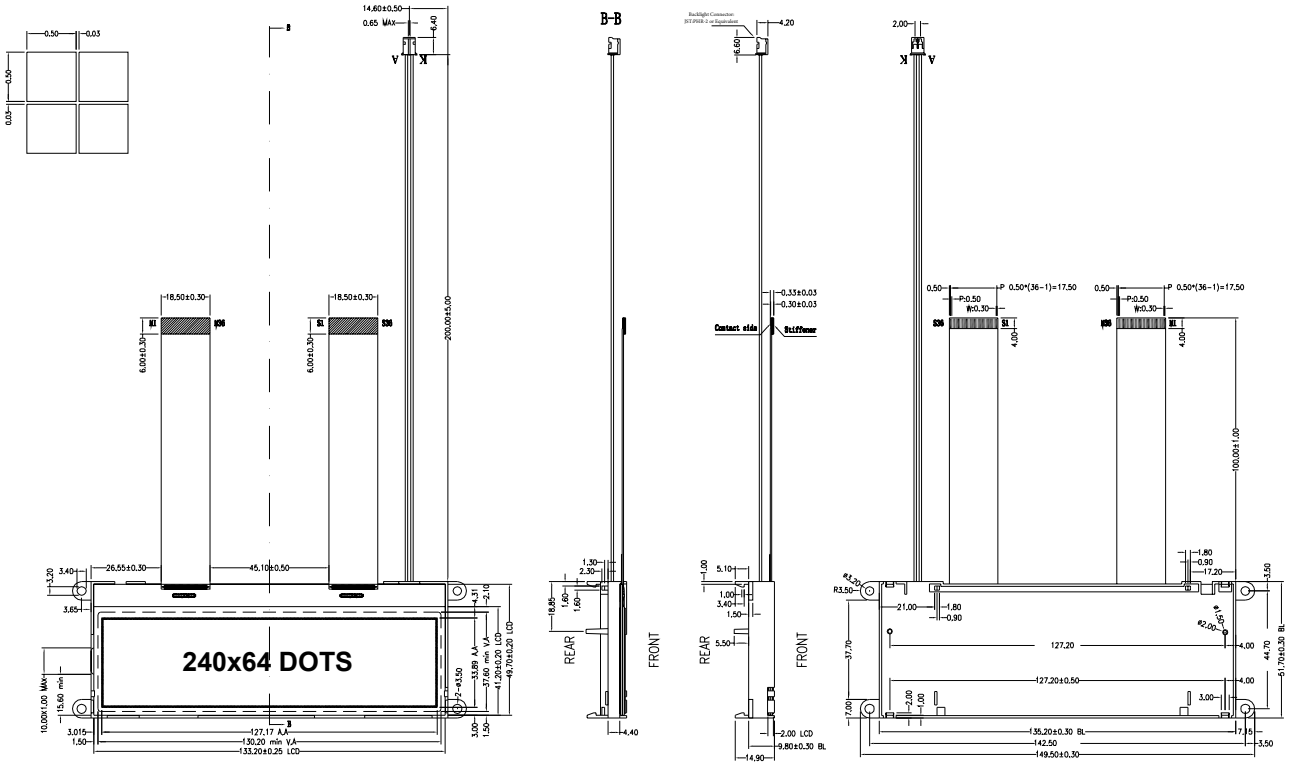
General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area (VA)	130.2 (H) x 37.6 (V)	mm	--
LCD Type	FSTN Positive	--	--
Viewing Angle	6:00	O'Clock	--
Polarizer	Transflective	--	--
Resolution	240x64	Dots	--
Backlight Type	LED	--	--
Backlight Color	White	mm	--
LCD IC	NT7534*2	--	--
Operating Temperature	-20 to +70	°C	--
Storage Temperature	-30 to +80	°C	--

Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	149.50	--	mm	--
	Vertical (V)	--	51.70	--	mm	--
	Depth (D)	--	14.90	--	mm	--
Weight		--	TBD	--	g	--

1. Outline Dimensions

Rev.	Description	Date
1.0	First	08/02/2021

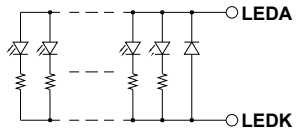


Interface(M):

NO	PIN
1	NC
2	FR
3	CL
4	/DOF
5	/CS1
6	CS2
7	/RES
8	A0
9	/WR
10	/RD
11	D0
12	D1
13	D2
14	D3
15	D4
16	D5
17	D6
18	D7
19	VDD
20	VSS
21	VOUT
22	C4+
23	C3+
24	C1-
25	C1+
26	C2+
27	C2-
28	V1
29	V2
30	V3
31	V4
32	V0
33	VR
34	C86
35	P/S
36	IRS

Interface(S):

NO	PIN
1	NC
2	FR
3	CL
4	/DOF
5	/CS1
6	CS2
7	/RES
8	A0
9	/WR
10	/RD
11	D0
12	D1
13	D2
14	D3
15	D4
16	D5
17	D6
18	D7
19	VDD
20	VSS
21	VOUT
22	C4+
23	C3+
24	C1-
25	C1+
26	C2+
27	C2-
28	V1
29	V2
30	V3
31	V4
32	V0
33	VR
34	C86
35	P/S
36	NC



Backlight Diagram

NOTES:

1. DISPLAY TYPE: 240x64 FSTN GRAY GRAPHIC LCD
2. POLARIZER: TRANSFLECTIVE, POSITIVE MODE
3. VIEWING ANGLE: 6:00
4. OPERATING TEMP: -20°C TO +70°C
   STORAGE TEMP: -30°C TO +80°C
5. DRIVE METHOD: 1/65 DUTY, 1/9 BIAS, VDD 3.0V, VLCD 9.7V
6. LCD IC: NT7534*2
7. BACKLIGHT: WHITE LED, 105mA, 3.3±0.2V
8. RoHS COMPLIANT.

Model Name: G24064B-FTW-DW63		FOCUS LCDs LCDs MADE SIMPLE
General Tol: ±0.2		
Approvals	Date	Drawing No.: / Scale:
DWN:		
CHK:		Size: / Unit: mm / Page: 1/1
APP:		

2. Input Terminal Pin Assignment

NO.	Symbol	Description	I/O
1	NC	--	--
2	FR	This is the liquid crystal alternative current signal I/O terminal. M/S="H": Output	I/O
3	CL	This is the display clock input terminal. When the NT7534 chips are used in master/slave mode, the various CL terminals must be connected.	I/O
4	/DOF	This is the liquid crytal display blanking control terminal. M/S="H": Output	I/O
5	/CS1	This is the chip select signal. When /CS1="L" and CS2="H", then the chip select becomes active, and the data/command I/O is enabled.	I
6	CS2		
7	/RES	When /RES is set to "L", the settings are initialized.	I
8	A0	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0="H": Indicates that D0 to D7 are display data A0="L": Indicates that D0 to D7 are control data	I
9	/WR	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When R/W="H": Read , When R/W="L": Write	I
10	/RD	When connected to an 8080 MPU, it is active LOW. This pad is connected to the /RD signal of the 8080 MPU, and the NT7534 data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 Series MPU.	I
11-18	D0-D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.	I/O
19	VDD	Power Supply.	S
20	VSS	Ground.	S
21	VOUT	DC/DC voltage converter output.	I/O
22	C4+	Capacitor 4+ pad for internal DC/DC voltage converter.	O
23	C3+	Capacitor 3+ pad for internal DC/DC voltage converter.	O
24	C1-	Capacitor 1- pad for internal DC/DC voltage converter.	O
25	C1+	Capacitor 1+ pad for internal DC/DC voltage converter.	O
26	C2+	Capacitor 2+ pad for internal DC/DC voltage converter.	O
27	C2-	Capacitor 2- pad for internal DC/DC voltage converter.	O

<table>
<tr><td>28-32</td><td>V1
V2
V3
V4
V0</td><td>LCD driver supplies voltages. The voltage determined by the LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be according to the following relationship:
V0≥V1≥V2≥V3≥V4≥VSS2
When the on-chip operating power circuit is on, the following voltages are supplied to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the LCD Bias Set command.</td><td>I/O</td></tr>
<tr><td>33</td><td>VR</td><td>Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.</td><td>I</td></tr>
<tr><td>34</td><td>C86</td><td>This is the MPU interface switch terminal.
C86="H": 6800 Series MPU Interface
C86="L": 8080 Series MPU Interface</td><td>I</td></tr>
<tr><td>35</td><td>P/S</td><td>This is the parallel data input/serial data input switch terminal.
P/S="H": Parallel data input
P/S="L": Serial data input.
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>"H"</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>-</td></tr>
<tr><td>"L"</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When the P/S="L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. /RD(E) and /WR (R/W) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.</td><td>I</td></tr>
<tr><td>36</td><td>IRS</td><td>This terminal selects the resistors for the V0 voltage level adjustment.
IRS="H", Use the internal resistors.
IRS="L", Do not use the internal resistors.</td><td>I</td></tr>
</table>

I: Input, O: Output, S: Supply

NO.	Symbol	Description	I/O
1	NC	--	--
2	FR	This is the liquid crystal alternative current signal I/O terminal. M/S="L": Input	I/O
3	CL	This is the display clock input terminal. When the NT7534 chips are used in master/slave mode, the various CL terminals must be connected.	I/O
4	/DOF	This is the liquid crytal display blanking control terminal. M/S="L": Input	I/O
5	/CS1	This is the chip select signal. When /CS1="L" and CS2="H", then the chip select becomes active, and the data/command I/O is enabled.	I
6	CS2		
7	/RES	When /RES is set to "L", the settings are initialized.	I
8	A0	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0="H": Indicates that D0 to D7 are display data A0="L": Indicates that D0 to D7 are control data	I

9	/WR	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When R/W="H": Read , When R/W="L": Write	I
10	/RD	When connected to an 8080 MPU, it is active LOW. This pad is connected to the /RD signal of the 8080 MPU, and the NT7534 data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 Series MPU.	I
11-18	D0-D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.	I/O
19	VDD	Power Supply.	S
20	VSS	Ground.	S
21	VOUT	DC/DC voltage converter output.	I/O
22	C4+	Capacitor 4+ pad for internal DC/DC voltage converter.	O
23	C3+	Capacitor 3+ pad for internal DC/DC voltage converter.	O
24	C1-	Capacitor 1- pad for internal DC/DC voltage converter.	O
25	C1+	Capacitor 1+ pad for internal DC/DC voltage converter.	O
26	C2+	Capacitor 2+ pad for internal DC/DC voltage converter.	O
27	C2-	Capacitor 2- pad for internal DC/DC voltage converter.	O
28-32	V1 V2 V3 V4 V0	LCD driver supplies voltages. The voltage determined by the LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be according to the following relationship: V0≥V1≥V2≥V3≥V4≥VSS2 When the on-chip operating power circuit is on, the following voltages are supplied to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the LCD Bias Set command.	I/O
33	VR	Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.	I
34	C86	This is the MPU interface switch terminal. C86="H": 6800 Series MPU Interface C86="L": 8080 Series MPU Interface	I

<table>
<tr>
<td>35</td>
<td>P/S</td>
<td>This is the parallel data input/serial data input switch terminal.
P/S="H": Parallel data input
P/S="L": Serial data input.
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>"H"</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>-</td></tr>
<tr><td>"L"</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When the P/S="L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. /RD (E) and /WR (R/W) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.</td>
<td>I</td>
</tr>
<tr>
<td>36</td>
<td>NC</td>
<td>-</td>
<td>-</td>
</tr>
</table>

I: Input, O: Output, S: Supply

3. LCD Optical Characteristics

Item		Symbol	Condition	Min	Typ.	Max	Unit
Contrast Ratio		CR		--	3	--	
Response Time	On	T_{on}		--	150	250	ms
	Off	T_{off}		--	180	300	ms
Viewing Angle $C_1 \geq 2$, 25°C	Hor.	Θ_L	Φ=270°, 9H	--	55	--	degree
		Θ_R	Φ=90°, 3H	--	55	--	
	Ver.	Θ_T	Φ=180°, 12H	--	40	--	
		Θ_B	Φ=0°, 6H	--	70	--	

4. Electrical Characteristics

4.1 Absolute Maximum Rating

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	VDD	-0.3	4.0	V
	Vout	-0.3	15.0	V
Operating Temperature	TOP	-20	+70	°C
Storage Temperature	TST	-30	+80	°C

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

4.2 DC Electrical Characteristics

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
LCD Driving Voltage		VLCD		--	9.7	--	V
Supply Voltage		Logic	VDD-GND	--	3.0	--	V
Input Voltage	H Level	VDD		0.8VDD	--	VDD	V
	L Level	VIH		VSS	--	0.2VDD	V

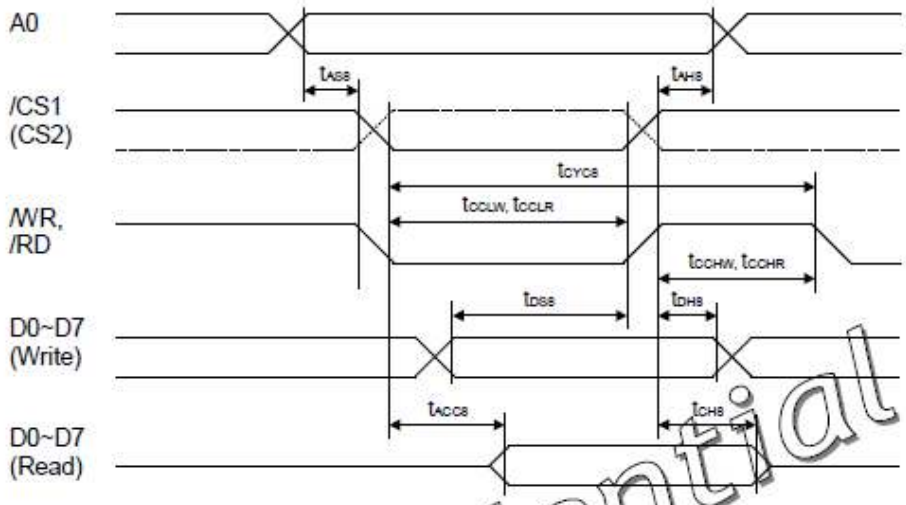
Condition:

1. VDD = 3.0V
2. 1/65 Duty, 1/9 Bias

5.0 Module Function

5.1 Timing Characteristics

1. System Buses Read/Write Characteristics (for 8080 Series MPU)



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH8}	Address hold time	0	-	-	ns	A0
t_{AS8}	Address setup time	0	-	-	ns	
t_{CYC8}	System cycle time	240	-	-	ns	
t_{CCLW}	Control low pulse width (write)	120	-	-	ns	/WR
t_{CCLR}	Control low pulse width (read)	120	-	-	ns	/RD
t_{CCHW}	Control high pulse width (write)	100	-	-	ns	/WR
t_{CCHR}	Control high pulse width (read)	100	-	-	ns	/RD
t_{DS8}	Data setup time	40	-	-	ns	D0~D7
t_{DH8}	Data hold time	10	-	-	ns	
t_{ACC8}	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
t_{CH8}	Output disable time	5	-	50	ns	

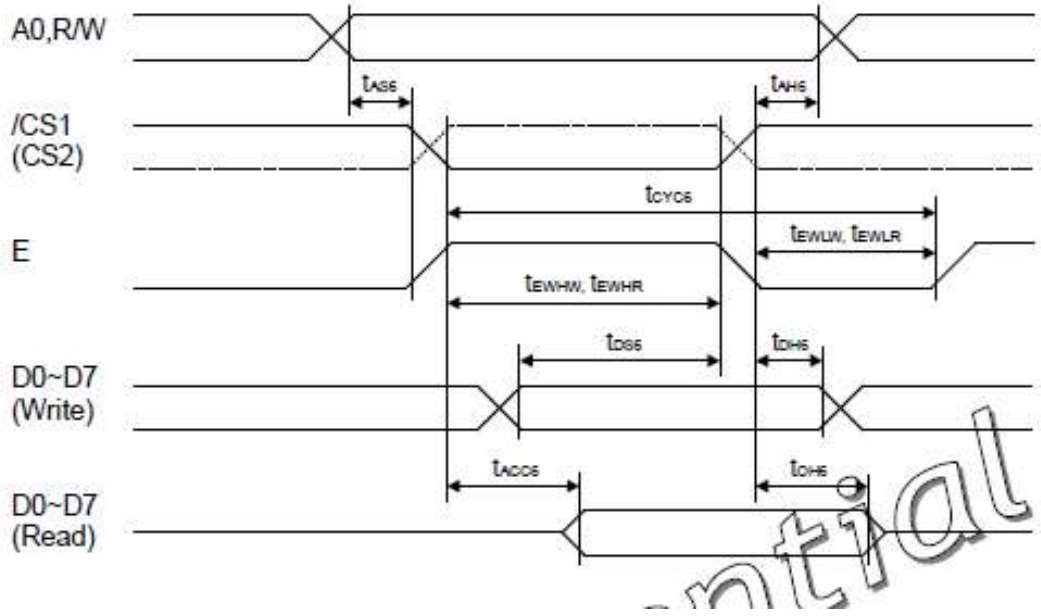
System Buses Read/Write Characteristics (for 8080 Series MPU) (continued)

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH8}	Address hold time	0	-	-	ns	A0
t_{AS8}	Address setup time	0	-	-	ns	
t_{CYC8}	System cycle time	400	-	-	ns	
t_{CCLW}	Control low pulse width (write)	150	-	-	ns	/WR
t_{CCLR}	Control low pulse width (read)	150	-	-	ns	/RD
t_{CCHW}	Control high pulse width (write)	120	-	-	ns	/WR
t_{CCHR}	Control high pulse width (read)	120	-	-	ns	/RD
t_{DS8}	Data setup time	80	-	-	ns	D0~D7
t_{DH8}	Data hold time	30	-	-	ns	
t_{ACC8}	/RD access time	-	-	240	ns	D0~D7, CL = 100pF
t_{CH8}	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < (t_{CYC8} - t_{CCLW} - t_{CCHW}) for write, ($t_r + t_f$) < (t_{CYC8} - t_{CCLR} - t_{CCHR}) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when /CS1 is low (CS2 is high) and /WR or /RD is low.

2. System Buses Read/Write Characteristics (for 6800 Series MPU)



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AHS}	Address hold time	0	-	-	ns	A0, R/W
t_{ASS}	Address setup time	0	-	-	ns	
t_{CYCS}	System cycle time	240	-	-	ns	
t_{EWHW}	Control low pulse width (write)	120	-	-	ns	E
t_{EWHR}	Control low pulse width (read)	120	-	-	ns	E
t_{EWLW}	Control high pulse width (write)	100	-	-	ns	E
t_{EWLR}	Control high pulse width (read)	100	-	-	ns	E
t_{DSS}	Data setup time	40	-	-	ns	D0~D7
t_{DHS}	Data hold time	10	-	-	ns	
t_{ACCS}	/RD access time	-	-	140	ns	D0~D7 CL = 100pF
t_{OHS}	Output disable time	5	-	50	ns	

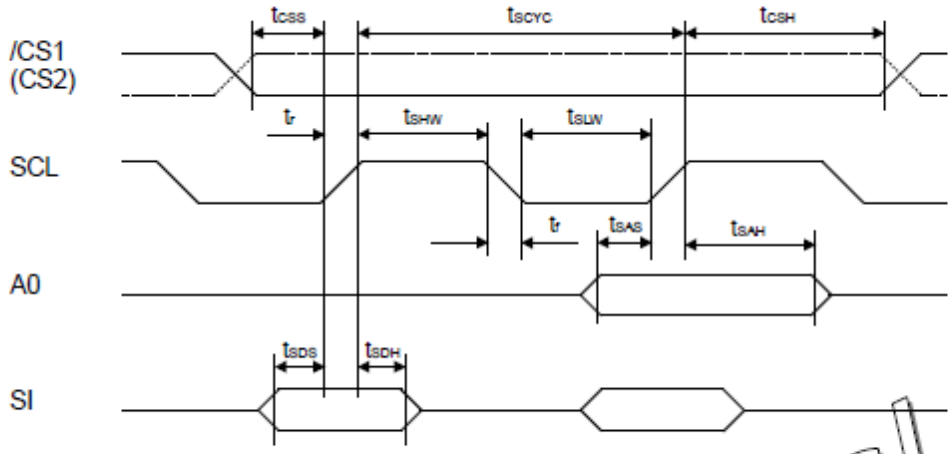
System Buses Read/Write Characteristics (for 6800 Series MPU) (continued)

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AHS}	Address hold time	0	-	-	ns	A0, R/W
t_{ASS}	Address setup time	0	-	-	ns	
t_{CYCS}	System cycle time	400	-	-	ns	
t_{EWHW}	Control low pulse width (write)	150	-	-	ns	E
t_{EWHR}	Control low pulse width (read)	150	-	-	ns	E
t_{EWLW}	Control high pulse width (write)	120	-	-	ns	E
t_{EWLR}	Control high pulse width (read)	120	-	-	ns	E
t_{DSS}	Data setup time	80	-	-	ns	D0~D7
t_{DHS}	Data hold time	30	-	-	ns	
t_{ACCS}	/RD access time	-	-	240	ns	D0~D7 CL = 100pF
t_{OHS}	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < (t_{CYCS} - t_{EWLW} - t_{EWHW}) for write, ($t_r + t_f$) < (t_{CYCS} - t_{EWLR} - t_{EWHR}) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. t_{EWHW} and t_{EWHR} are specified as the overlap interval when /CS1 is low (CS2 is high) and E is high.

3. Serial Interface Timing



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	120	-	-	ns	SCL
tSHW	Serial clock H pulse width	60	-	-	ns	SCL
tSLW	Serial clock L pulse width	60	-	-	ns	SCL
tSAS	Address setup time	30	-	-	ns	A0
tSAH	Address hold time	20	-	-	ns	A0
tSDS	Data setup time	30	-	-	ns	SI
tSDH	Data hold time	20	-	-	ns	SI
tCSS	Chip select setup time	20	-	-	ns	/CS1, CS2
tCSH	Chip select hold time	40	-	-	ns	/CS1, CS2

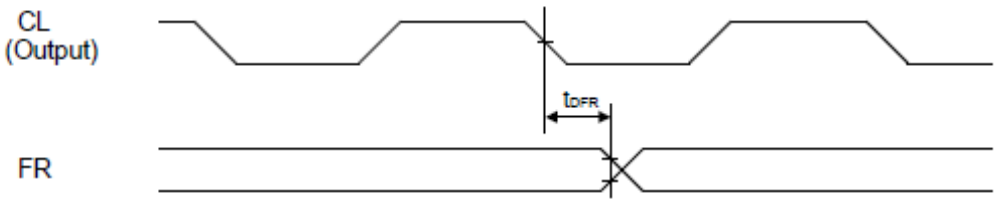
Serial Interface Timing (continued)

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	200	-	-	ns	SCL
tSHW	Serial clock H pulse width	80	-	-	ns	SCL
tSLW	Serial clock L pulse width	80	-	-	ns	SCL
tSAS	Address setup time	60	-	-	ns	A0
tSAH	Address hold time	30	-	-	ns	A0
tSDS	Data setup time	60	-	-	ns	SI
tSDH	Data hold time	40	-	-	ns	SI
tCSS	Chip select setup time	40	-	-	ns	/CS1, CS2
tCSH	Chip select hold time	100	-	-	ns	/CS1, CS2

*1. The input signal rise time and fall time (tr, tf) is specified as 15ns or less.
*2. All timing is specified using 20% and 80% of VDD as the standard.

4. Display Control Timing



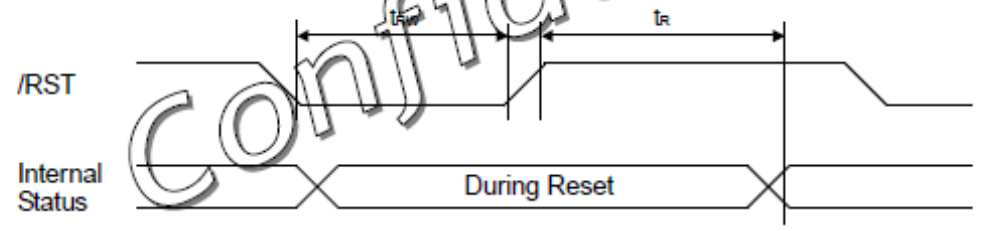
(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{DFR}	FR delay time	-	20	80	ns	CL = 50 pF

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{DFR}	FR delay time	-	40	160	ns	CL = 50 pF

5. Reset Timing



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset Time	-	-	1.0	µs	
t_{RW}	Reset low pulse width	10	-	-	µs	/RES

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

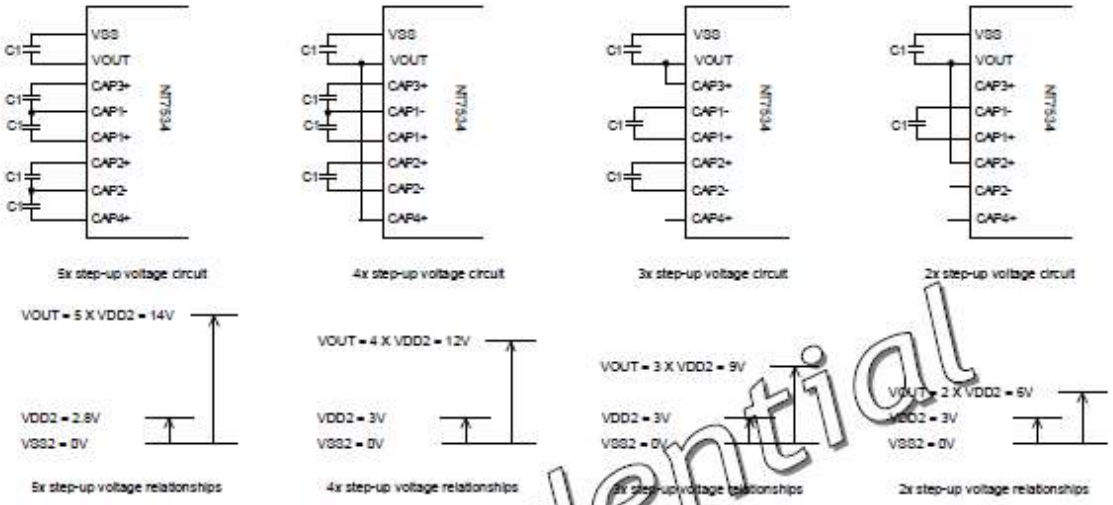
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset Time	-	-	2.0	µs	
t_{RW}	Reset low pulse width	20	-	-	µs	/RES

5.2 LCM Application

The Step-up Voltage Circuits

Using the step-up voltage circuits within the NT7534 chips it is possible to product 5X, 4X, 3X, 2X step-ups of the VDD2-VSS2 voltage levels.

Figure 7



The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the liquid crystal driver voltage V0 through the voltage regulator circuit. Because the NT7534 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

Moreover, NT7534 has thermal gradients: approximately –0.05%/°C.

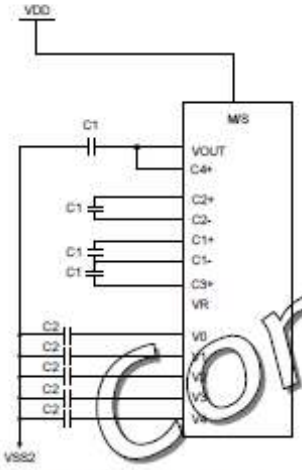
High Power Mode

The power supply circuit equipped in the NT7534 chips has very low power consumption (normal mode: /HPM="H"). However for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the /HPM terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.

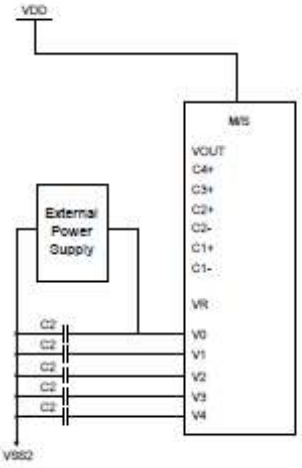
Moreover, if the improvement to the display is inadequate even after the high power mode has been set, then it is necessary to add a Command Sequence when Built-in Power Supply is turned OFF. To turn off the built-in power supply, follow the command sequence as shown below to turn it off after making the system enter standby mode.

Reference Power Supply Circuit for Driving LCD Panel

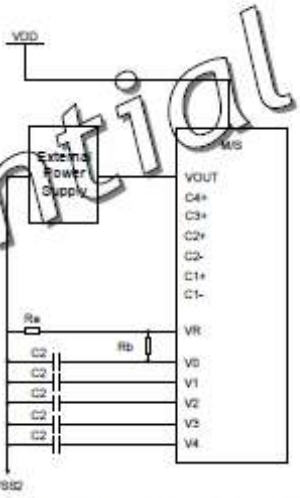
-When using all LCD power circuits
(Voltage booster, regulator and follower)
(In case of 4X boosting circuit and internal regulator resistors, IRS=1)



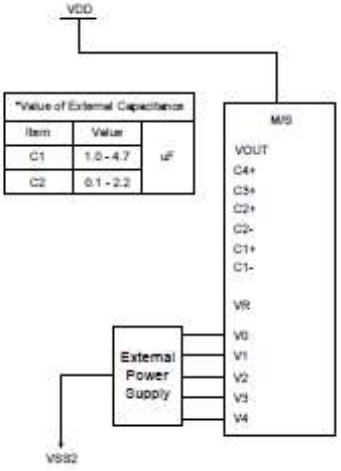
-When only using voltage follower



--When not using voltage booster circuits
(In case of external regulator resistors, IRS=0)



-When not using internal LCD power supply circuits



5.3 Command Table

Command	A0	/RD	/WR	Code D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies RAM display line for COM0
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h to B8h	Set the display data RAM page in Page Address register
(4) Column Address Set	0	1	0	0	0	0	1	Higher Column Address				00h to 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Select normal display (0) or entire display on
(11)LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Select COM output scan direction *: invalid data
(16)Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Select the power circuit operation mode
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Select internal resistor ratio Rb/Ra mode
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19)Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation

Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(22)Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency
(23)Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0 1	82h 83h	Enter/Release the partial display mode
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1	Partial Start Line						XX	Sets the LCD Number of partial display start line
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	1	0	*	*	*	Number of Line					XX	Sets the number of line used for N-Line inversion
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division				XX	Set the Division of DC/DC Clock Frequency
(30)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

Note: Do not use any other command, or system malfunction may result.

5.3 Initialization Code

```
void init()
{
        RES=0;
        delay(2);
        RES=1;
        delay(2);
  write_com_M(0xa2);      //1/9Bias
        write_com_M(0xa1);        //ADC set (SEG)
        write_com_M(0xc0);         //COM reves
        write_com_M(0xa6);         //DISPLAY NORMAL
        write_com_M(0x40);         //DISPLAY START LINE SET
        write_com_M(0x24);
        write_com_M(0x81);        //Electronic Volume Mode Set
        write_com_M(0x32);        //Electronic Volume Register Set()
        write_com_M(0xf8);        //The Booster set 4x
        write_com_M(0x00);        //The Booster set 4x
        write_com_M(0x2f);        //The Power Control Set    VOUT
        write_com_S(0xa2);        //1/7 Bias
        write_com_S(0xa1);        //ADC set (SEG)
        write_com_S(0xc0);        //COM reves
        write_com_S(0xa6);        //DISPLAY NORMAL
        write_com_S(0x40);        //DISPLAY START LINE SET
        write_com_S(0x24);
       write_com_S(0xf8);         //The Booster set 4x
        write_com_S(0x00);        //The Booster set 4x
        write_com_S(0x2f);        //The Power Control Set VOUT
        delay(50);              //
        clealddram();
        delay(50);              //
        write_com_A(0xaf);        //Lcd Disply ON
        delay(50);              //
}
```

6.0 Cautions and Handling Precautions

6.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

6.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.