AN2950
Application note

EVLVIPER28L-10W: 5 V/10 W, 60 kHz isolated flyback with extra power management

Introduction

This document describes a 5 V, 2 A application with 3.3 A peak current capability of 1.9 sec, using VIPer28, a new offline high-voltage converter from STMicroelectronics.

In some applications, an SMPS sometimes undergoes load peaks that can be two or more times as much as the power it is supposed to deliver, though only for a short time interval compared to the thermal time constants of the power components. Typical examples of such loads are printers and audio systems.

In such cases, it is more cost-effective to thermally design the system for the maximum continuous power and not for the peak power demand, which is sustained only for a limited time window.

Such a design is possible thanks to the EPT function of the VIPer28, which allows the designer to fix the maximum time window during which the converter is able to manage the peak power and still maintain output voltage regulation. If the overload lasts for longer than this time window, the converter is automatically shut down and enters auto-restart mode until the overload is removed, so as to prevent damage to the power components.

The device has many other features such as an 800 V avalanche rugged power section, PWM operation at 60 kHz with frequency jittering for lower EMI, a limiting current with adjustable setpoint, an on-board soft-start, a safe auto-restart after a fault condition, and a low standby power (< 50 mW at 265 V_{AC}).

The available protections include adjustable and accurate overvoltage protection, thermal shutdown with hysteresis and delayed overload protection.

Figure 1. Demonstration board

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1 Adapter features

Table 1 lists the electrical specifications of the demonstration board.

Table 1. Electrical specification

Parameter	Symbol	Value
Input voltage range	V_{IN}	[90 V_{RMS}; 265 V_{RMS}]
Output voltage	V_{OUT}	5 V
Maximum output current	I_{OUTmax}	2 A
Peak output current	I_{OUTpk}	3 A
Precision of output regulation	Δ_{VOUT_LF}	±5%
High-frequency output voltage ripple	Δ_{VOUT_HF}	50 mV
Maximum ambient operating temperature	T_A	60°C

1.1 Circuit description

The power supply is set-up in a flyback topology. Its schematic is shown in *Figure 2*. The input section includes the protection elements (fuse and NTC for inrush current limiting), a filter for EMC suppression (C1, T2, C13), a diode bridge (BR1) and an electrolytic bulk capacitor (C3) as the front-end AC-DC converter. The transformer uses a standard E25 ferrite core. A transil clamp network is used to demagnetize the leakage inductance.

At power-up, the DRAIN pin supplies the internal HV start-up current generator that charges the C4 capacitor up to V_{DDon}. At this point, the power MOSFET starts switching, the generator is turned off and the IC is powered by the energy stored in C4 until the auxiliary winding voltage becomes high enough to sustain the operation through D1 and R1.

The value of the resistor R3 between the CONT and GND pins is high enough that the VIPer28's current limit does not change with respect to the datasheet's default value I_{Dlim}. This resistor, in conjunction with D2, R14 and R15, is used to realize the overvoltage protection and the feedforward correction function, as described further in this document.

The output rectifier D4 has been selected according to the calculated maximum reverse voltage, forward voltage drop and power dissipation, and is a power Schottky type.

The output voltage regulation is performed by a secondary feedback with a TS431 driving an optocoupler (in this case a PC817) ensuring the required insulation between the primary and secondary. The opto-transistor drives directly the FB pin of the VIPer28, which is connected to the compensation network made up by C6, C7 and R12.

A small LC filter has been added at the output in order to filter the high-frequency ripple without increasing the size of the output capacitors, and a 100 nF capacitor has been placed very close to the solder points of the output connector to limit the spike amplitude.

Figure 2. Application schematic

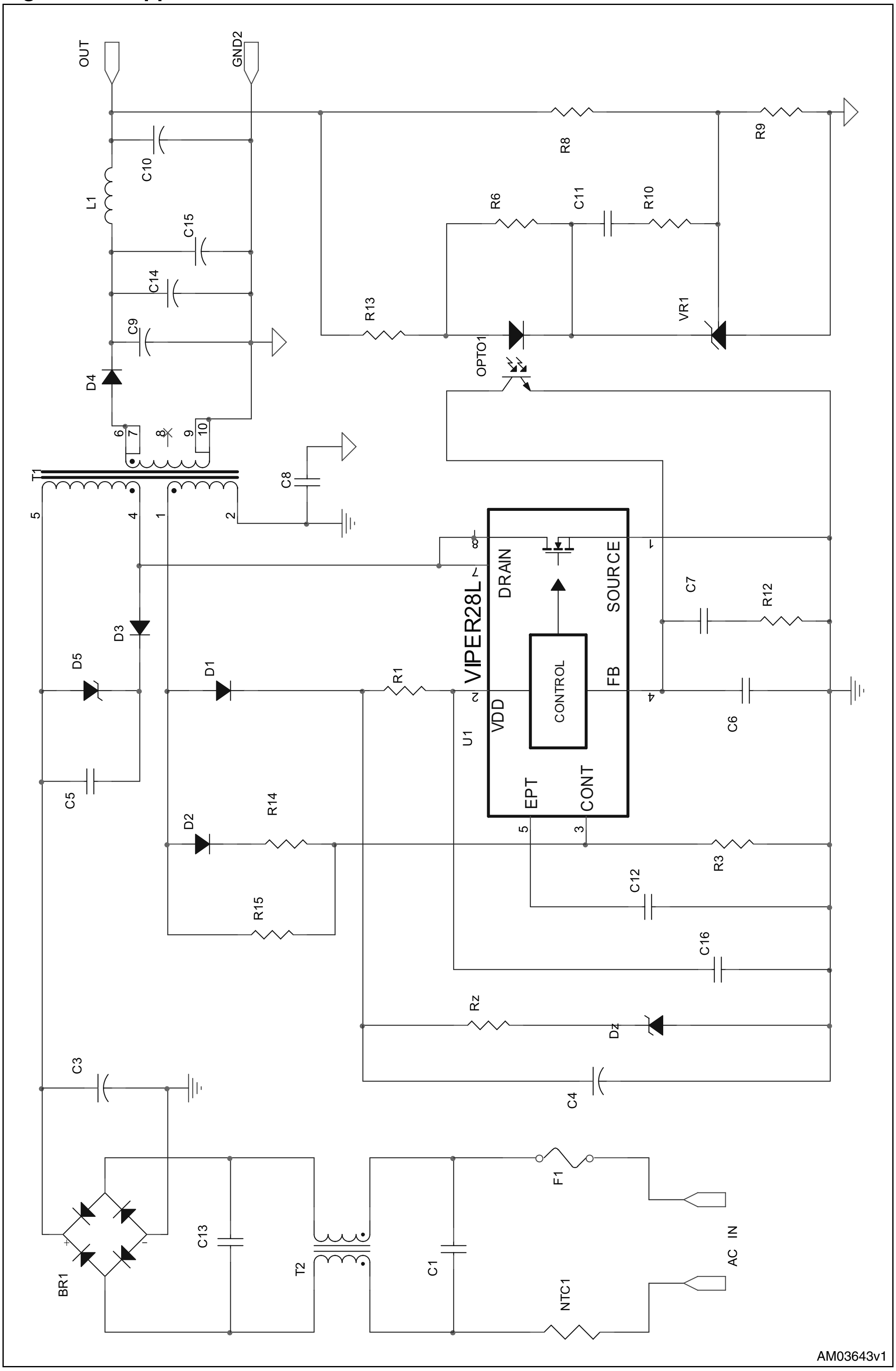


Table 2. **Bill of materials**

Reference	Part	Description	Manufacturer
BR1	DF06M	600 V 1 A diodes bridge	VISHAY
C1, C13		100 nF X2 capacitor	EVOX RIFA
C3		47 µF 450 V electrolytic capacitor	PANASONIC
C4		22 µF 35 V electrolytic capacitor	PANASONIC
C5, C9		Not mounted	
C6		3.3 nF 25 V ceramic capacitor	EPCOS
C7		33 nF 50 V ceramic capacitor	EPCOS
C8		2.2 nF Y1 capacitor	CERAMITE
C14, C15	MCZ series	1000 µF 10 V ultra-low ESR electrolytic capacitor	RUBYCON
C10		100 µF 10 V electrolytic capacitor	PANASONIC
C11		4.7 nF 100 V ceramic capacitor	EPCOS
C12		2.2 µF 50 V electrolytic capacitor	PANASONIC
C16		2.2 nF 100 V ceramic capacitor	AVX
D1	BAT46	Diode	STMicroelectronics
D2	1N4148	Small-signal, high-speed diode	NXP
D3	STTH1L06	Ultra-fast, high-voltage diode	STMicroelectronics
D4	STPS5L40	5 A - 40 V power Schottky rectifier	STMicroelectronics
D5	1.5KE300	Transil	STMicroelectronics
Dz	BZX79-C18	18 V Zener diode	NXP
F1	TR5 250 V 500 mA	Fuse	SCHURTER
L1	RFB0807-2R2L	2.2 µH	COILCRAFT
NTC1		2.2 Ω thermistor	EPCOS
OPTO1	PC817D	Opto coupler	SHARP
R1		4.7 Ω 1/4 W axial resistor	
R3		68 kΩ 1/4 W axial resistor	
R6		15 kΩ 1/4 W axial resistor	
R8		82 kΩ 1/4 W axial resistor 1% tolerance	
R9		27 kΩ 1/4 W axial resistor 1% tolerance	
R10		560 kΩ 1/4 W axial resistor	
R12		10 kΩ 1/4 W axial resistor	
R13		3.3 kΩ 1/4 W axial resistor	
R14		330 kΩ 1/4 W axial resistor	
R15		2 MΩ 1/4 W axial resistor	
Rz		68 Ω 1/4 W axial resistor	

Table 2. Bill of materials (continued)

Reference	Part	Description	Manufacturer
T2	BU16-4530R5BL	Common mode choke	COILCRAFT
VR1	TS431	Voltage reference	STMicroelectronics
U1	VIPER28LN	Offline high voltage controller	STMicroelectronics
T1	1338.0019	Switch mode power transformer	MAGNETICA

1.2 Transformer

Table 3 lists the electrical characteristics of the transformer.

Table 3. 1338.0019 transformer characteristics

Properties	Value	Test Condition
Primary inductance	1.5 mH ±15%	Measured at 1 kHz
Leakage inductance	0.8% nom.	Measured at 10 kHz
Primary to secondary turn ratio (4 - 5)/(6,7 – 10,9)	12.85 ±5%	Measured at 10 kHz
Primary to auxiliary turn ratio (4 - 5)/(1 - 2)	5.29 ±5%	Measured at 10 kHz
Nominal operating frequency	60 kHz	
Nominal/peak power	10 W/15 W	
Saturation current	1 A	B_{SAT} = 0.32T
Insulation	4 kV	Primary to secondary

The size, pinout and mechanical characteristics are given in the following figures.

Figure 3. Transformer size and pin diagram - bottom view (pin side)

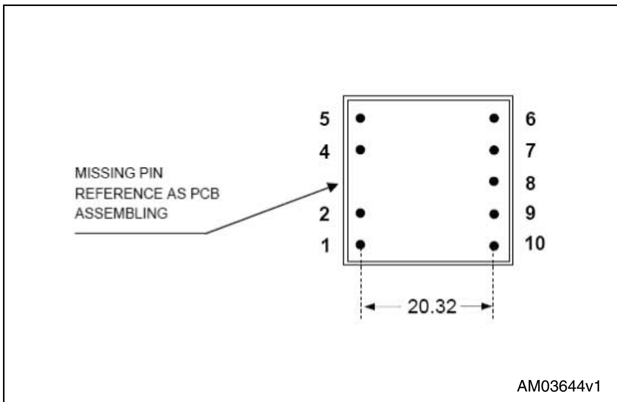
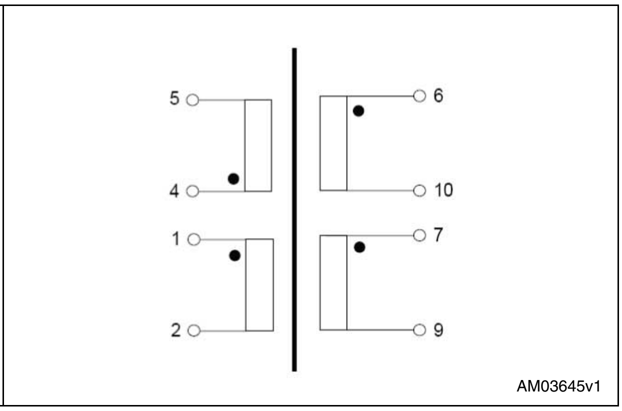


Figure 4. Transformer size and pin diagram - electrical diagram



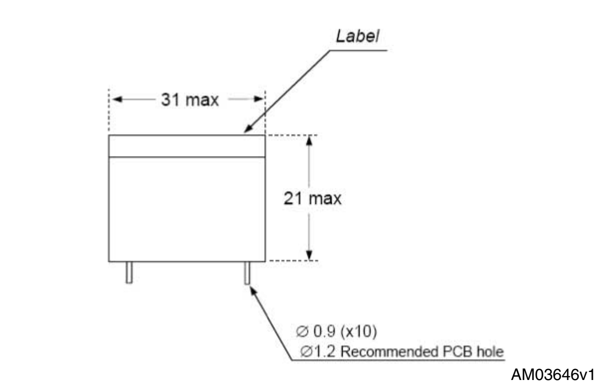


Figure 5. Transformer size - side view 1

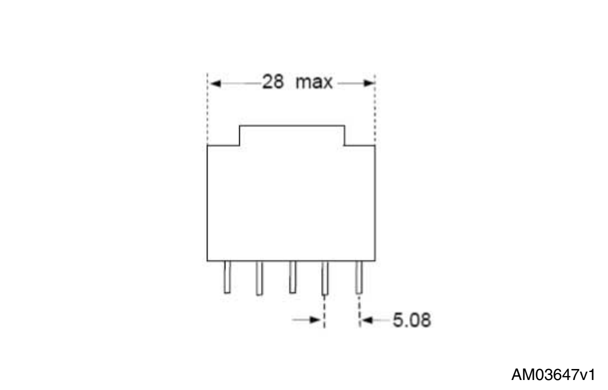


Figure 6. Transformer size - side view 2

Table 4. Transformer pin description

Pin	Description	Pin	Description
5	Primary, to the DC input voltage (400 V)	6	Secondary output
4	Primary, to the drain of the MOSFET	7	
3	Removed	8	n.c
2	Auxiliary GND	9	Secondary GND
1	Auxiliary output	10	

2 Testing the board

2.1 Typical board waveforms

The drain voltage and current waveforms are reported for the two nominal input voltages and for the minimum and maximum voltages of the converter's input operating range.

Figure 7 and *Figure 8* show the drain current voltage waveforms at nominal input voltages (115 V_{AC} and 230 V_{AC}) and maximum load (2 A). *Figure 9* and *Figure 10* show the same waveforms for the same load conditions, but with minimum (90 V_{AC}) and maximum (265 V_{AC}) input voltages.

Figure 11 and *Figure 12* show the same waveforms during peak load conditions (3.3 A), which the converter is able to sustain for approximately 1.9 seconds while still keeping the output voltage under regulation.

The converter is operated in continuous conduction mode (CCM) at low input voltage during full load conditions and even at high input voltage during peak load conditions. CCM allows reducing the value of the root mean square currents, both on the primary side (in the power switch) and on the secondary side (in the output diode D4 and in the output capacitors C9 and C14), thus reducing the power dissipation and the stress on the power components.

Figure 7. Drain current and voltage at maximum load 115 V_{AC}

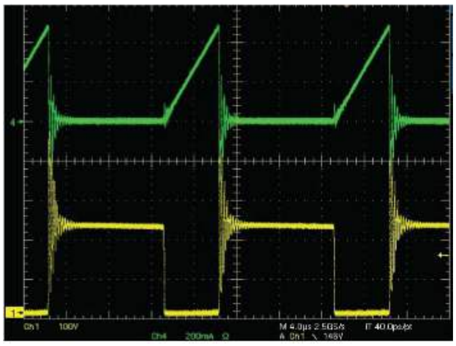


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Figure 8. Drain current and voltage at maximum load 230 V_{AC}

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Figure 9. Drain current and voltage at maximum load 90 V_{AC}

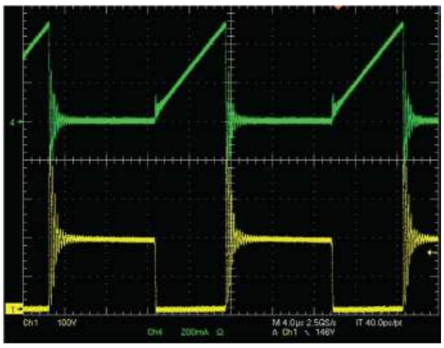

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Figure 10. Drain current and voltage at maximum load 265 V_{AC}

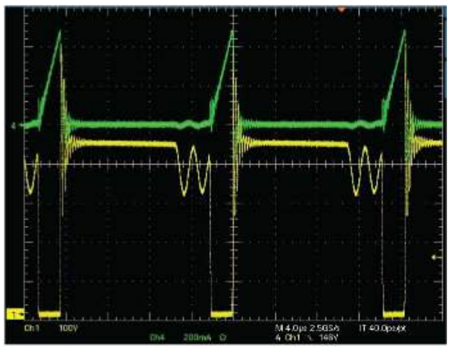

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Figure 11. Drain current and voltage at peak load 90 V_{AC}

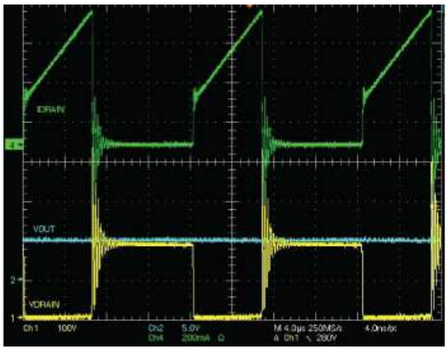

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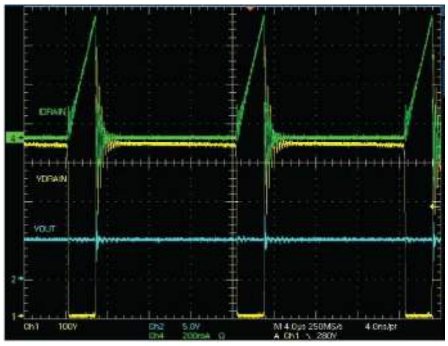
Figure 12. Drain current and voltage at peak load 265 V_{AC}



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2.2 Regulation precision and output voltage ripple

The output voltage of the board has been measured with different line and load conditions. The results are reported in *Table 5*. The output voltage is not affected by the line condition. The V_{DD} voltage has also been measured to verify that it is within the device's operating range.

As confirmed by the results reported in *Table 5*, the V_{DD} voltage (unregulated auxiliary output) increases as the load on the regulated output increases. To prevent the V_{DD} voltage from exceeding its operating range, an external clamp has been used (Dz, Rz).

Table 5. Output voltage and V_{DD} line-load regulation

V_{IN_AC} (V)	No load		Half load		Full load		Peak load	
	V_{OUT} (V)	V_{DD} (V)	V_{OUT} (V)	V_{DD} (V)	V_{OUT} (V)	V_{DD} (V)	V_{OUT} (V)	V_{DD} (V)
90	5.02	10.8	4.99	18.8	4.99	19.6	4.98	20.5
115	5.02	10.4	4.99	18.7	4.99	19.5	4.98	20.3
230	5.02	10.3	4.99	18.6	4.99	19.4	4.98	20
265	5.02	10.1	4.99	18.5	4.99	19.2	4.98	19.8

The ripple at the switching frequency superimposed at the output voltage has also been measured and the results are reported in *Table 6*. The board is provided with an LC filter to better filter the voltage ripple.

Table 6. Output voltage ripple

V_{IN_AC} (V)	Half load	Full load	Peak load
	V_{OUT} (mV)	V_{OUT} (mV)	V_{OUT} (mV)
90	15	17	30
115	14	21	28
230	15	22	25
265	14	20	24

Figure 13. **Output voltage ripple 115 V_{IN_AC} full load**

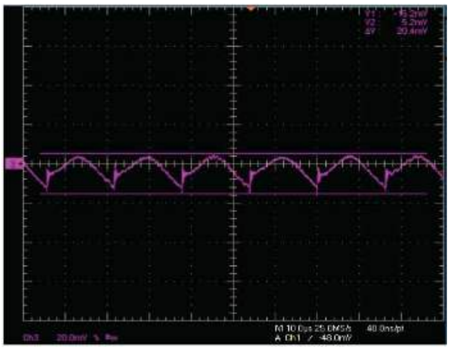

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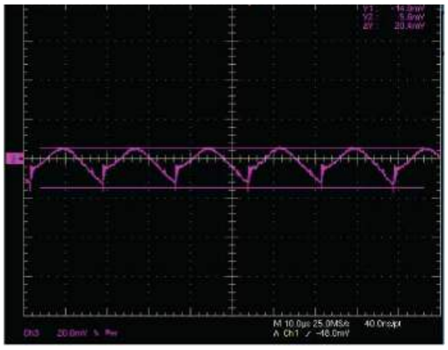
Figure 14. **Output voltage ripple 230 V_{IN_AC} full load**



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2.3 Burst mode and output voltage ripple

When the load is so low that the voltage at the FB pin falls below the internal threshold V_{FBbm} (0.6 V typical), the VIPer28 is disabled. At this point, the feedback's reaction to the stop of energy delivery makes the FB voltage increase again, and when it goes 100 mV above the V_{FBbm} threshold the device restarts switching. This results in a controlled on/off operation referred to as "burst mode" and is shown in the figures below, which report the output voltage ripple and the feedback voltage when the converter is not or only lightly loaded and supplied with 115 V_{AC} and 230 V_{AC} respectively. This mode of operation keeps the frequency-related losses low when the load is very light or disconnected and makes it easier to comply with energy-saving regulations.

Figure 15. **Output voltage ripple at 115 V_{IN_AC} no load**

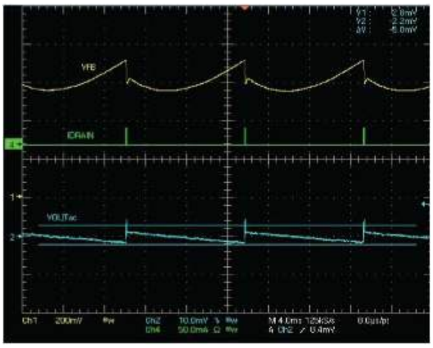

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Figure 16. **Output voltage ripple at 230 V_{IN_AC} no load**

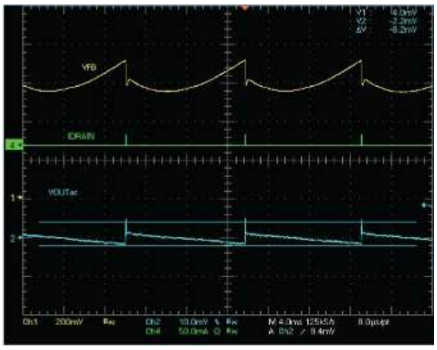

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Figure 17. Output voltage ripple at 115 V_{IN_AC} 50 mA

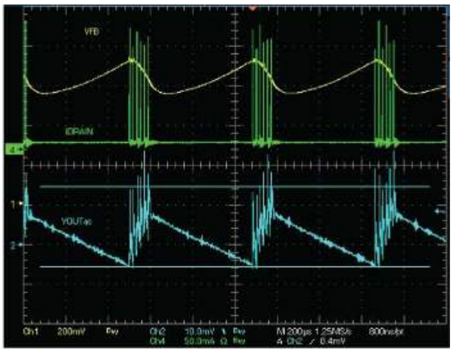

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Figure 18. Output voltage ripple at 230V_{IN_AC} 50 mA

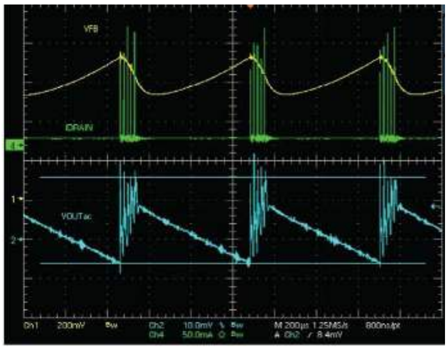

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Table 7 shows the measured value of the burst mode frequency ripple measured in different operating conditions. The ripple in burst mode operation is very low and always below 25 mV.

Table 7. Burst mode related output voltage ripple

V_{IN}	No load (mV)	25 mA load (mV)	50 mA load (mV)
90	5	14	15.4
115	5.6	18.2	20.2
230	6	19.2	22
265	6.5	20.2	24

2.4 Efficiency

This and the following section report the results of efficiency and light load measurements. *Appendix A* at the end of this document provides some details on the settings of the power measurement equipment.

According to the ENERGY STAR® average active mode efficiency testing method, the efficiency measurements have been done at full load and at 75%, 50% and 25% of full load for different input voltages. The results are reported in *Table 8*.

Table 8. Efficiency

V_{IN_AC} (VRMS)	Efficiency (%)			
	Full load (2 A)	75% load (1.5 A)	50% load (1 A)	25% load (0.5 A)
90	79.06	79.93	79.41	83.72
115	80.61	81.12	83.45	83.78
150	81.53	81.85	81.73	85.03
180	81.90	81.58	80.46	80.38

Table 8. Efficiency (continued)

V_{IN_AC} (VRMS)	Efficiency (%)			
	Full load (2 A)	75% load (1.5 A)	50% load (1 A)	25% load (0.5 A)
230	82.07	82.13	80.06	80.39
265	81.96	81.94	81.16	80.36

For better visibility, the results have also been plotted in the diagrams below. *Figure 19* plots the efficiency versus V_{IN} for the four different load values. *Figure 20* reports the efficiency as a function of the load for different input voltage values.

Figure 19. Efficiency vs V_{IN}

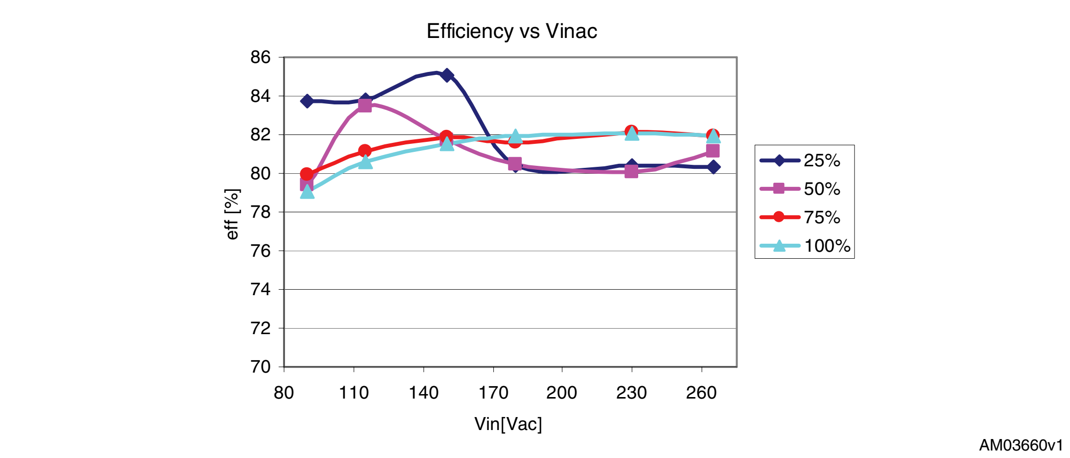
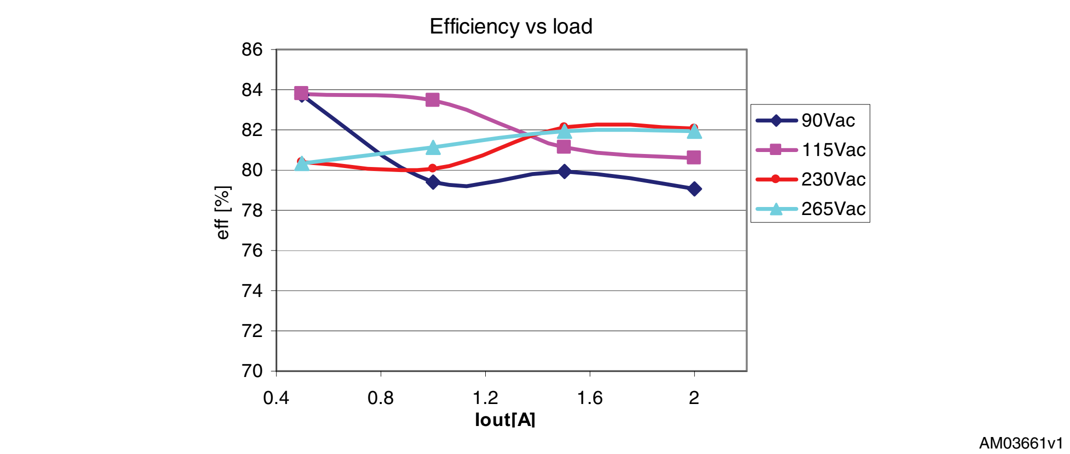


Figure 20. Efficiency vs load

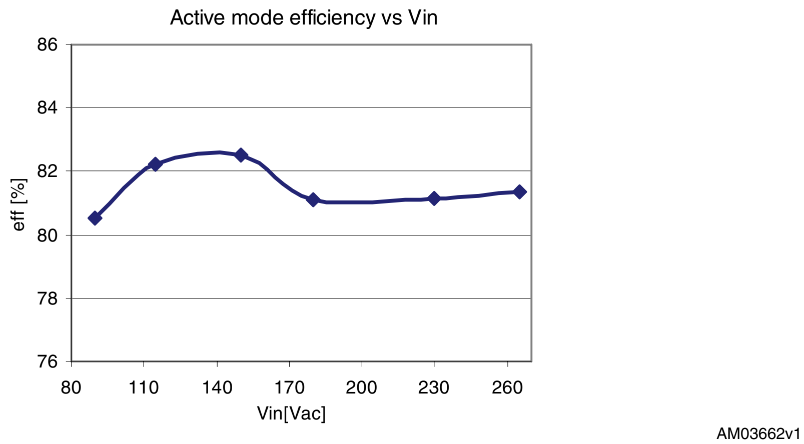


The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50% and 75% of the maximum load and at the maximum load itself. *Table 9* reports the active mode efficiency calculated from the values in *Table 8*. For clarity, the values in *Table 9* are plotted in *Figure 21*.

Table 9. Active mode efficiency

Active mode efficiency	
V_{IN_AC} (V_{RMS})	Efficiency (%)
90	80.53
115	82.24
150	82.53
180	81.08
230	81.16
265	81.36

Figure 21. Active mode efficiency vs V_{IN}

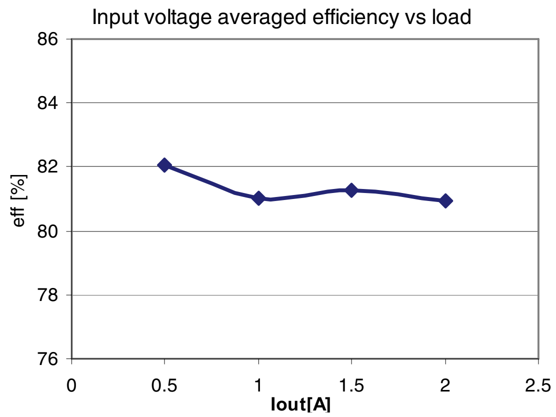


In *Table 10* and *Figure 22* the averaged values of the efficiency versus load are reported (the average has been done considering the efficiency at different values of the input voltage).

Table 10. Input voltage averaged efficiency

Load (% of full load)	Efficiency (%)
100	80.93
75	81.28
50	81.02
25	82.06

Figure 22. Input voltage averaged efficiency vs load



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In version 2.0 of the ENERGY STAR® program requirements for single voltage external AC-DC power supplies[(a)], the power supplies are divided into two categories: low-voltage power supplies and standard power supplies with respect to the nameplate output voltage and current. To be considered a low-voltage power supply, an external power supply must have a nameplate output voltage of less than 6 V and a nameplate output current of more than or equal to 550 mA.

The following tables report the EPA energy efficiency criteria for AC-DC power supplies in active mode for standard models and low voltage models respectively.

Table 11. Energy efficiency criteria for standard models

Nameplate output power (P_{no})	Minimum average efficiency in active mode (expressed as a decimal)
0 to = 1 W	= 0.48 × Pno + 0.140
> 1 to = 49 W	= [0.0626 × ln (P_{no})] + 0.622
> 49 W	= 0.870

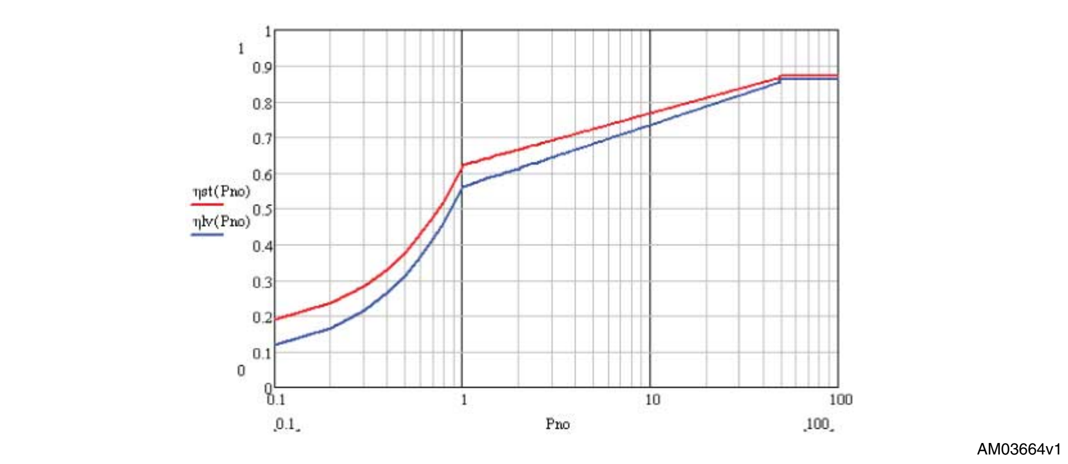
Table 12. Energy efficiency criteria for low-voltage models

Nameplate output power (P_{no})	Minimum average efficiency in active mode (expressed as a decimal)
0 to = 1 W	= 0.497 × Pno + 0.067
> 1 to = 49 W	= [0.075 × ln (P_{no})] + 0.561
> 49 W	= 0.860

The criteria are plotted in *Figure 23*, where the red line depicts the criteria for the standard model and the blue line the criteria for the low voltage model. The PNO axis uses a logarithmic scale.

a. Refer to *Chapter : References*.

Figure 23. ENERGY STAR® efficiency criteria



The presented power supply belongs to the low-voltage power supply category and, in order to be compliant with ENERGY STAR® requirements, needs to have an efficiency higher than 73.37%. For all the considered input voltages, the efficiency (see *Table 8*) results are higher than the recommended value.

2.5 Light load performances

The input power of the converter has been measured in no load conditions for different input voltages. The results are reported in *Table 13*.

Table 13. No load input power

V_{IN_AC} (V_{RMS})	Pin (mW)
90	13.8
115	14.5
150	16
180	17
230	20
265	24

Version 2.0 of the ENERGY STAR® program also takes into consideration the power consumption of the power supply when it is not loaded. The criteria to be compliant with are reported in *Table 14*.

Table 14. Energy consumption criteria for no load

Nameplate output power (P_{no})	Maximum power in no load for AC-DC EPS
0 to = 50 W	< 0.3 W
> 50 W < 250 W	< 0.5 W

The performance of the presented board is much better than the requirement; the power consumption is about twelve times lower than the ENERGY STAR® limit.

Even if the performance seems to be unproportionally better than the requirement, it is worth noting that often AC-DC adapter or battery charger manufacturers have very strict requirements about no load consumption, and if the converter is used as an auxiliary power supply, the line filter is often the big line filter of the entire power supply that significantly increases consumption in standby mode.

Even if the ENERGY STAR® program does not have other requirements regarding light load performance, in order to provide complete information we have also reported the input power and efficiency of the demonstration board in two other low load cases. *Table 15* and *Table 16* show the board's performances when the output load is 25 mW and 50 mW respectively.

Table 15. Low load performance - POUT = 25 mW

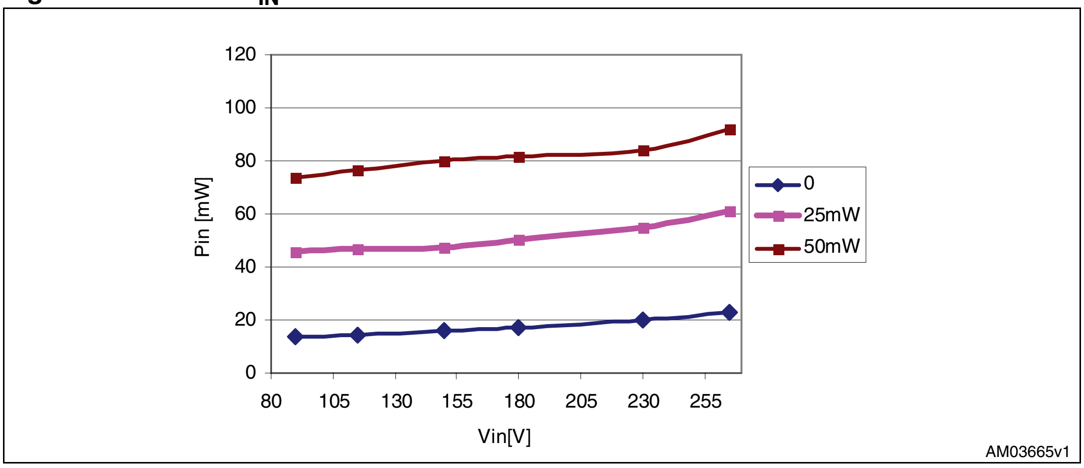
V_{IN_AC}	P_{OUT} (mW)	P_{IN} (mW)	Eff. (%)	P_{IN}-P_{OUT} (mW)
90	25	45.5	54.94505	20.5
115	25	46.8	53.4188	21.8
150	25	47.7	52.4109	22.7
180	25	50.4	49.60317	25.4
230	25	55	45.45455	30
265	25	61	40.98361	36

Table 16. Low load performance - POUT = 50 mW

V_{IN_AC}	P_{OUT} (mW)	P_{IN} (mW)	Eff. (%)	P_{IN}-P_{OUT} (mW)
90	50	73.5	68.02721	23.5
115	50	76.6	65.27415	26.6
150	50	80	62.5	30
180	50	82	60.97561	32
230	50	84	59.52381	34
265	50	92	54.34783	42

Figure 24 reports the input power vs input voltage for no load and low load conditions.

Figure 24. Pin vs V_{IN} at low load

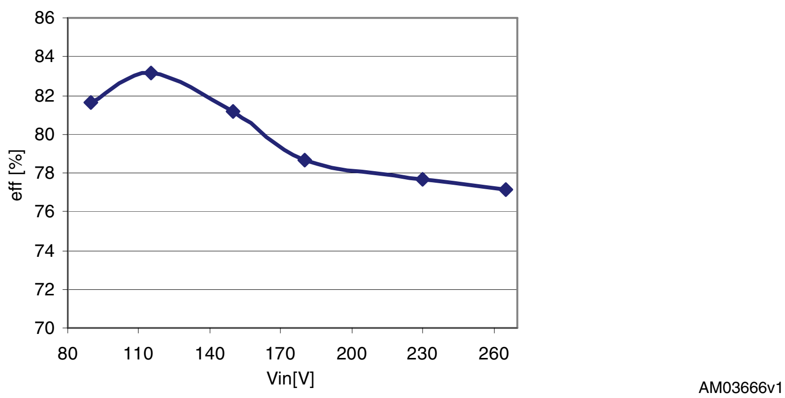


Depending on the equipment supplied, there are several criteria to measure the standby or light load performance of a converter. One of these is the measurement of the output power when the input power is equal to one watt. *Table 17* reports the output power needed to obtain 1 W of input power in different line conditions. *Figure 25* shows the results of this measurement.

Table 17. Output power when the input power is 1 W

V_{IN_AC}	P_{IN} (W)	P_{OUT} (W)	Eff. (%)	P_{IN}-P_{OUT} (W)
90	1	0.81663	81.663	0.18337
115	1	0.83166	83.166	0.16834
150	1	0.81162	81.162	0.18838
180	1	0.78657	78.657	0.21343
230	1	0.77655	77.655	0.22345
265	1	0.77154	77.154	0.22846

Figure 25. Pout vs V_{IN} at Pout = 1 W



2.6 Overload protection

The VIPer28 is a current mode converter. This means that the regulation of the output voltage is made by increasing or decreasing the primary peak current on a cycle-by-cycle basis as a consequence of the increase or decrease of the output power demand.

The peak current is internally sensed and converted into a voltage that is compared with the FB pin voltage. The device is shut down as soon as the two voltages become equal.

When the FB pin voltage reaches V_{FBlin} (3.5 V typical), the drain peak current reaches its maximum value, I_{Dlim} (which is 0.8 A typical or a lower value according to the value of the resistor if connected between the LIM and GND pins).

If the load power demand exceeds the converter's power capability, the FB pin voltage exceeds V_{FBlin} and the device waits for a certain time, fixed by the value of the capacitor C7, before shutting down the system: the internal pull-up is disconnected and the pin starts sourcing a 3 µA current that charges the capacitor.

As the voltage on the feedback pin reaches the V_{FBolp} threshold (4.8 V typical), the VIPer28 stops switching (see *Figure 27*) and is not allowed to switch again until the V_{DD} voltage has fallen below $V_{DD(RESTART)}$ (4.5 V typical) and risen again up to V_{DDon} (14 V typical, see *Figure 26* and *Figure 30*).

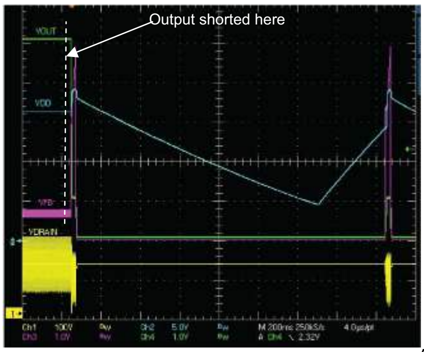
If the short-circuit is not removed, the protection is tripped again and the system works in auto-restart mode (see *Figure 26*, *28* and *30*).

If the overload disappears, the converter resumes working normally at the first V_{DD} recycling, as shown in *Figure 30* and *31*.

C7 is needed because usually the value of the C6 capacitor, coming from the loop stability calculations, is too small to ensure an OLP delay time long enough to bypass the initial output voltage transient at start-up. The value of C7 can be sufficiently high to provide the needed delay, and the value of R12 chosen so that the R12-C7 pole does not affect the stability of the loop.

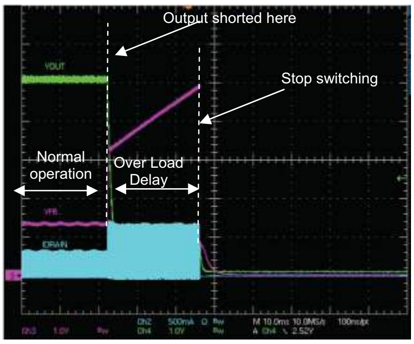
During an overload the converter is operated at a very low duty cycle, being the MOSFET kept in the off state for most of the time. This results in a very low average power throughput, which is safe for the power elements in this condition.

Figure 26. OLP: output short and protection tripping



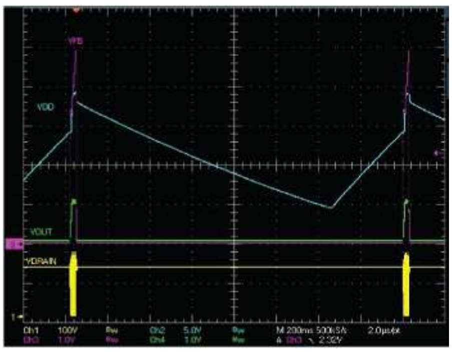
AM03667v1

Figure 27. OLP: output short and protection tripping (zoom on FB pin voltage)



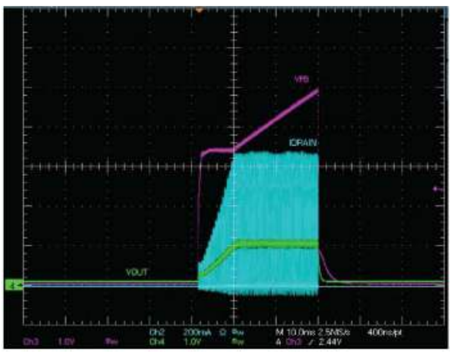
AM03668v1

Figure 28. OLP: steady state (autorestart mode)



AM03691v1

Figure 29. OLP: steady state (zoom on FB pin voltage)

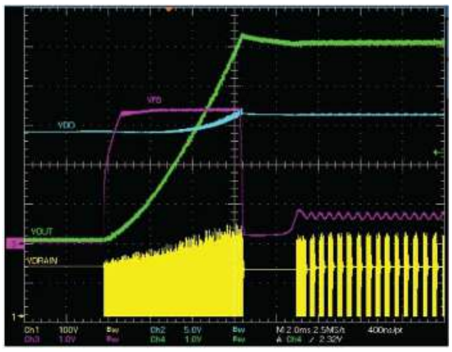


AM03669v1

Figure 30. OLP: steady-state, short removal and restart

AM03670v1

Figure 31. OLP: restart after short removal (zoom)



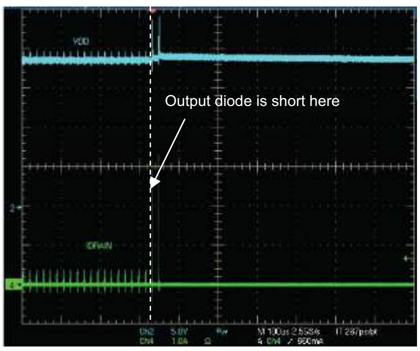
AM03671v1

2.7 Second OCP protection

The VIPer28 is provided with a first adjustable level of primary overcurrent limitation that switches off the power MOSFET if this level is exceeded. This limitation acts cycle by cycle, and its main purpose is to limit the maximum deliverable output power. A second level of primary overcurrent protection is also present, which is not adjustable but fixed to 1.2 A (typical value). If the drain peak current exceeds this second overcurrent protection threshold, the device enters a warning state. If, during the next on time of the power MOSFET, the second level of overcurrent protection is exceeded again, the device assumes that a secondary winding short-circuit or a hard saturation of the transformer is occurring and stops the PWM activity. To re-enable the operation, the V_{DD} pin voltage has to be recycled, which means that V_{DD} has to go down to $V_{DD(RESTART)}$, then rise up to V_{DDon}. At this point the MOSFET restarts switching. If the cause of activation of the second overcurrent protection is still present, the protection is tripped again and the system works in auto-restart mode, resuming normal operation as soon as the cause of the fault is removed and the V_{DD} recycled.

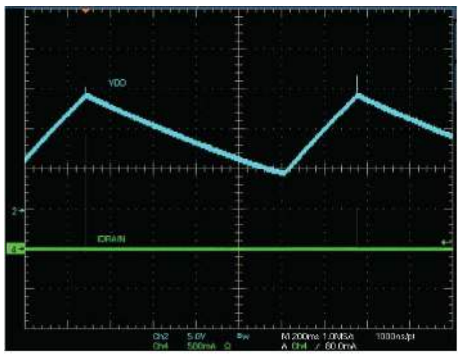
This protection has been tested in different operating conditions, short-circuiting the output diode. The following figures show the behavior of the system during these tests.

Figure 32. Second OCP protection tripping



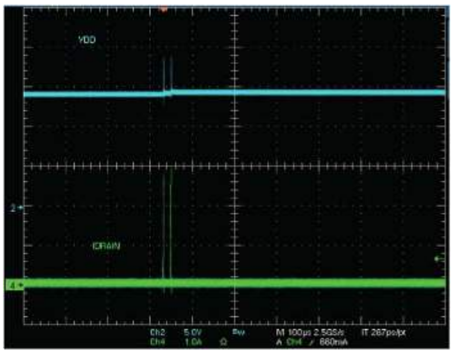
AM03672v1

Figure 33. Operating with secondary winding shorted. Restart mode



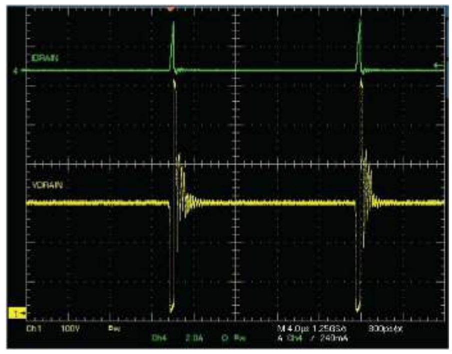
AM03673v1

Figure 34. Operating with secondary winding shorted. Steady state



AM03674v1

Figure 35. Operating with secondary winding shorted. Steady state (zoom)



AM03675v1

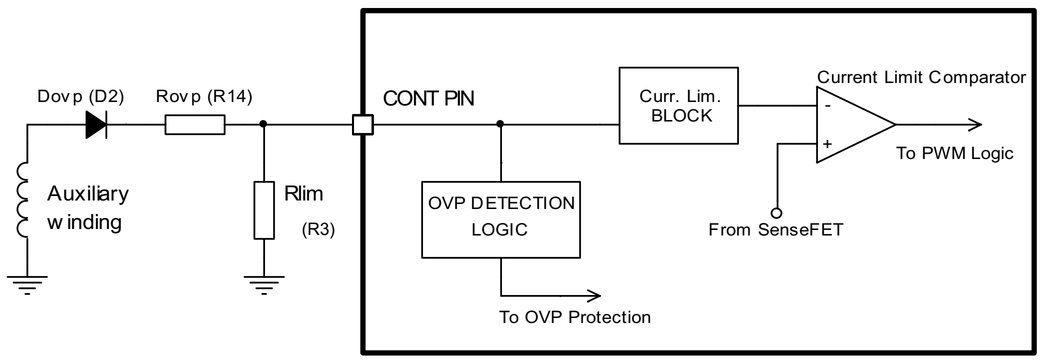
With faults like the ones described, the second OCP protection of the VIPer28 stops the operation after two switching cycles, thus avoiding high currents in both the primary and secondary windings and through the power section of the VIPer28 itself. *Figure 33* shows the operation when a permanent short-circuit is applied on the secondary winding. Most of the time the power section of the VIPer28 is off, eliminating any risk of overheating.

2.8 Output overvoltage protection

During the power MOSFET's off time, the voltage generated by the auxiliary winding tracks the converter's output voltage through the transformer's auxiliary-to-secondary turn ratio.

The diode D2 is forward biased, and the voltage divider made up by R14 and R3 (see *Figure 2* and *Figure 36*) between the auxiliary winding and the CONT pin performs an output voltage monitor function: if the voltage applied to the CONT pin exceeds the internal V_{OVP} threshold (3 V typical) for four consecutive switching cycles, the controller recognizes an overvoltage condition and shuts down the converter. This is done to provide high noise immunity and avoid that spikes erroneously trip the protection. To re-enable operation the V_{DD} voltage has to be recycled.

Figure 36. OVP circuit



AM03676v1

Since the value of R3 has already been selected as a consequence of the maximum output power that the converter has to deliver, R14 can be chosen according to the following formula to reach the desired output overvoltage threshold, V_{OUT_OVP}:

Equation 1

$$R_{OVP\_(R14)} = \frac{R_{LIM\_(R3)}}{V_{OVP}} \cdot \left(\frac{N_{AUX}}{N_{SEC}} \cdot (V_{OUT\_OVP} + V_{\gamma_{D4}} - V_{\gamma_{D2}}) - V_{OVP} \right)$$

where $V_{\gamma D2}$ and $V_{\gamma D4}$ are the forward drop of the diodes D2 and D4 respectively, N_{AUX} and N_{SEC} are the number of turns of the auxiliary and secondary winding respectively. If the overvoltage protection is not required, D2 and R14 can be removed.

The above formula, solved for V_{OUT_OVP}, gives about 7.2 V for the setting of the presented board.

This value has been verified experimentally, short-circuiting the lower resistor (R9) of the output voltage divider and thus producing an output overvoltage, as shown in the figures below. In *Figure 37* one can see that as VOUT reaches the value of 7.2 V, the converter stops switching. In the same figure, the CONT pin voltage and the FB pin voltage are reported. The crest value of the CONT pin voltage during the MOSFET's off time tracks the output voltage. The converter is shut down when the CONT pin voltage reaches the 3 V threshold, as shown in *Figure 38*.

Figure 37. Output overvoltage protection at 115 V_{IN_AC} 0.2 A

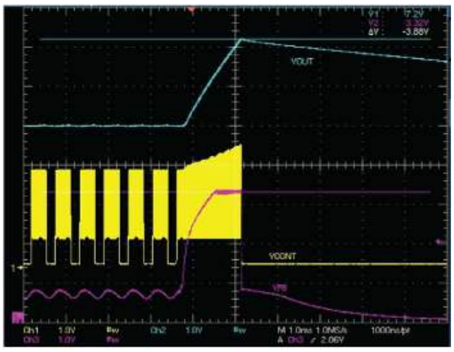
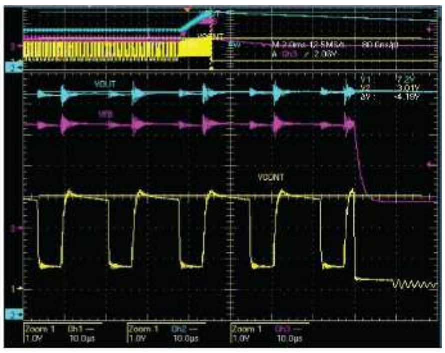


Figure 38. Output voltage ripple at 230 V_{IN_AC} no load



The OVP protection is in auto-restart mode: after the shutdown for protection tripping, the V_{DD} recycles and, if the overvoltage is still present, the protection is tripped again, indefinitely, until the cause of the fault is removed, at which point the converter resumes normal operation, as shown in *Figure 39*.

Figure 39. Auto-restart mode of the overvoltage protection

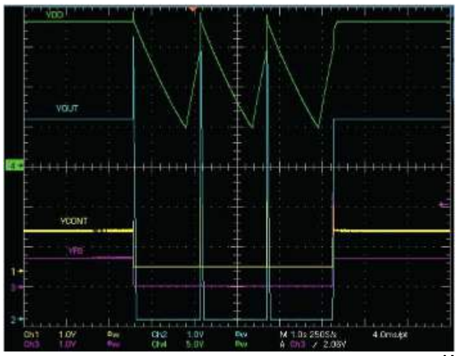
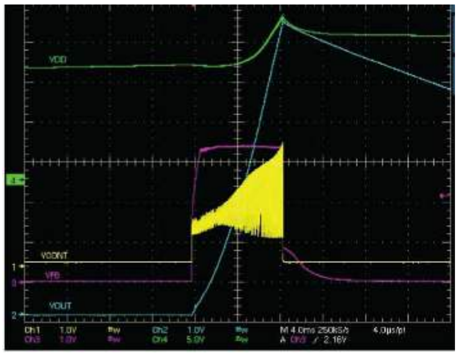


Figure 40. Auto-restart mode of the overvoltage protection (zoom)



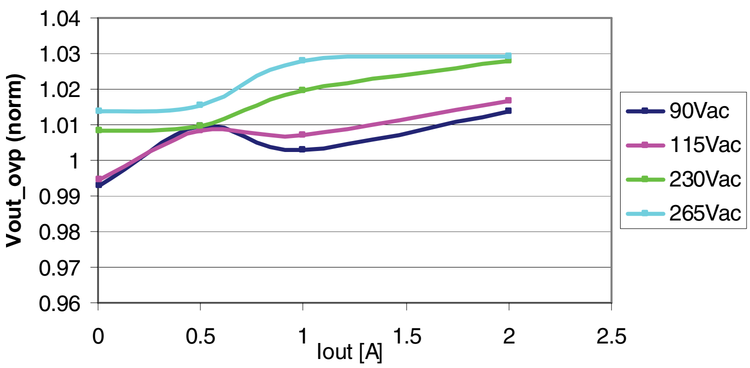
The output OVP threshold has been measured in different line/load conditions and the results are reported in *Table 18*.

Table 18. Output overvoltage threshold at different input/output conditions

V_{OUT_OVP} [V]		V_{IN} [V_{AC}]			
		90	115	230	265
I_{OUT} [A]	0.01	7.15	7.16	7.26	7.3
	0.5	7.27	7.26	7.27	7.31
	1	7.22	7.25	7.34	7.4
	2	7.3	7.32	7.4	7.41

In *Figure 41*, the same results – normalized with respect to the calculated V_{OUT_OVP} threshold (7.2 V) – are plotted in a graphic format to show that in any case the actual threshold is within some percentage of tolerance of the expected value.

Figure 41. Normalized output OVP threshold vs load



2.9 EPT function

Some applications need a power higher than the nominal one to be supplied for a limited time window, during which regulation of the converter has to be maintained.

In the VIPer28 this can be accomplished by the extra power management function, available at the EPT pin. This function requires the use of a capacitor C_{EPT} connected between the pins EPT and GND (capacitor C12 in *Figure 2*).

During normal operation, the EPT pin voltage is zero. When, due to the output power demand, the peak drain current rises over 85% of the I_{Dlim} value (I_{Dlim_EPT}, 0.68 A typical), the C_{EPT} capacitor is charged by an internal 5 µA current on a cycle-by-cycle basis.

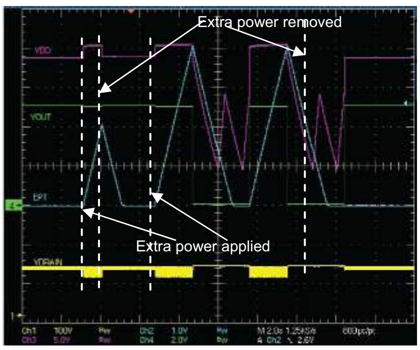
If the extra power demand disappears before the EPT pin voltage has reached the $V_{EPT(STOP)}$ threshold (4 V typical), the capacitor is discharged to zero at the same rate, while the system continues working normally.

If the extra power duration is so long that the C_{EPT} voltage reaches the $V_{EPT(STOP)}$ threshold, the converter is shut down and the C_{EPT} capacitor is discharged to zero by the 5 µA current.

Both cases are illustrated in *Figure 42*, for a load demand changing from 1 A to 3.3 A and back again to 1 A. After shutdown (*Figure 43*), the V_{DD} voltage drops down and has to fall below the $V_{DD(RESTART)}$ threshold (4.5 V typical) before the V_{DD} capacitor can be charged again up to V_{DDon}. In any case, the PWM operation is only enabled again after the EPT pin voltage has dropped below the $V_{EPT(RESTART)}$ threshold (0.6 V typical), as illustrated in *Figure 44*.

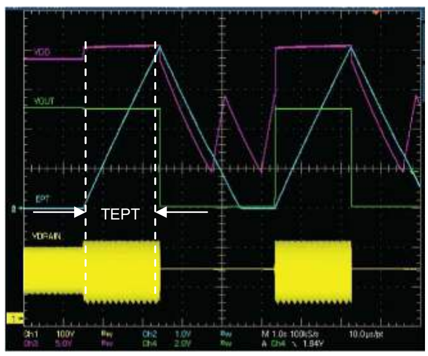
The converter works indefinitely in this on-off condition until the extra power demand is removed (*Figure 42*). This ensures safe operation and avoids overheating in case of repeated overload events.

Figure 42. Extra power applied and removed



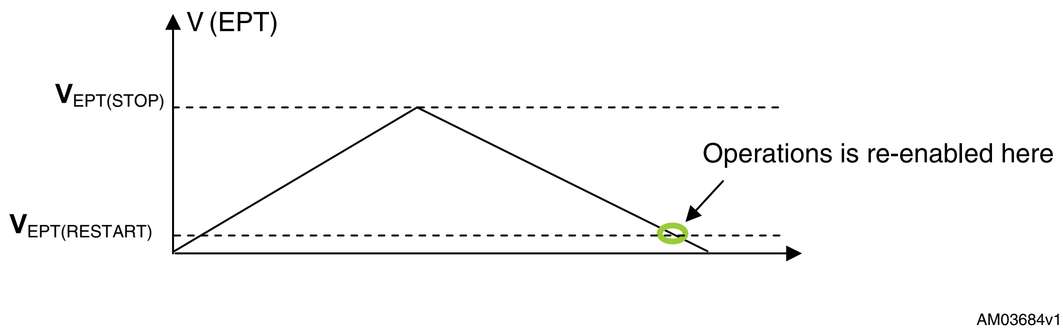
AM03682v1

Figure 43. Extra power applied indefinitely



AM03683v1

Figure 44. EPT thresholds



The time window T_{EPT} during which the extra power is allowed to be supplied can be chosen according to the following formula:

Equation 2

$$C_{EPT} = \frac{I_{EPT} \cdot T_{EPT}}{V_{EPT}}$$

The value of T_{EPT} has to be chosen so as to prevent overheating of the VIPer28 and of the power elements (usually up to a few seconds).

The EPT pin can be connected to GND if the function is not used.

2.10 Thermal measurements

A thermal analysis of the board has been performed using an IR camera. The results are shown in *Figure 45* for a 90 V_{AC} mains input, full load condition.

Figure 45. Thermal measurements at 90 V_{AC} full load, Tamb = 25 °C

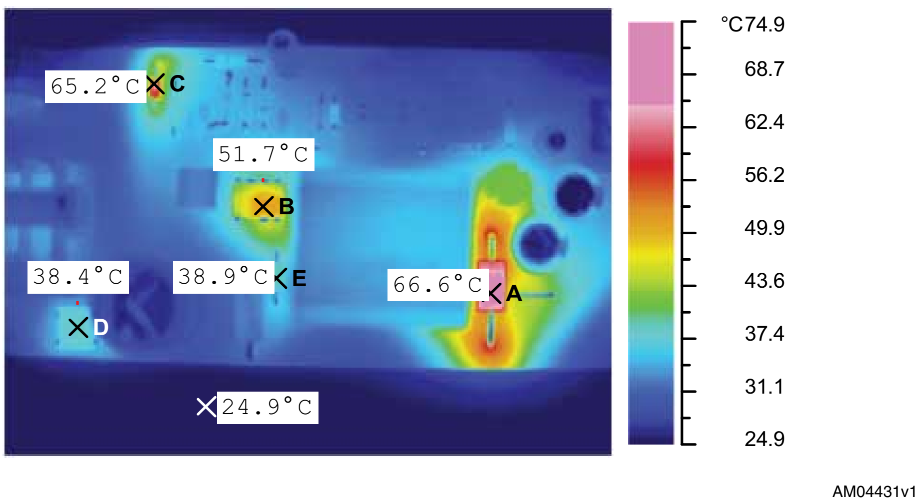


Table 19. Temperature of key components at 115 V_{AC} full load

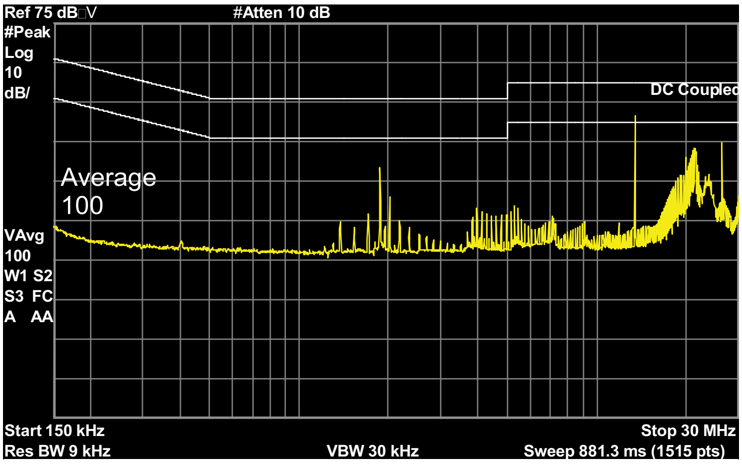
Point	Temperature (in °C)	Reference
A	66.6	D4 (output diode)
B	51.7	VIPer28LN
C	65.2	Dz (zener diode)
D	38.4	BR1 (Diode bridge)
E	38.9	D3 (clamp diode)

2.11 EMI measurements

A pre-compliant test to the EN55022 (class B) European norm has been performed using an EMC analyzer and a LISN.

First of all, an average measurement of the background noise (board disconnected from the mains) has been performed and is reported in *Figure 46*.

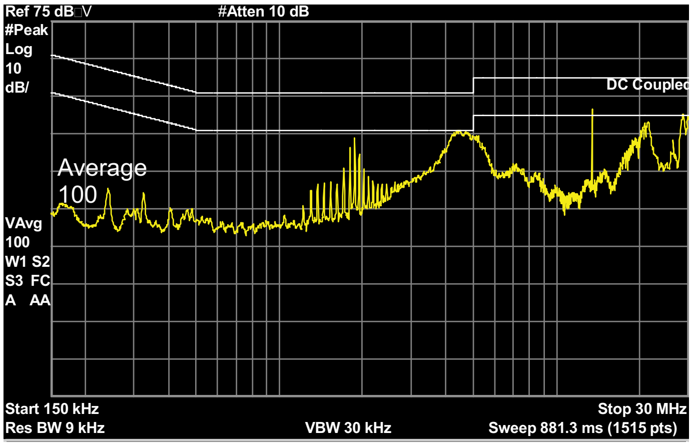
Figure 46. Average measurement of background noise (board disconnected from mains)



AM03685v1

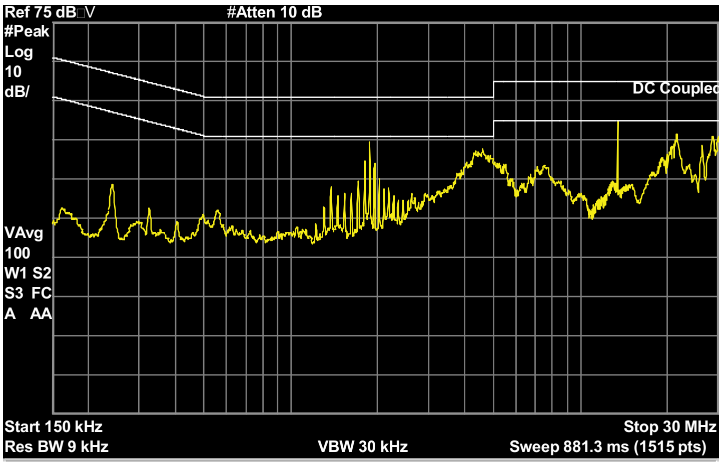
The average EMC measurements at 115 Vac/full load and 230 Vac/full load have then been performed and the results are shown in *Figure 47* and *Figure 48* respectively.

Figure 47. Average measurement at 115 Vac, full load



AM03686v1

Figure 48. Average measurements at 230 Vac, full load



AM03687v1

2.12 Board layout

Figure 49. Top layer

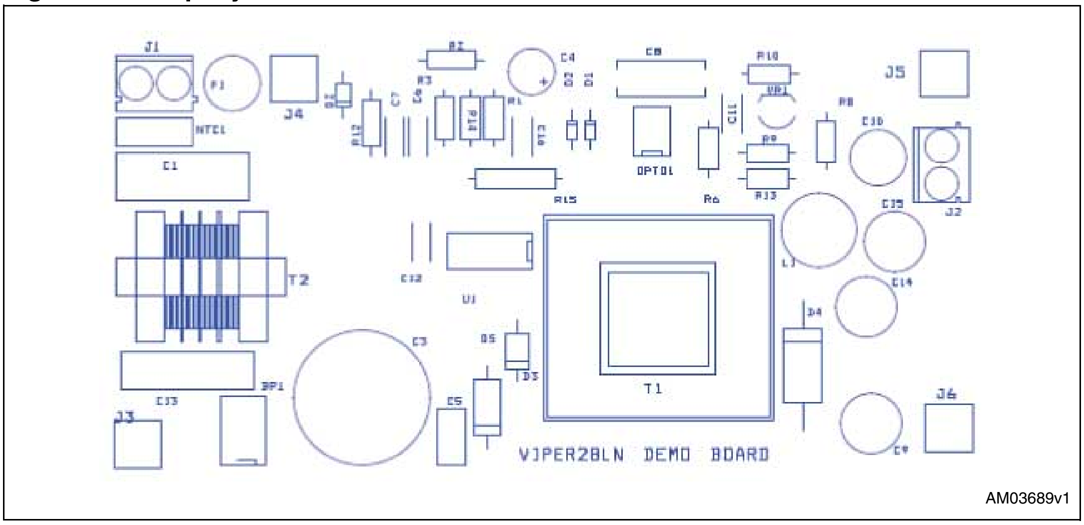
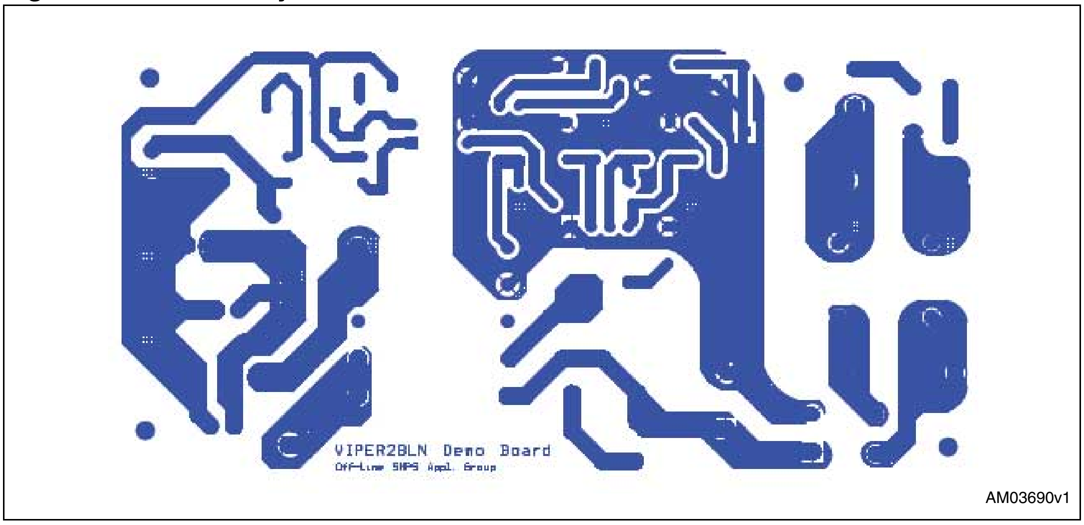


Figure 50. Bottom layer



3 Conclusions

The presented flyback converter is suitable for a wide range of applications. It can be used as an external adapter or as an auxiliary power supply in consumer devices. Special attention has been given to low-load performances and the bench results are good with very low input power in light load conditions. The efficiency performances have been compared with the requirements of the ENERGY STAR® program (version 2.0) for external AC/DC adapters, with very good results showing that the measured active mode efficiency is always higher than the minimum required.

Appendix A Test equipment and measurement of efficiency and low load performance

The converter's input power has been measured using a wattmeter. The wattmeter simultaneously measures the converter's input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument, so it samples the current and voltage and converts them into digital forms. The digital samples are then multiplied, yielding the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher, depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 sec typ.).

Figure 51 shows how the wattmeter is connected to the UUT (unit under test) and to the AC source, as well as the wattmeter's internal block diagram.

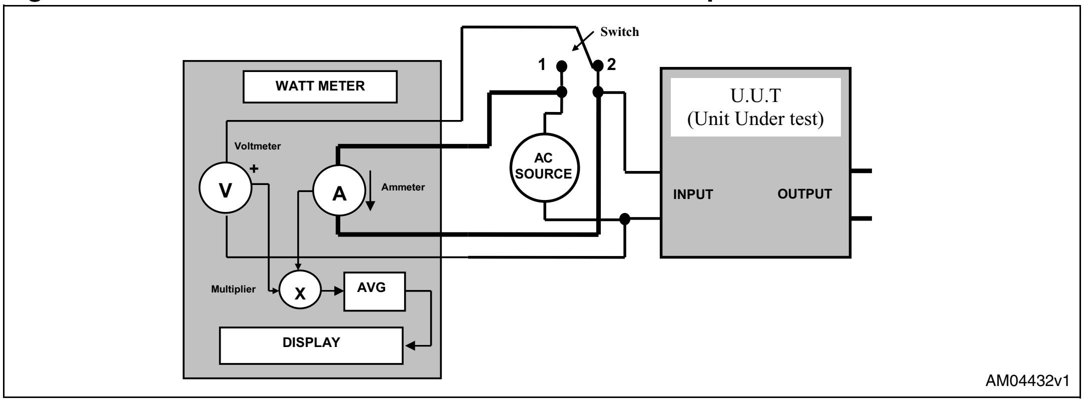
An electronic load has been connected to the output of the power converter (UUT), enabling one to set and measure the converter's load current, while the output voltage has been measured by a voltmeter. The output power is the product of the load current vs. output voltage.

The ratio between the output power, calculated as previously said, and the input power, measured by the wattmeter, is the converter's efficiency. It has been measured in different input/output conditions acting on the AC source and on the electronic load.

A.1 Notes on input power measurement

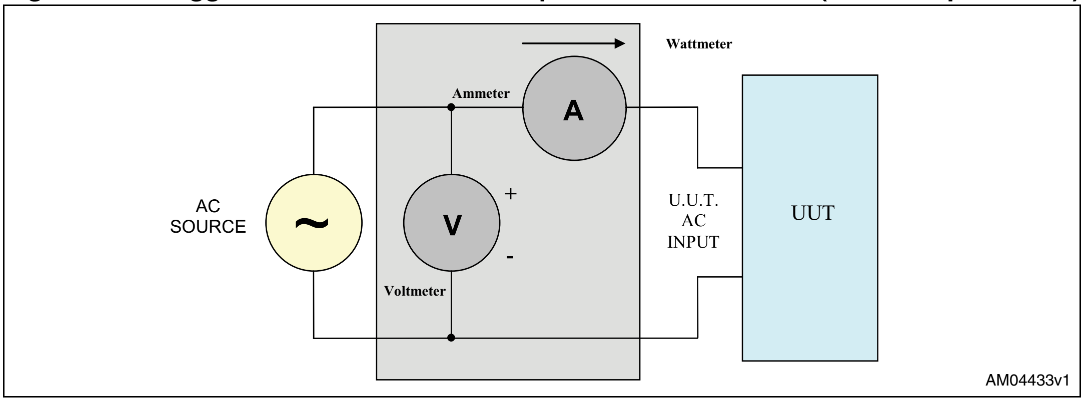
This section shows two possible connections between the wattmeter and the unit under test (UUT) for power measurements, each one represented in *Figure 51* by the connection of the switch either in position 1 or in position 2.

Figure 51. Connection of the UUT to the wattmeter for power measurements



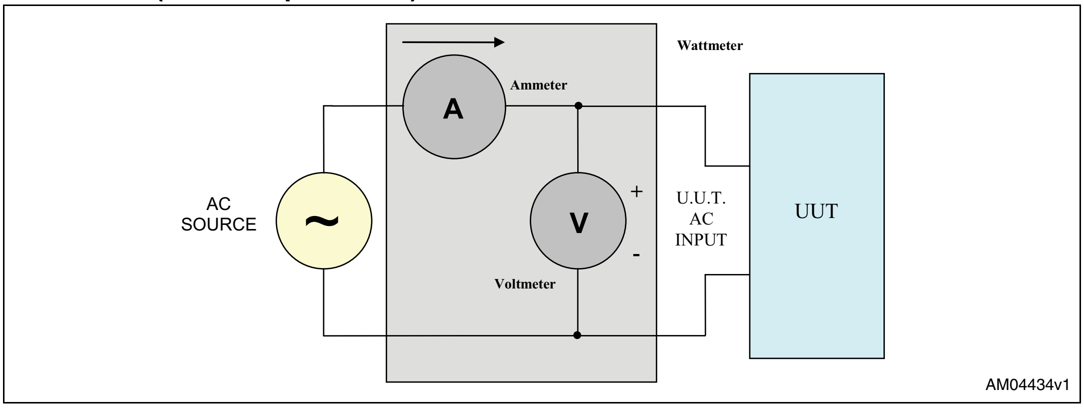
If the switch shown in *Figure 51* is in position 1 (see also the simplified scheme in *Figure 52*), the ammeter's internal shunt resistance (which is higher than zero) has to be taken into account. This resistance produces a voltage drop (then an input measured voltage) higher than the input voltage at the UUT's input. This voltage drop is generally negligible if the UUT's input current is low (for example, when measuring the input power of the UUT at low load conditions), but at heavy load conditions, when the UUT input current increases, the error introduced in the measurement with this setting can be relevant.

Figure 52. Suggested connection for low power measurements (switch in position 1)



In this case, it is advisable to connect the switch shown in *Figure 51* to position 2 (see simplified scheme in *Figure 53*): the UUT's input voltage is measured directly to the UUT's input terminal and the input current does not affect the measured input voltage.

Figure 53. Suggested connection for high power measurements (switch in position 2)



With this setting, the measurement error is introduced by the shunt resistance of the voltmeter, which is not infinite and then causes a leakage current inside the voltmeter itself. This current is measured by the ammeter together with the UUT's input current, but the error is negligible at heavy loads, when the UUT's input current is much higher than the voltmeter's leakage current.

On the other hand, at low load conditions, when the UUT's input current decreases and approaches the voltmeter's leakage current, the measurement error introduced with this setting becomes significant.

To conclude, we could say that the setting shown in *Figure 52* should be used for low loads and stand-by measurements, the setting shown in *Figure 53* for heavy loads and efficiency measurements. In you are not sure which measurement scheme has the least effect on the results, you can try with both and register the input power's lower value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT should be operated at 100% of the nameplate output current output for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements. After this warm-up period, the AC input power should be monitored for a period of 5 minutes to assess the stability of the UUT.

If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5-minute period.

If the AC input power is not stable over a 5-minute period, the average power or accumulated energy should be measured over time for both the AC input and DC output. Some wattmeter models allow integrating the measured input power in a time range and then measuring the energy absorbed by the UUT during the integration time. The average input power is calculated by dividing the measured energy by the integration time itself.

References

1. ENERGY STAR® program requirements for single-voltage, external AC-DC adapter (version 2.0).
2. VIPer28 datasheets.

Revision history

Table 20. Document revision history

Date	Revision	Changes
29-Apr-2010	1	Initial release