TEXAS INSTRUMENTS

ADS5423/24/33 and ADS5411 EVM User Guide

User's Guide

February 2006

SLWU020B

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Overview

This User's Guide document gives a general overview of the ADS5423/24/33 and ADS5411 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module.

1.1 Purpose

The EVM provides a platform for evaluating the ADS5423/24/33 14-bit analog-to-digital converter (ADC) under various signals, references, and supply conditions. This evaluation module also allows the evaluation of the ADS5411, an 11-bit analog-to-digital converter. This document should be used in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Analog input to the ADC is provided via external SMA connectors. The single-ended input the user provides is converted into a differential signal at the input of the device. One input path uses a differential amplifier, while the other input is transformer coupled.

The EVM provides an external SMA connector for input of the ADC clock. The single-ended input the user provides is converted into a differential signal at the input of the device.

Digital output from the EVM is via a 40-pin connector. The digital outputs from the ADC are buffered before going to the connector.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the ADC analog and digital supplies, the external buffer supply, and the differential amplifier supply.

1.3 Power Requirements

The EVM can be powered directly with only two supplies: a 3.3-V supply for the ADC digital driver supply and external buffer supply, and 5 V for the ADC analog supply if using the EVM with transformer coupled analog inputs. If using the differential amplifier analog inputs, ±5 V is required. Provision has also been made to allow the EVM to be powered with independent 3.3-V supplies to provide higher performance.

1.3.1 Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Under voltage may cause improper operation of some or all of the EVM components.

1.4 EVM Operational Procedure

The EVM provides a flexible means of evaluating the ADS5423/24/33 or ADS5411 in a number of modes of operation. A basic setup procedure that can be used as a board confidence check is as follows:

1. Verify all jumper settings against the schematic jumper list in Table 1-1.

Table 1-1. Three Pin Jumper List Table

JUMPER	FUNCTION	LOCATION: PINS 1–2	LOCATION: PINS 2–3	DEFAULT
SJP3	Provides AIN+ source to ADC device	Source provided from T2	Source provided from Diff Amp	1–2
SJP4	Provides AIN– source to ADC device	Source provided from Diff Amp	Source provided from T2	2-3

2. Connect supplies to the EVM as follows:
   +5 V (4.75 V–5.25 V) ADC analog supply to J3 and return to J2.
   +3.3 V (3 V–3.6 V) digital buffer supply to J4 and J1 and return to J6
3. Switch power supplies on.
4. Use a function generator with 50-Ω output to input a 105-MHz, 0-V offset, 1-Vrms sine-wave signal into J5. The frequency of the clock must be within the specification for the device speed grade.
5. Supply an input signal by using a frequency generator with a 50-Ω output to provide a 15.5 MHz, 0-V offset, –1-dBFS amplitude sine-wave signal into J11. A full-scale input tone into the ADC device is a differential 2.2 Vpp and dBFS can be calculated by using the following formula:

$$-\text{dBFS} = 20\log\frac{\text{captured max code} - \text{captured min code}}{2^N}, \text{ where N is the number of bits.}$$

6. The digital pattern on the output connector J9 should now represent a 2's compliment sine wave and can be monitored using a logic analyzer.

Circuit Description

2.1 Schematic Diagram

The schematic diagram for the EVM is attached at the end of this document.

2.2 Circuit Function

The following paragraphs describe the function of EVM circuits. See the relevant data sheet for the device operating characteristics.

2.2.1 Analog Inputs

The EVM can be configured to provide the ADC with either transformer-coupled or differential amplifier inputs from a single-ended source. The default configuration uses the transformer configuration for which the layout has been optimized to give the best performance. The inputs are provided via SMA connectors J11 for transformer coupled input and J10 for differential amplifier input. To setup for one of these options, the EVM must be configured as follows:

1. For a 1:1 transformer coupled input to the ADC, a single ended source is connected to J11. SJP3 has pins 1 and 2 shorted and SJP4 has pins 2 and 3 shorted. This is the default configuration for the EVM.
2. For a differential input into the amplifier, the input source is connected to J10. SJP3 has pins 2 and 3 shorted and SJP4 has pins 1 and 2 shorted. ±5VDC must be connected to the board to provide power to U3 and U4 for this configuration.

2.2.2 Power

Power is supplied to the EVM via banana jack sockets. A separate connection is provided for a +3.3V digital buffer supply (J1 and J2), 5-V analog supply (J3 and J2), ±5-V amplifier supply (J7, J8, and J12), and 3.3-V external buffer supply (J4 and J6). A single 3.3-V buffer supply could be used by installing L6. In this case, connect the 3.3 V to J1 and the return to J2.

2.2.3 Outputs

The data outputs from the ADC are buffered using a Texas Instruments SN74AVC16244. Output data header J9 is a standard 40-pin header on a 100-mil grid, and allows easy connection to a logic analyzer. The connector pinout is listed in Table 2-1. Furthermore, two test points are provided and can be monitored using a multimeter. Description of the test points is listed in Table 2-2.

Table 2-1. Output Connector J9

J9 PIN	DESCRIPTION	J9 PIN	DESCRIPTION
1	CLK	21	DATA BIT 6
2	GND	22	GND
3	NC	23	DATA BIT 7
4	GND	24	GND
5	NC	25	DATA BIT 8
6	GND	26	GND
7	NC	27	DATA BIT 9
8	GND	28	GND
9	DATA BIT 0 (LSB)	29	DATA BIT 10
10	GND	30	GND
11	DATA BIT 1	31	DATA BIT 11
12	GND	32	GND
13	DATA BIT 2	33	DATA BIT 12
14	GND	34	GND
15	DATA BIT 3	35	DATA BIT 13 (MSB)
16	GND	36	GND
17	DATA BIT 4	37	OVERFLOW
18	GND	38	GND
19	DATA BIT 5	39	DRV_{DD}
20	GND	40	GND

Table 2-2. Test Point Description

TEST POINT	FUNCTION
J14	Monitor Vref (AVDD/2)
J17	Monitor DMID (DVDD/2)

Parts List

Table 3-1 lists the parts used in constructing the EVM

Table 3-1. Bill of Materials for EVM

VALUE	QTY	PART NUMBER	VENDOR	REF DES	NOT INSTALLED
CAPACITORS					
0.1 µF, 25 V, +80/–20% Capacitor	4	ECJ-0EF1E104Z	Panasonic	C1, C2, C3, C4	
0.01 µF, 25 V, +80/–20% Capacitor	6	ECJ-0EF1E103Z	Panasonic	C30, C31, C32, C33, C34, C35	
220 pF, 50 V, 5%, Capacitor	6	ECJ-OEC1H221J	Panasonic	C41–C46	
22 pF, 50 V, 5%, Capacitor	1	ECJ-1VC1H220J	Panasonic	C26	
220 pF, 50 V, 5%, Capacitor	3	ECJ-1VC1H221J	Panasonic	C47, C48, C49	
0.01 µF,16 V, 10% Capacitor	7	ECJ-1VB1C103K	Panasonic	C27, C28, C29, C36, C37, C38, C39	
0.1 µF,16 V, 10% Capacitor	12	ECJ-1VB1C104K	Panasonic	C6, C8, C11, C12, C14, C16, C17, C18, C19, C24, C25, C40	
470 pF,50 V, 5% Capacitor	4	ECJ-1VC1H471J	Panasonic	C20, C21, C22, C23	
10 µF, 10 V, 10%, Capacitor	1	ECS-T1AX106R	Panasonic	C15	
33 µF, 10 V, 10% Capacitor	5	ECS-T1AX336R	Panasonic	C5, C7, C9, C10, C13	
RESISTORS					
51.1 Ω	2	CTS_742	CTS	R5, R25	
0 Ω	2	CTS_742	CTS	R7, R8	
24.9 Ω resistor, 1/16 W, 1%	4	ERJ-3EKF24R9V	Panasonic	R6, R11, R12, R27	
49.9 Ω resistor, 1/16 W, 1 %	5	ERJ-6EKF49R9V	Panasonic	R1, R4, R10, R18, R23	R9
36.5 Ω resistor, 1/16 W, 1%	2	ERJ-6EKF36R5V	Panasonic	R2, R3	
499 Ω resistor, 1/16 W, 1%	4	ERJ-6EKF4990V	Panasonic	R14, R15, R16, R17	
0 Ω resistor, 1/16 W, 1%	1	ERJ-6ENF0R00V	Panasonic	R24	
200 Ω resistor, 1/16 W, 1%	0	ERJ-3RKF2000X	Panasonic		R13
FERRITE BEAD, JUMPER, TRANSFORMER, JACKS, CONN etc.					
Ferrite Bead	5	EXC-ML32A680U	Minicircuits	L1–L5	
ADT1-1WT	1	ADT1-1WT	Minicircuits	T2	
ADT4-1WT	1	ADT4-1WT	NEWARK	T3	
SMA End Small	3	16F3627	Keystone	J5, J10, J11	
Red Test Point	1	5001K-ND	Keystone	J14	
Black Test Point	1	5000K-ND	Allied	J17	
Red Banana Jack	5	ST-351A	Allied	J1, J3, J4, J8, J12	
Black Banana Jack	3	ST-351B	Samtec	J2, J6, J7	
40-Pin IDC Connector	1	TSW-120-07-L-D		J9	
3 Circuit Jumper	2			SJP3, SJP4	

Table 3-1. Bill of Materials for EVM (continued)

VALUE	QTY	PART NUMBER	VENDOR	REF DES	NOT INSTALLED
ICs					
ADS5423/24/33 or ADS5411	1	ADS5423/24/33 or ADS5411	Texas Instruments	U1	
SN74AVC16244	1	SN74AVC16244DGG	Texas Instruments	U2	
THS4503	1	THS4503	Texas Instruments	U3	
THS4601	1	THS4601	Texas Instruments	U4	
Surface Mount Jumper Location: SJP3 (2–1), SJP4 (2–3)					

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

4.1 PCB Layout

The EVM is constructed on a 6-layer, 4.77-inch × 3.4-inch, 0.062-inch thick PCB using FR-4 material. The individual layers are shown in Figure 4-1 through Figure 4-6.

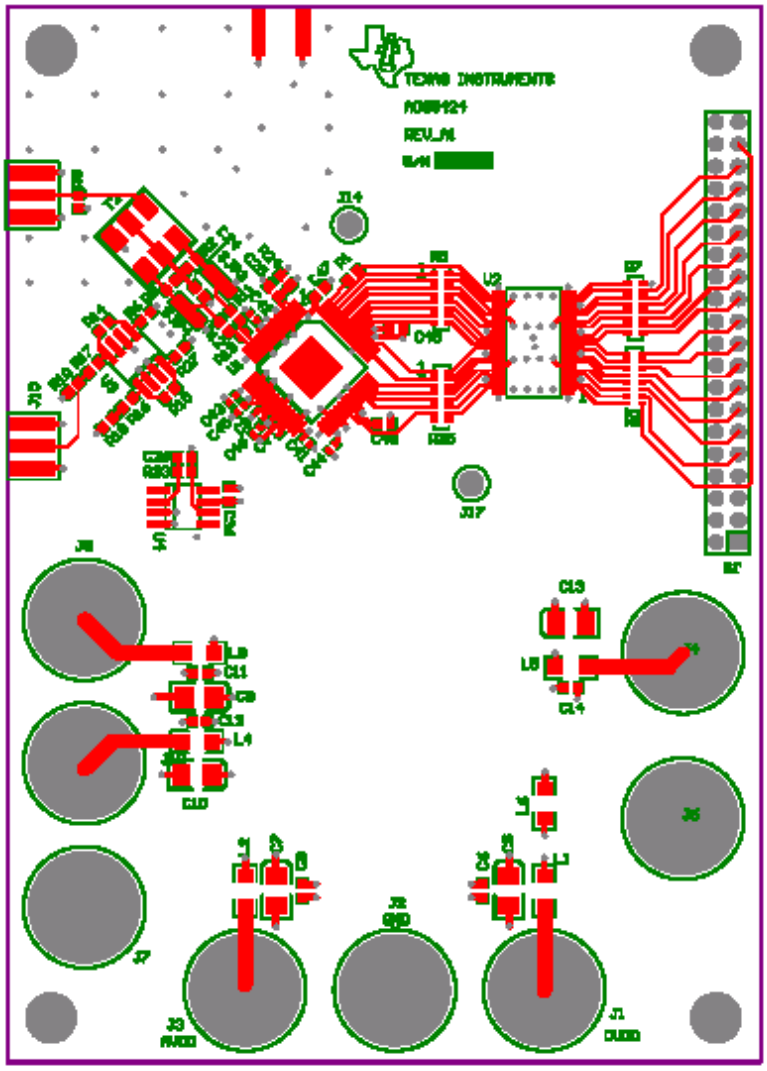


Figure 4-1. Top Layer

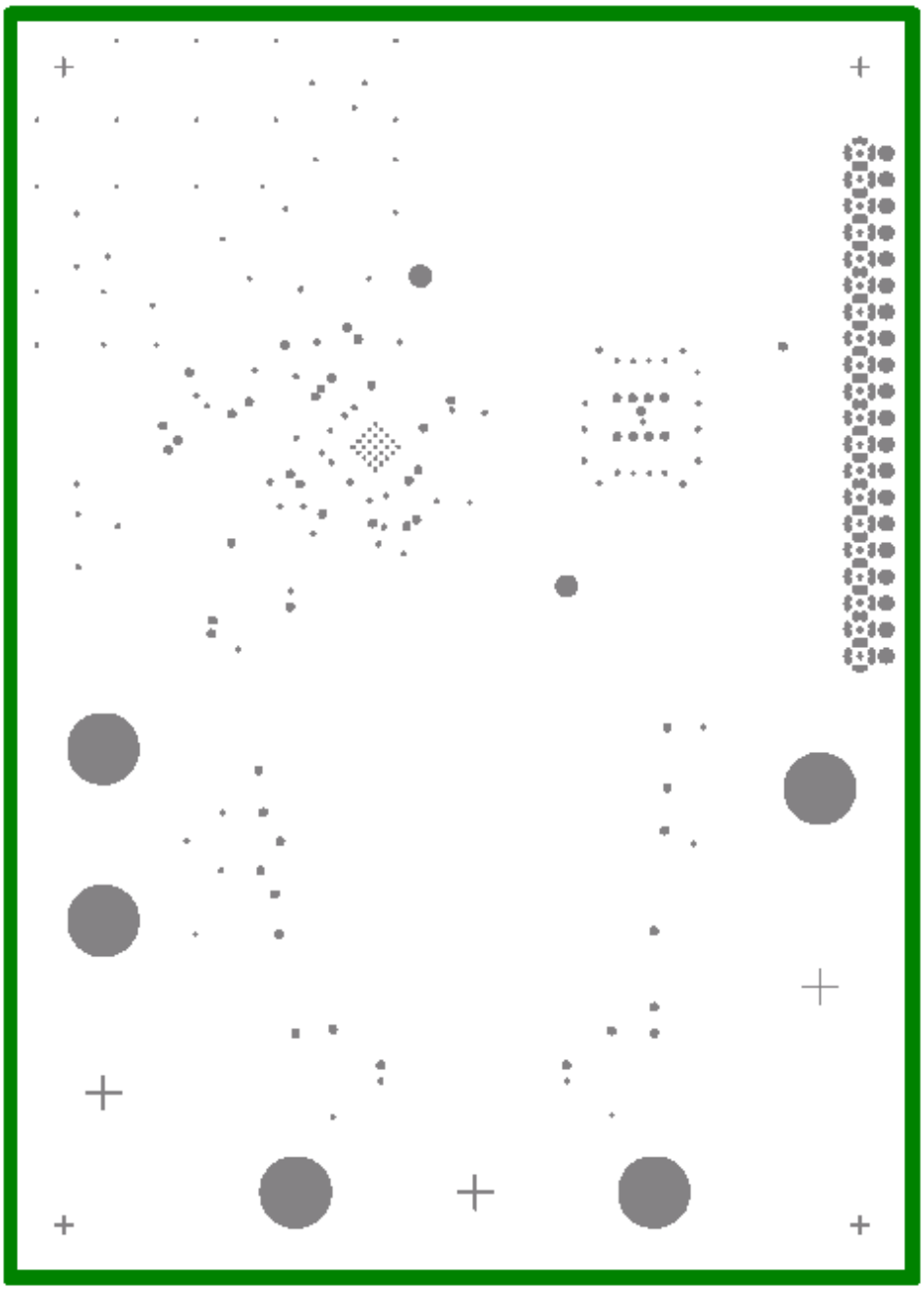


Figure 4-2. Layer 2, Ground Plane

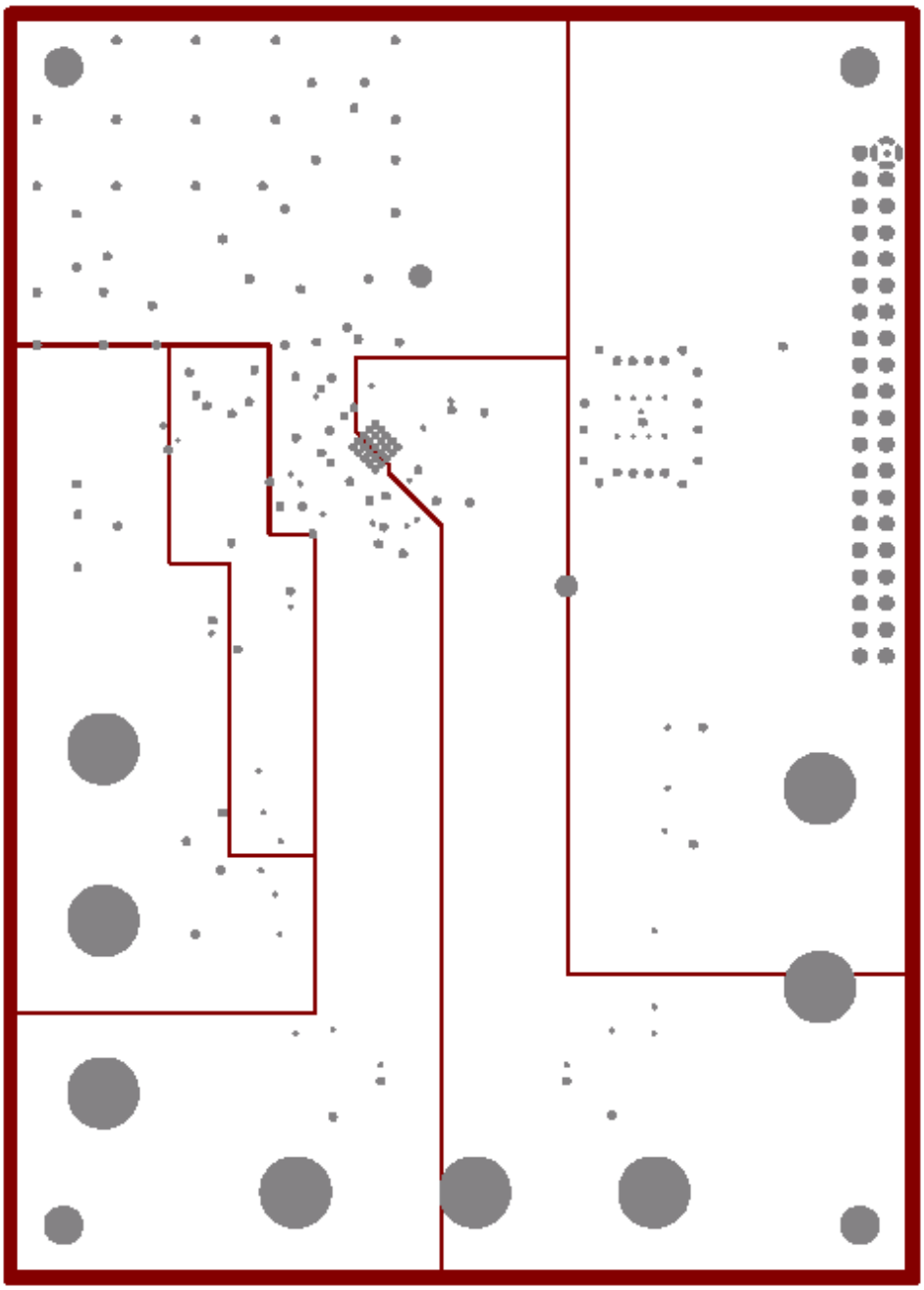


Figure 4-3. Layer 3, Power Plane #1

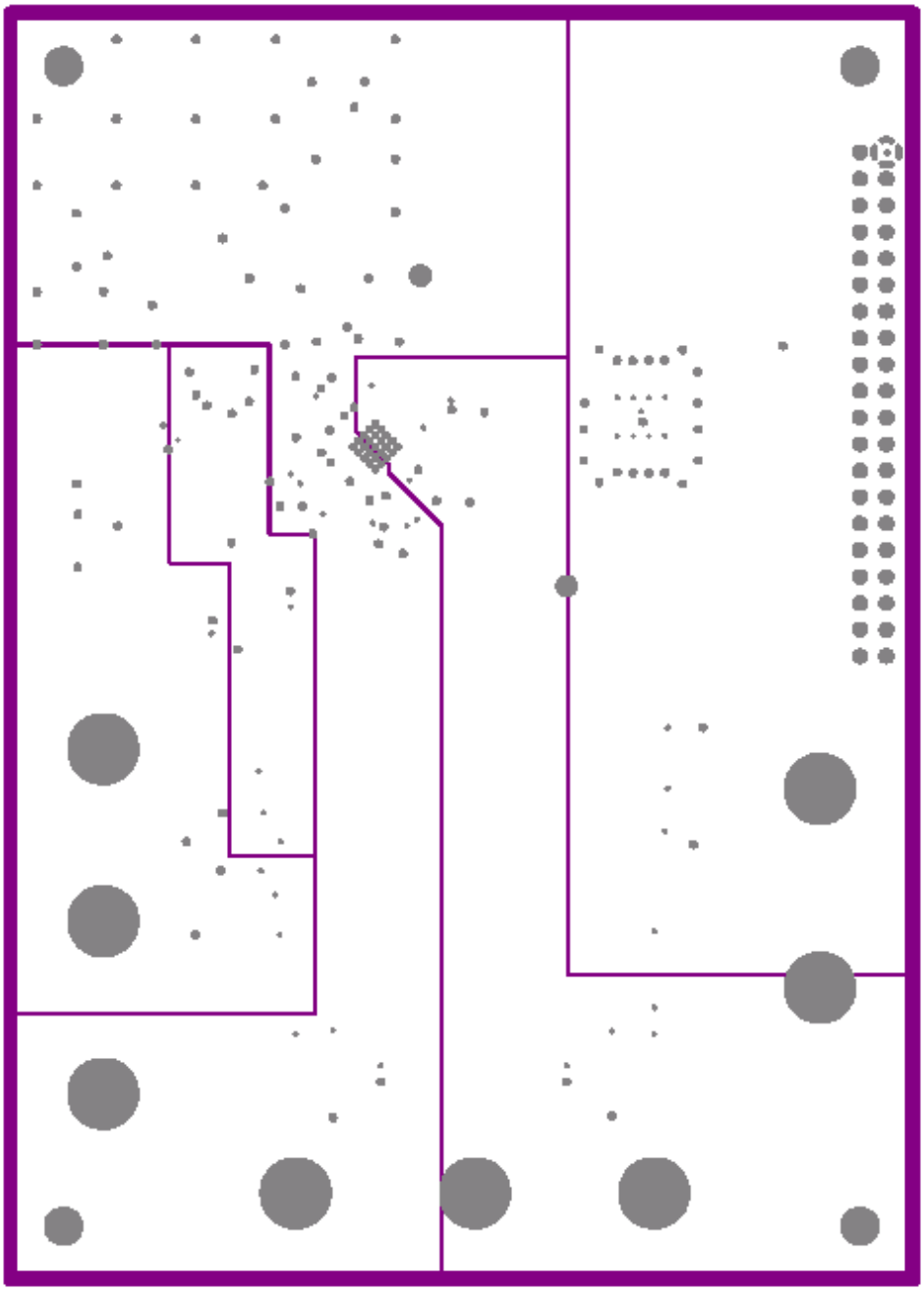


Figure 4-4. Layer 4, Power Plane #2

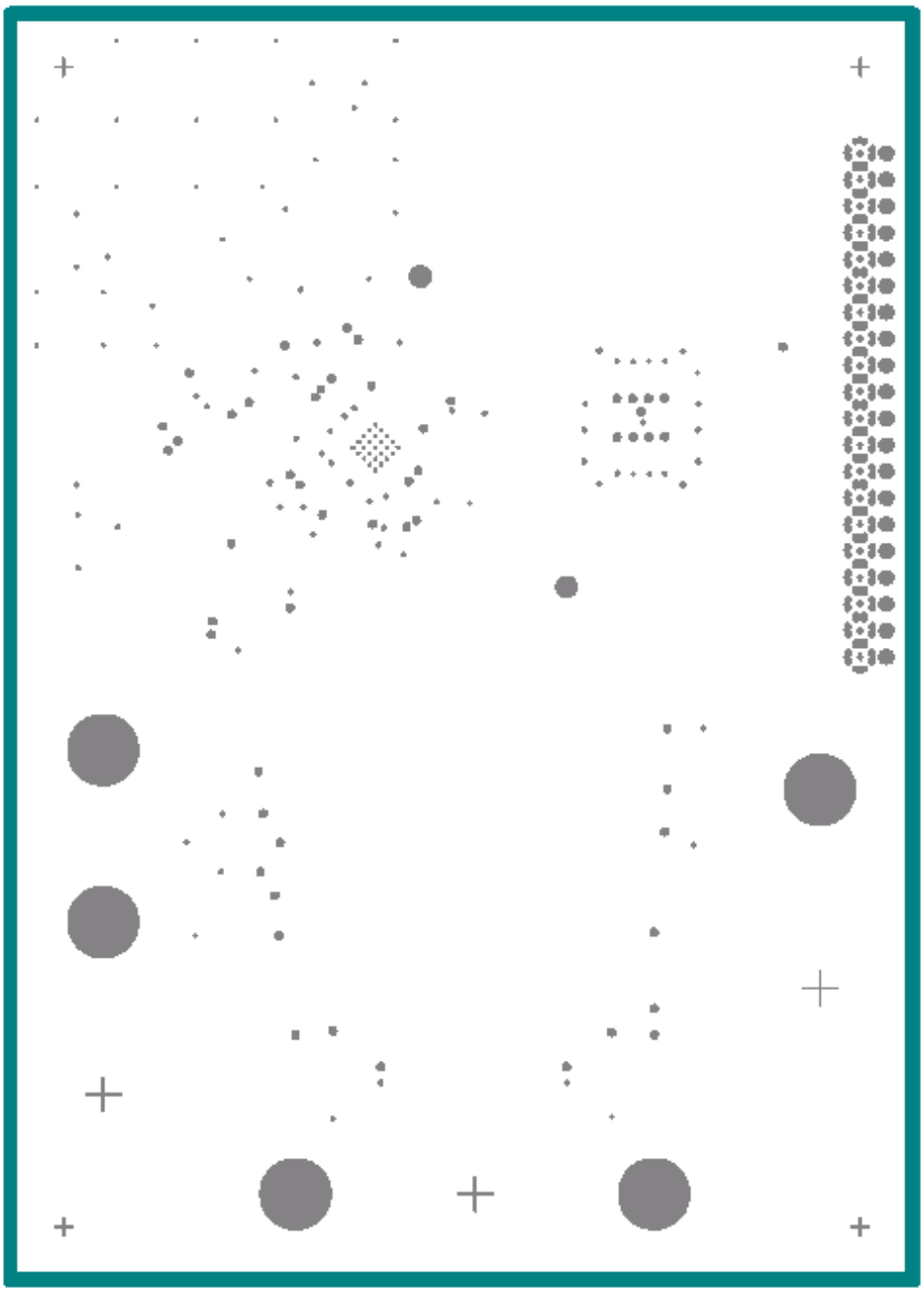


Figure 4-5. Layer 5, Ground Plane

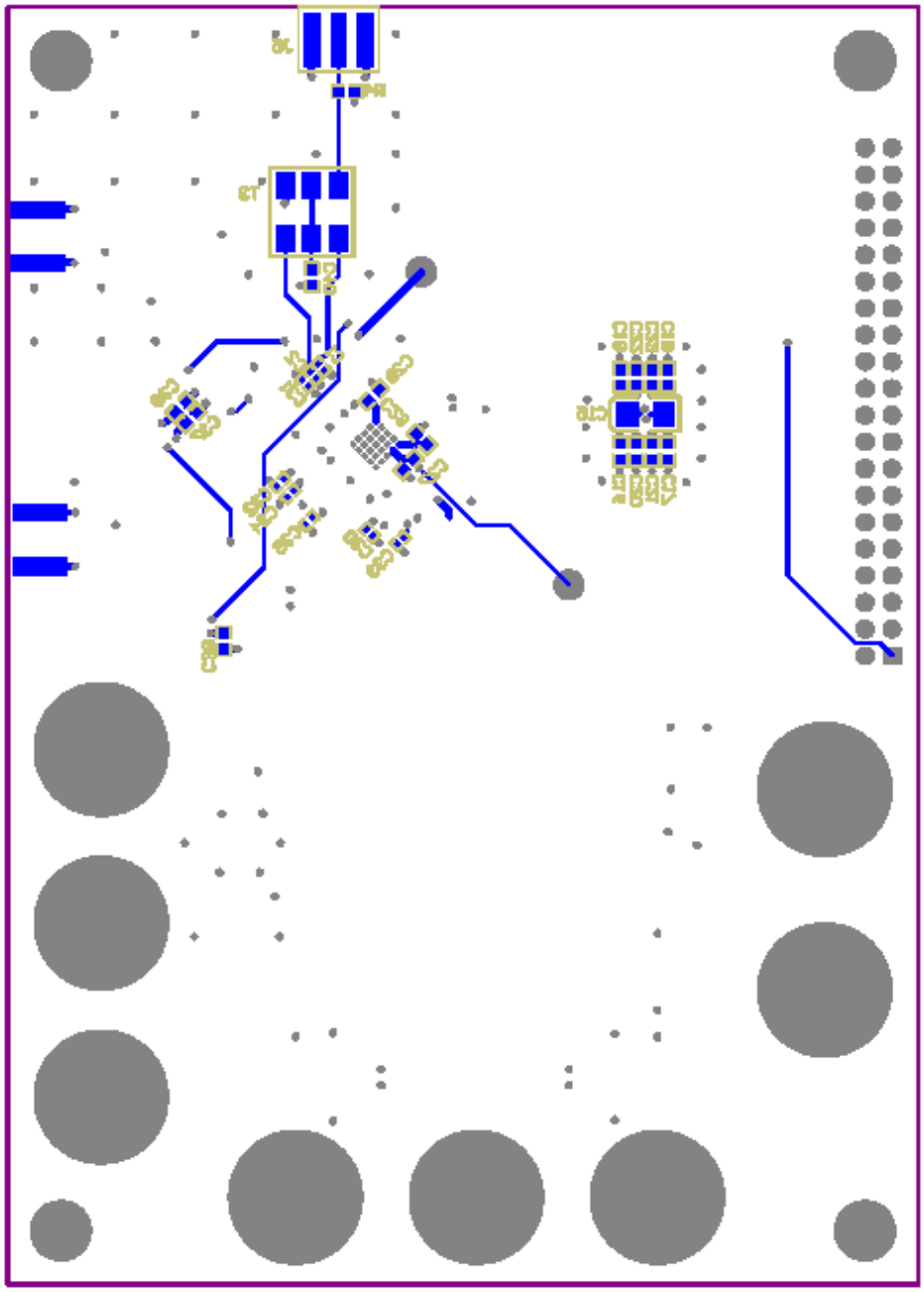
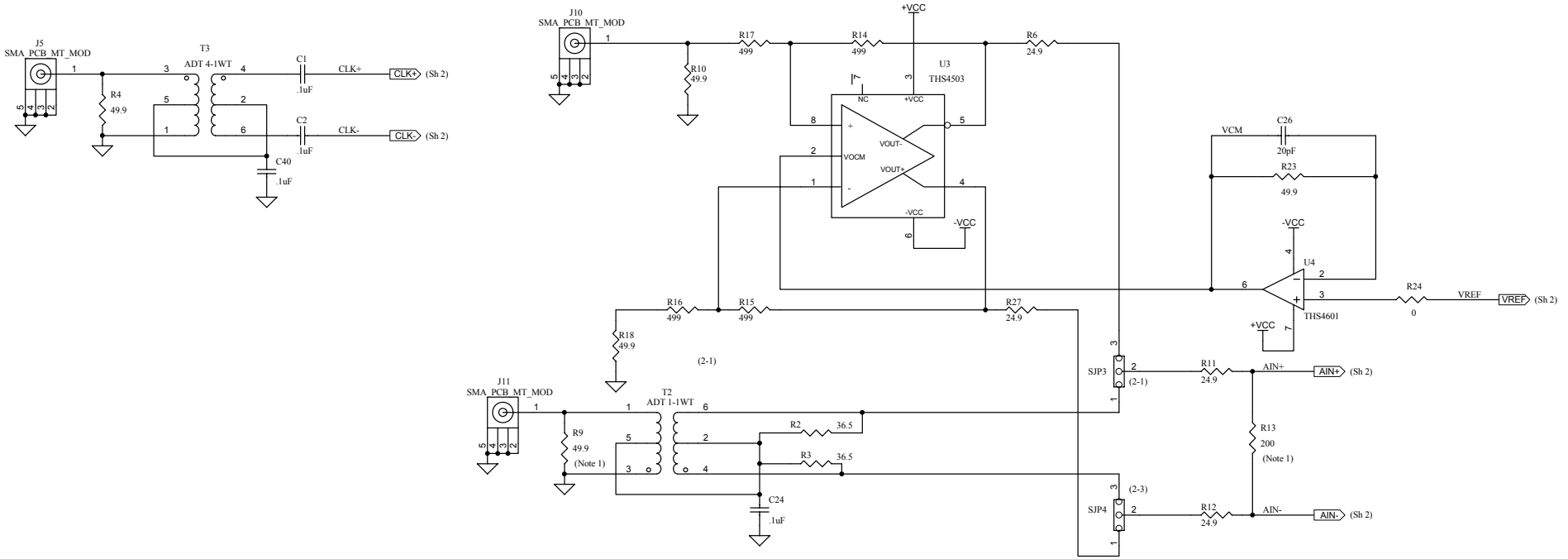


Figure 4-6. Layer 6, Bottom Layer

4.2 Schematics



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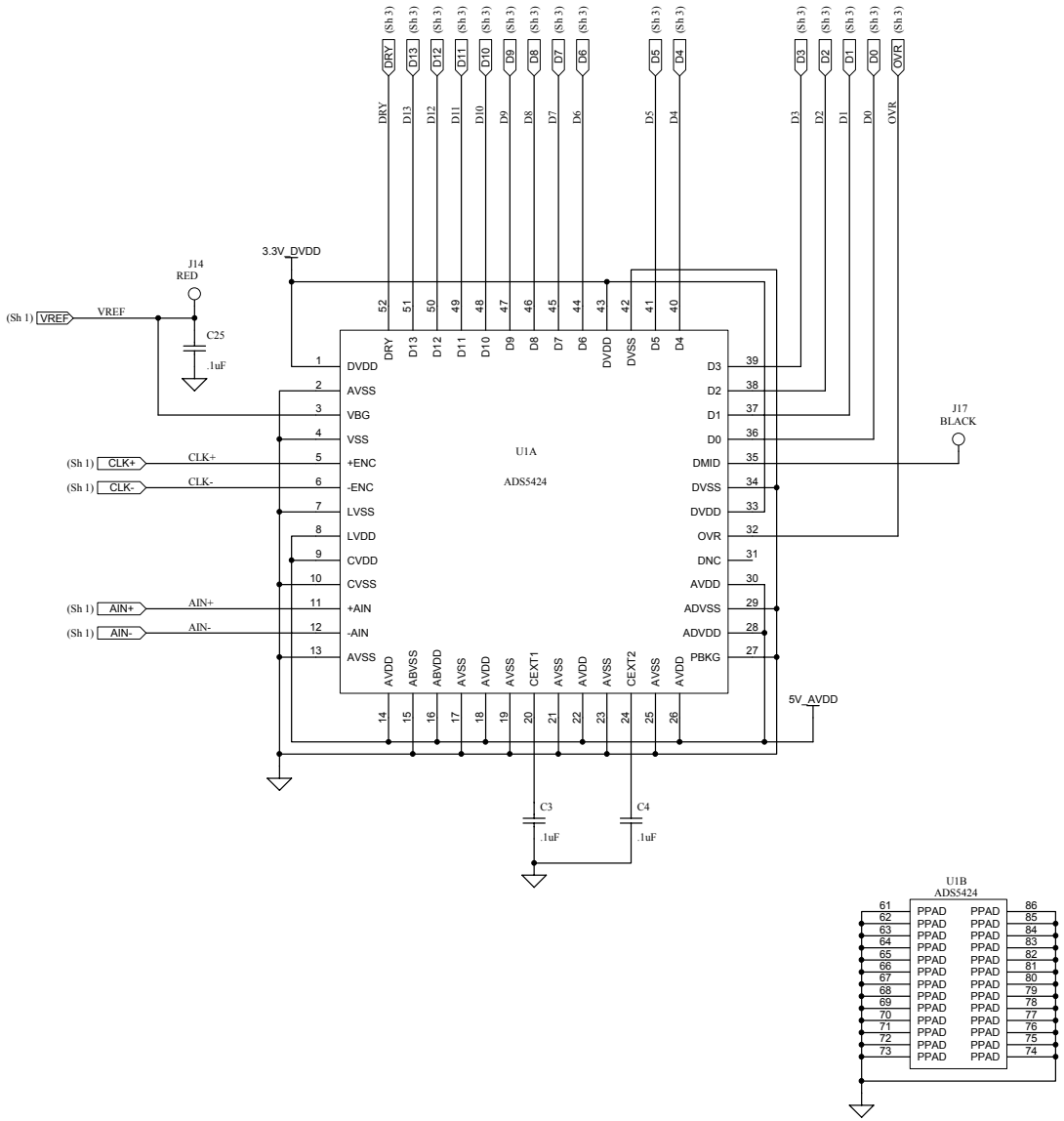
Title:	ADS5424		
Engineer: J. SETON	DOCUMENTCONTROL #		REV: A
Drawn By: Y. DEWONCK	DATE: 8-Dec-2004	SIZE:	SHEET: 1 OF: 4
FILE:			



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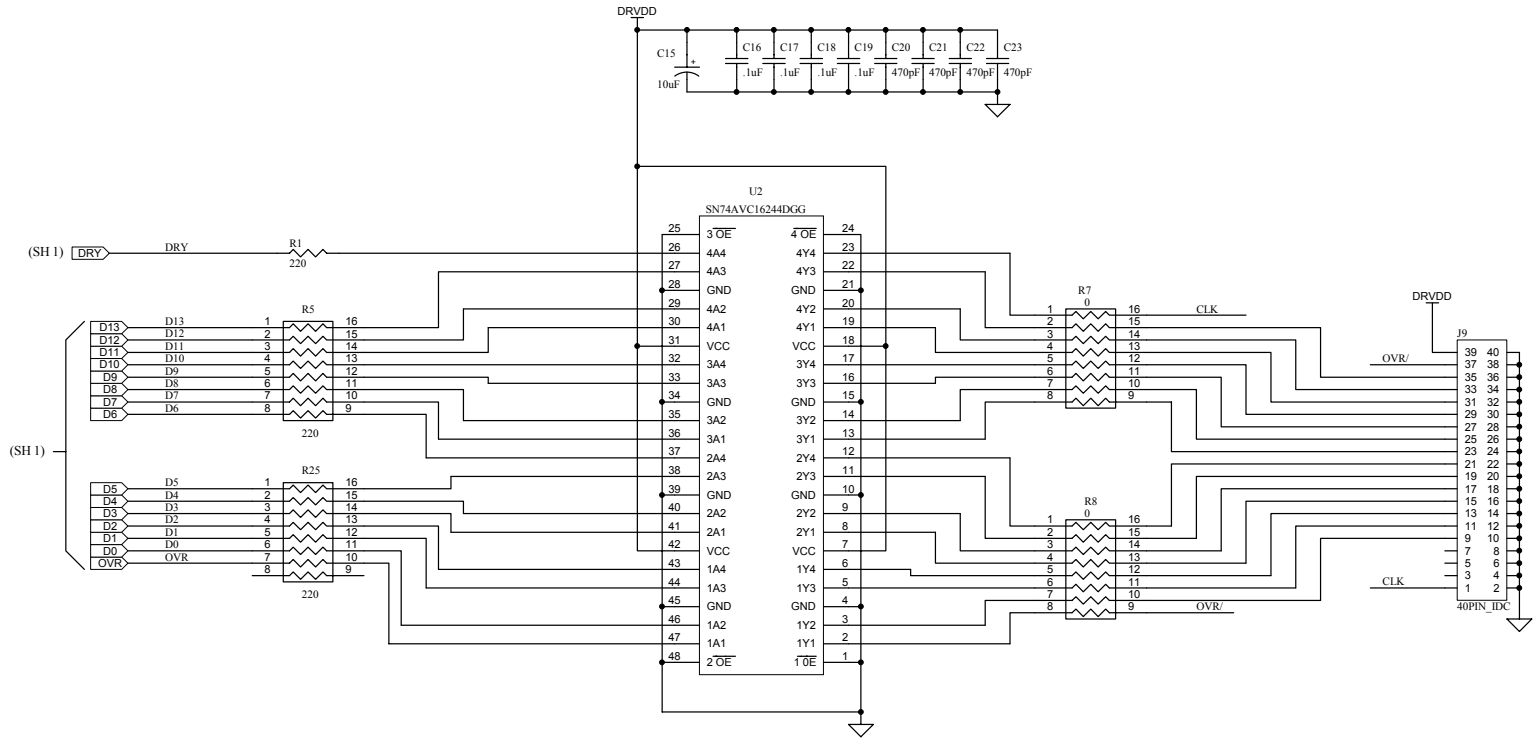

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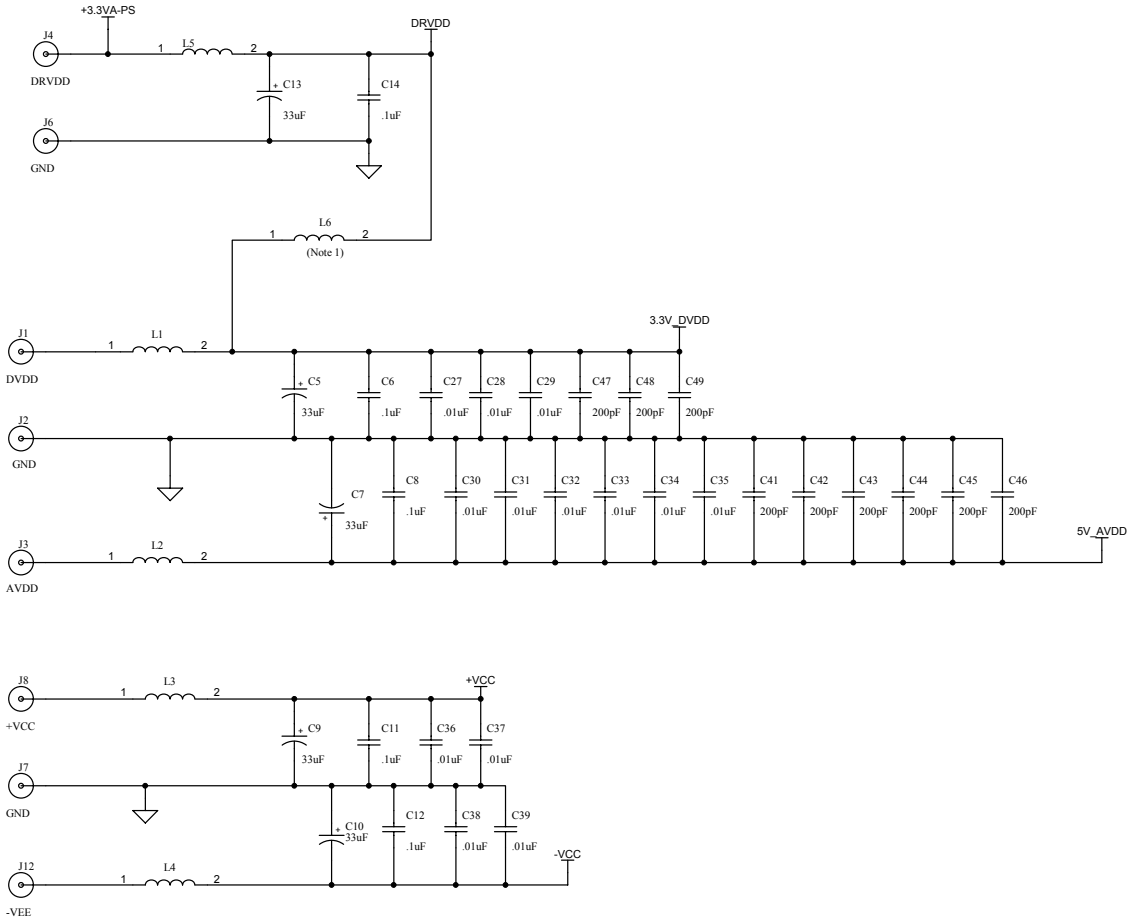

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the AVDD voltage range of –0.3 V to 3.8 V and the DVDD voltage range of –0.3 V to 3.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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