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FAIRCHILD SEMICONDUCTOR®

November 2013

FCB11N60

N-Channel SuperFET® MOSFET

600 V, 11 A, 380 mΩ

Features

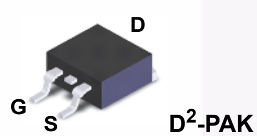
- 650V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 320 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 40 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 95 pF)
- 100% Avalanche Tested
- RoHS Compliant

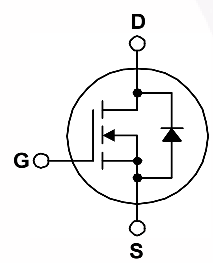
Application

- Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCB11N60TM	Unit
V_{DSS}	Drain to Source Voltage		600	V
I_D	Drain Current	- Continuous (T_C = 25°C)	11	A
		- Continuous (T_C = 100°C)	7	
I_{DM}	Drain Current	- Pulsed (Note 1)	33	A
V_{GSS}	Gate to Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		340	mJ
I_{AR}	Avalanche Current (Note 1)		11.0	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		12.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)	125	W
		- Derate Above 25°C	1.0	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCB11N60TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (1 in² Pad of 2-oz Copper), Max.	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCB11N60TM	FCB11N60	D^2-PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA, $T_C = 25^oC$	600	-	-	V
		V_{GS} = 0 V, I_D = 250 µA, $T_C = 150^oC$	-	650	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25^oC	-	0.6	-	$V/^oC$
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 11 A	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 480 V, V_{GS} = 0 V, $T_C = 125^oC$	-	-	10	µA
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 µA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 5.5 A	-	0.32	0.38	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 5.5 A	-	9.7	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	-	1148	1490	pF
C_{oss}	Output Capacitance		-	671	870	pF
C_{rss}	Reverse Transfer Capacitance		-	63	-	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	-	35	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	95	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 11 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	-	34	80	ns
t_r	Turn-On Rise Time		-	98	205	ns
$t_{d(off)}$	Turn-Off Delay Time		-	119	250	ns
t_f	Turn-Off Fall Time		-	56	120	ns
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 480 V, I_D = 11 A, V_{GS} = 10 V (Note 4)	-	40	52	nC
Q_{gs}	Gate to Source Gate Charge		-	7.2	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	21	-	nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	11	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	33	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 11 A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 11 A, dI_F/dt = 100 A/µs	-	390	-	ns
Q_{rr}	Reverse Recovery Charge		-	5.7	-	µC

Notes:
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 5.51 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq$ 11 A, di/dt $\leq$ 200 A/µs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

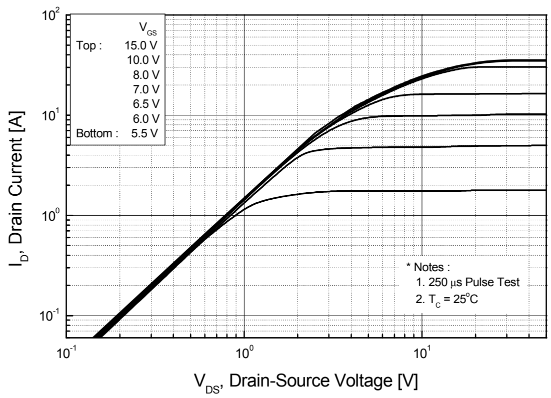


Figure 2. Transfer Characteristics

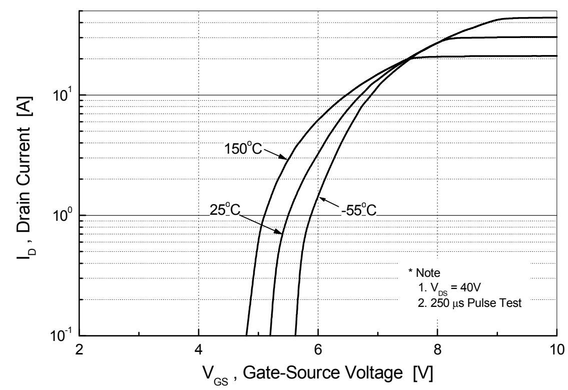


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

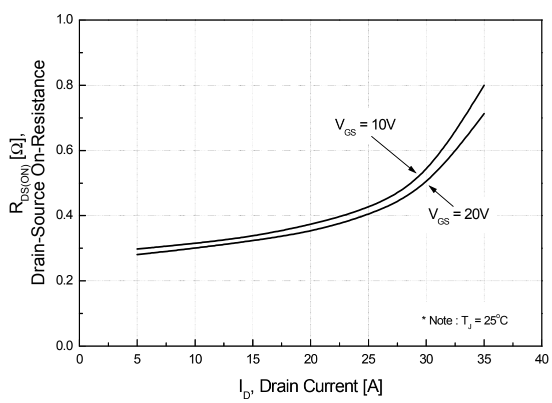


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

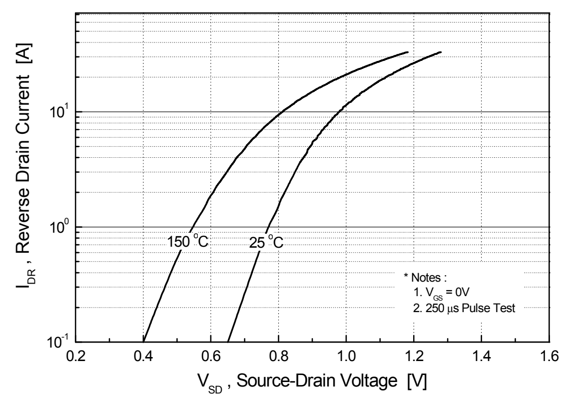


Figure 5. Capacitance Characteristics

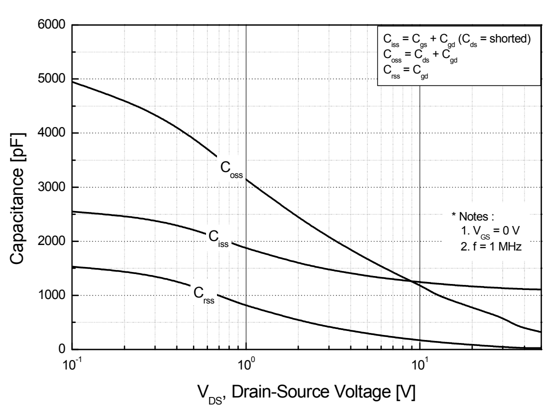
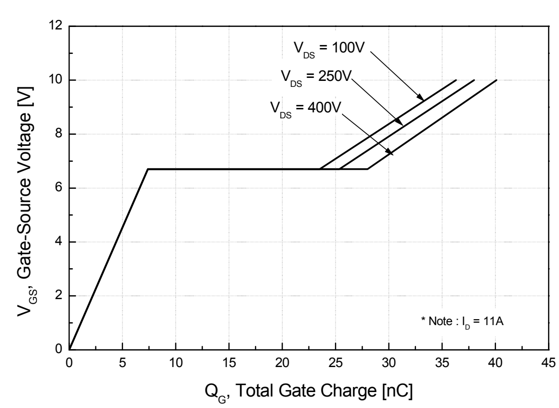


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

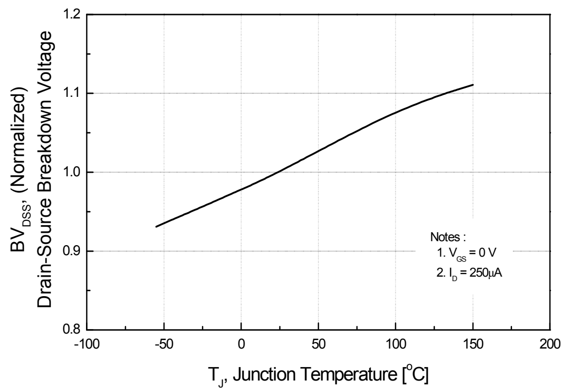


Figure 8. On-Resistance Variation vs. Temperature

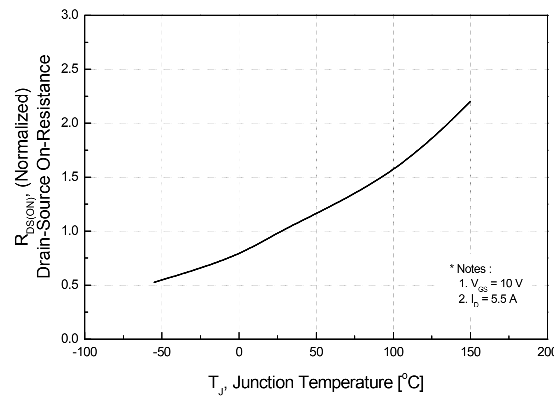


Figure 9. Maximum Safe Operating Area

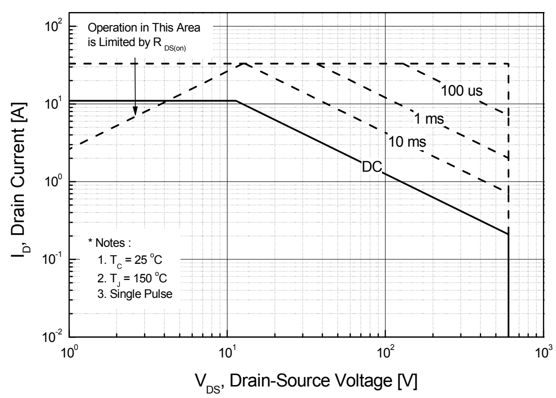


Figure 10. Maximum Drain Current vs. Case Temperature

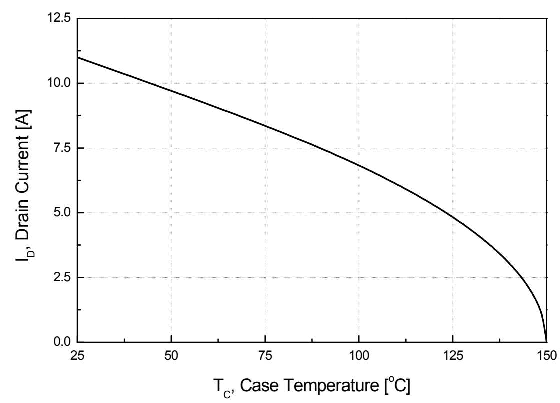
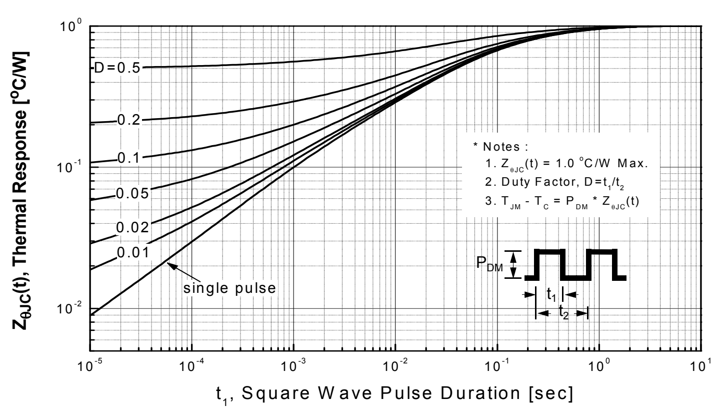


Figure 11. Transient Thermal Response Curve



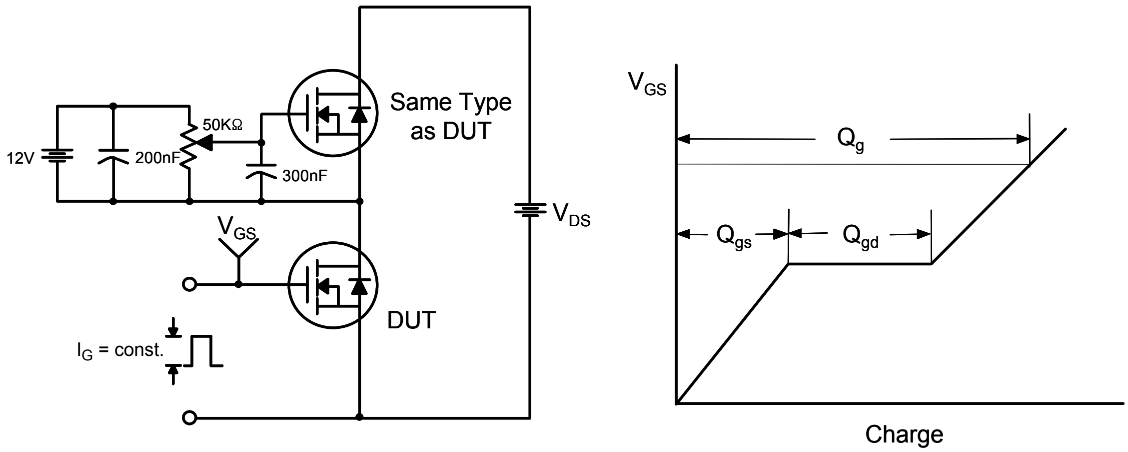


Figure 12. Gate Charge Test Circuit & Waveform

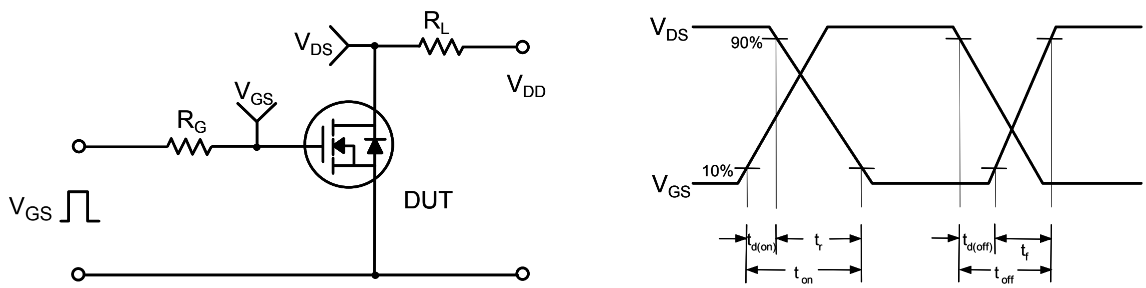


Figure 13. Resistive Switching Test Circuit & Waveforms

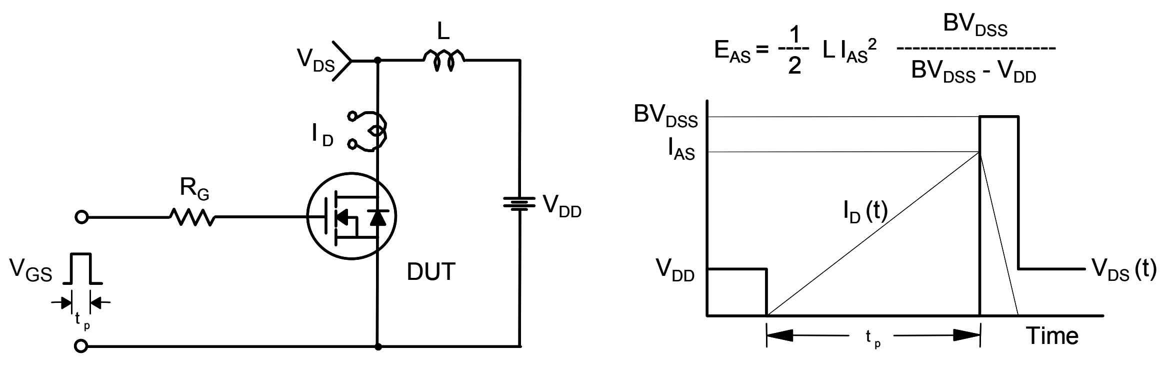


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

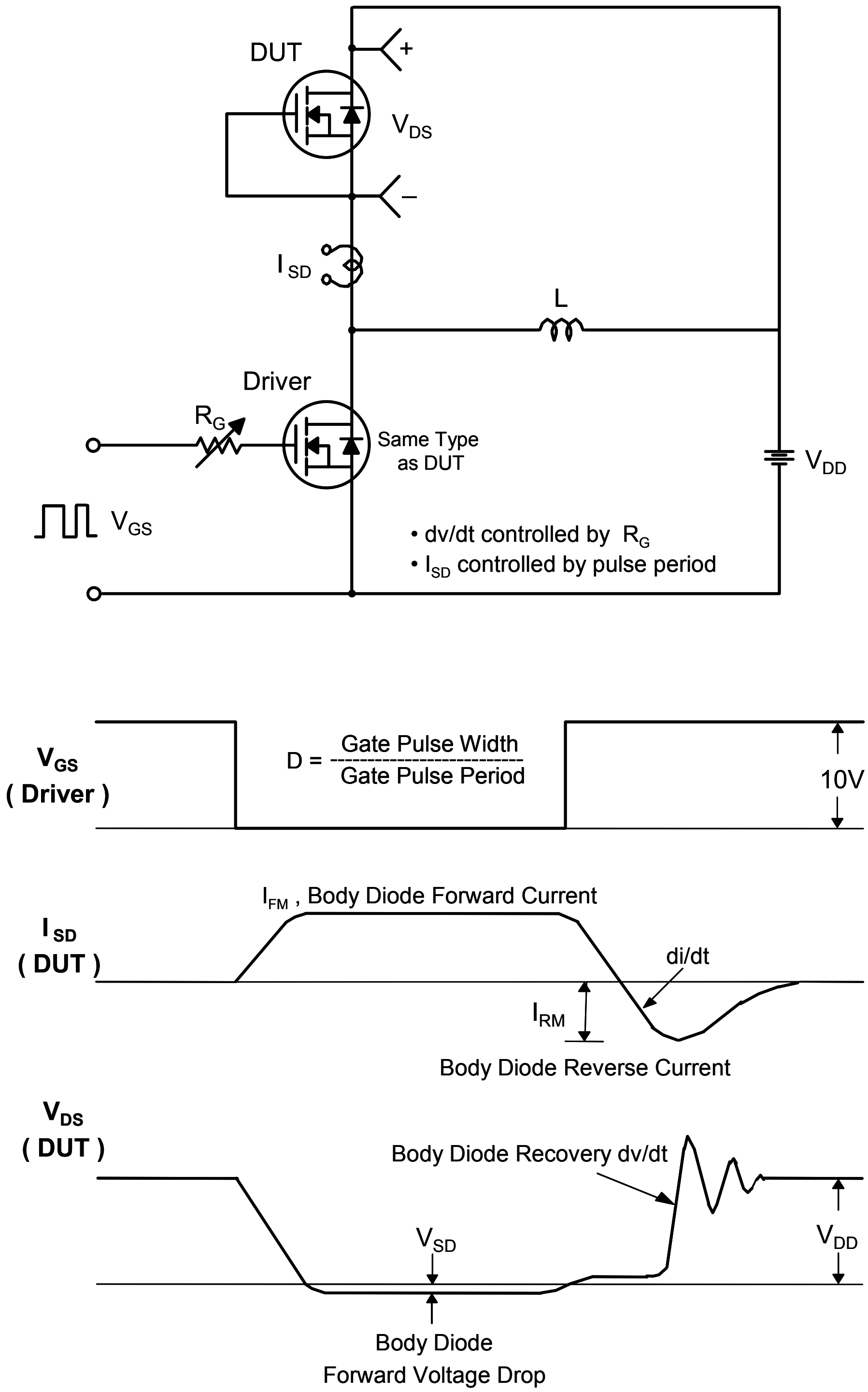


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

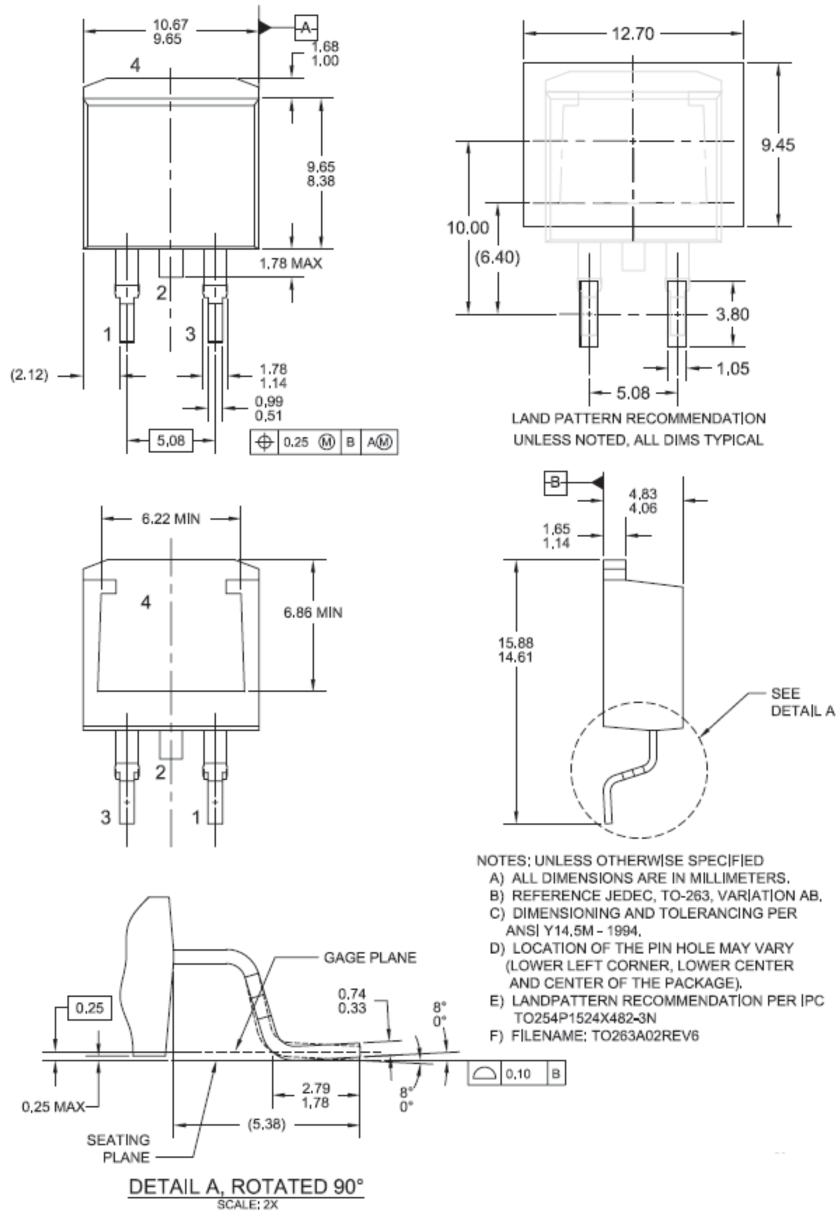


Figure 16. TO263 (D^2PAK), Molded, 2-Lead, Surface Mount

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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